

E Series Power MOSFET



N-Channel MOSFET

FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

PRODUCT SUMMARY

| | | |
|---|-----------------|-------|
| V_{DS} (V) at T_J max. | 650 | |
| $R_{DS(on)}$ typ. (Ω) at 25 °C | $V_{GS} = 10$ V | 0.070 |
| Q_g max. (nC) | 63 | |
| Q_{gs} (nC) | 19 | |
| Q_{gd} (nC) | 10 | |
| Configuration | Single | |

ORDERING INFORMATION

| | |
|---------------------------------|-----------------|
| Package | TO-220AB |
| Lead (Pb)-free and halogen-free | SIHP080N60E-GE3 |

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


| PARAMETER | SYMBOL | LIMIT | UNIT | |
|---|------------------|----------------|------|------|
| Drain-source voltage | V_{DS} | 600 | V | |
| Gate-source voltage | V_{GS} | ± 30 | | |
| Continuous drain current ($T_J = 150$ °C) | V_{GS} at 10 V | $T_C = 25$ °C | 35 | A |
| | | $T_C = 100$ °C | 22 | |
| Pulsed drain current ^a | I_{DM} | 96 | | |
| Linear derating factor | | 1.8 | W/°C | |
| Single pulse avalanche energy ^b | E_{AS} | 226 | mJ | |
| Maximum power dissipation | P_D | 227 | W | |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +150 | °C | |
| Drain-source voltage slope | dv/dt | $T_J = 125$ °C | 100 | V/ns |
| Reverse diode dv/dt ^d | | 10 | | |
| Soldering recommendations (peak temperature) ^c | For 10 s | 260 | °C | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4.0$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $di/dt = 100$ A/ μ s, starting $T_J = 25$ °C



| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|-------------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum junction-to-ambient | R _{thJA} | - | 62 | °C/W |
| Maximum junction-to-case (drain) | R _{thJC} | - | 0.55 | |

| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | | |
|---|----------------------------------|---|--|------|-------|-------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-source breakdown voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | | 600 | - | - | V |
| V _{DS} temperature coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | | - | 0.64 | - | V/°C |
| Gate-source threshold voltage (N) | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | | 3.0 | - | 5.0 | V |
| Gate-source leakage | I _{GSS} | V _{GS} = ± 20 V | | - | - | ± 100 | nA |
| | | V _{GS} = ± 30 V | | - | - | ± 1 | μA |
| Zero gate voltage drain current | I _{DSS} | V _{DS} = 600 V, V _{GS} = 0 V | | - | - | 1 | μA |
| | | V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C | | - | - | 10 | |
| Drain-source on-state resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 17 A | - | 0.070 | 0.080 | Ω |
| Forward transconductance ^a | g _{fs} | V _{DS} = 20 V, I _D = 17 A | | - | 4.6 | - | S |
| Dynamic | | | | | | | |
| Input capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz | | - | 2557 | - | pF |
| Output capacitance | C _{oss} | | | - | 105 | - | |
| Reverse transfer capacitance | C _{rss} | | | - | 6 | - | |
| Effective output capacitance, energy related ^a | C _{o(er)} | V _{DS} = 0 V to 480 V, V _{GS} = 0 V | | - | 79 | - | pF |
| Effective output capacitance, time related ^b | C _{o(tr)} | | | - | 499 | - | |
| Total gate charge | Q _g | V _{GS} = 10 V | I _D = 17 A, V _{DS} = 480 V | - | 42 | 63 | nC |
| Gate-source charge | Q _{gs} | | | - | 19 | - | |
| Gate-drain charge | Q _{gd} | | | - | 10 | - | |
| Turn-on delay time | t _{d(on)} | V _{DD} = 480 V, I _D = 17 A, V _{GS} = 10 V, R _g = 9.1 Ω | | - | 31 | 62 | ns |
| Rise time | t _r | | | - | 96 | 144 | |
| Turn-off delay time | t _{d(off)} | | | - | 37 | 74 | |
| Fall time | t _f | | | - | 31 | 62 | |
| Gate input resistance | R _g | f = 1 MHz, open drain | | 0.3 | 0.7 | 1.4 | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous source-drain diode current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 35 | A |
| Pulsed diode forward current | I _{SM} | | | - | - | 96 | |
| Diode forward voltage | V _{SD} | T _J = 25 °C, I _S = 17 A, V _{GS} = 0 V | | - | - | 1.2 | V |
| Reverse recovery time | t _{rr} | T _J = 25 °C, I _F = I _S = 17 A, di/dt = 80 A/μs, V _R = 25 V | | - | 441 | 882 | ns |
| Reverse recovery charge | Q _{rr} | | | - | 5.2 | 10.4 | μC |
| Reverse recovery current | I _{RRM} | | | - | 21 | - | A |

Notes

- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
- b. C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

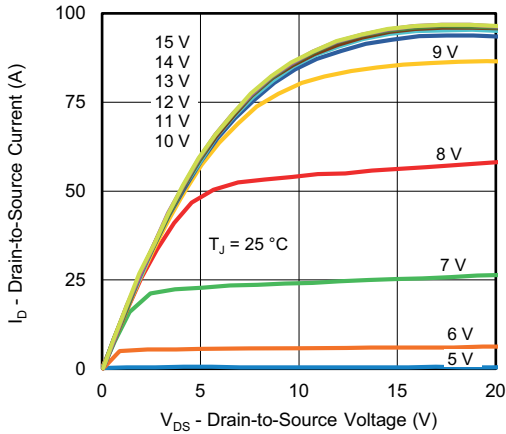


Fig. 1 - Typical Output Characteristics

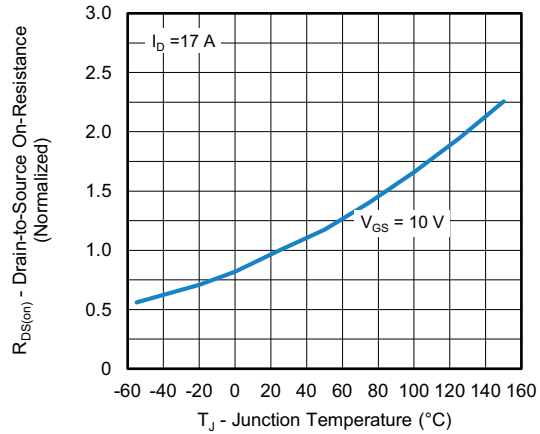


Fig. 4 - Normalized On-Resistance vs. Temperature

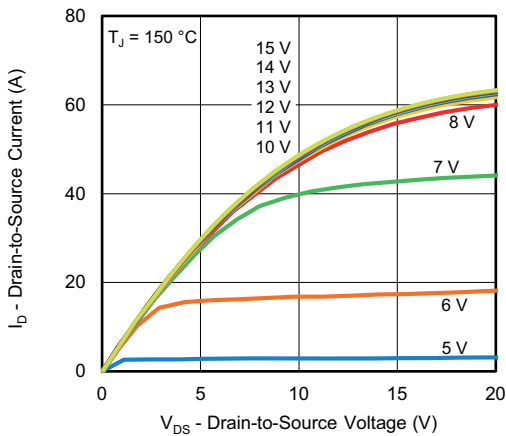


Fig. 2 - Typical Output Characteristics

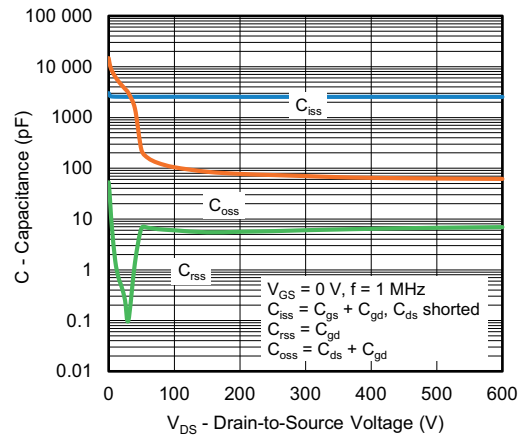


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

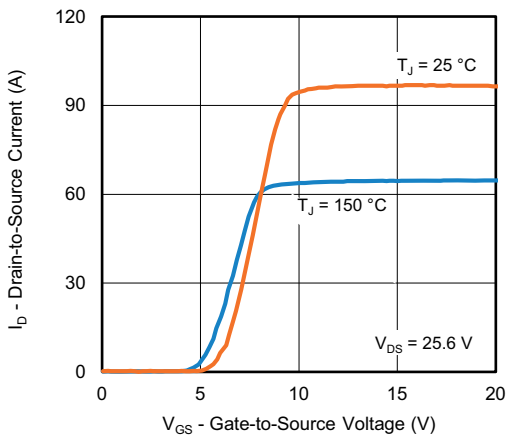


Fig. 3 - Typical Transfer Characteristics

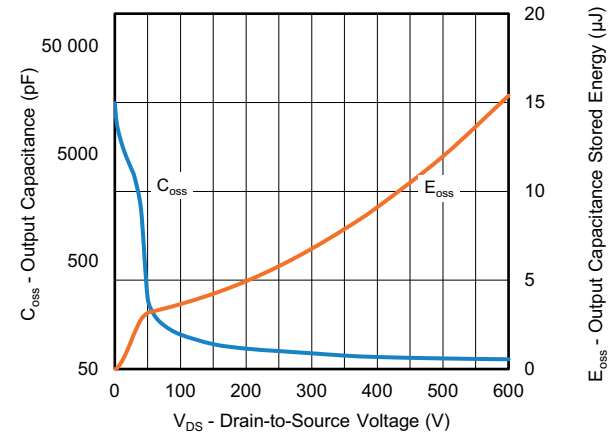


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}



Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

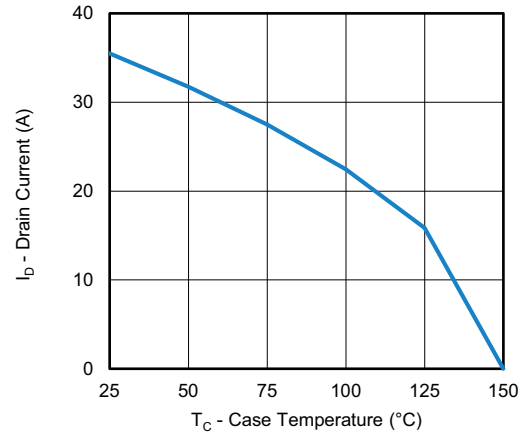


Fig. 10 - Maximum Drain Current vs. Case Temperature

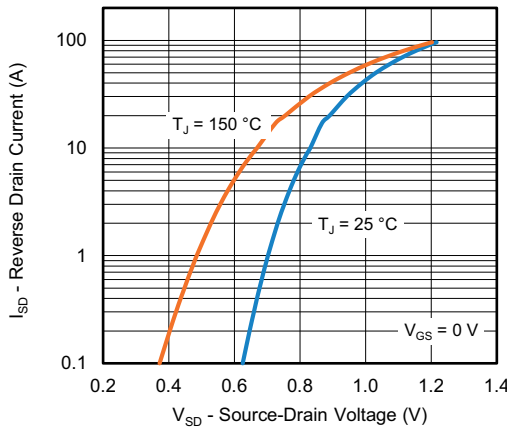


Fig. 8 - Typical Source-Drain Diode Forward Voltage

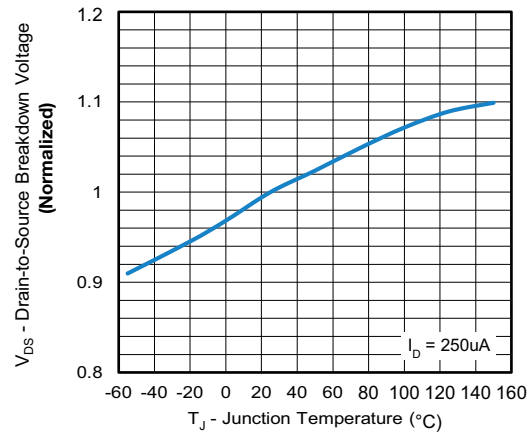


Fig. 11 - Temperature vs. Drain-to-Source Voltage



Fig. 9 - Maximum Safe Operating Area

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

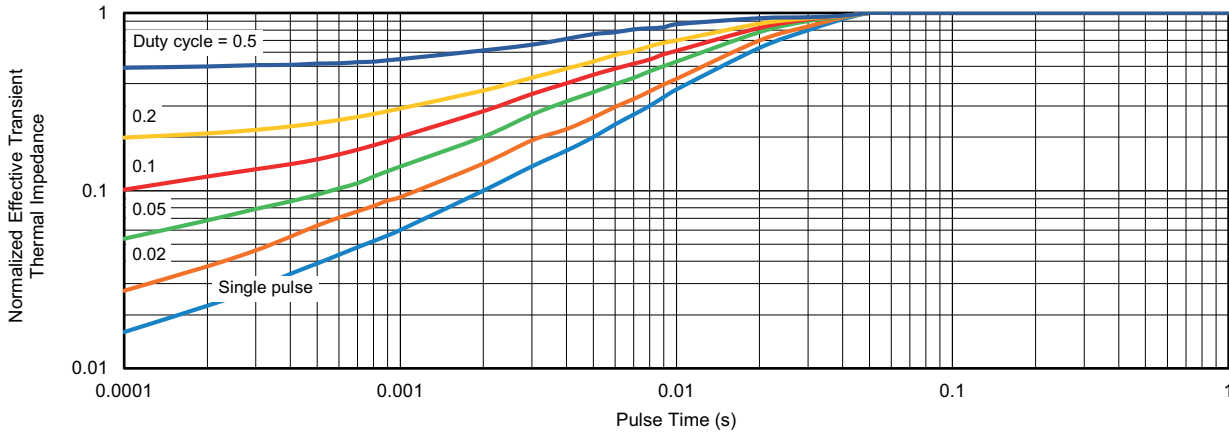


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

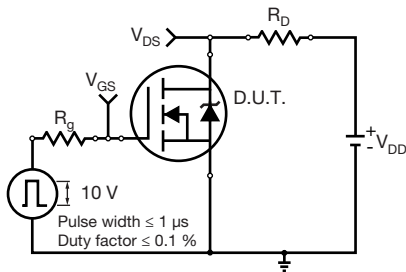


Fig. 13 - Switching Time Test Circuit

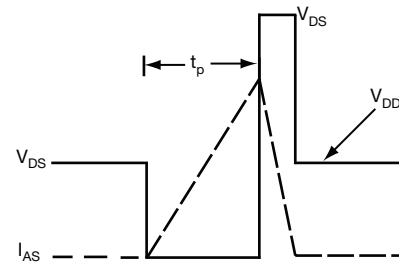


Fig. 16 - Unclamped Inductive Waveforms

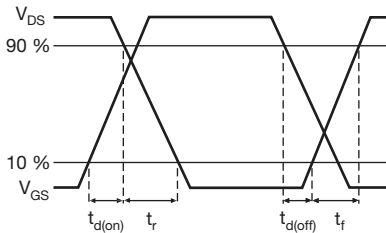


Fig. 14 - Switching Time Waveforms

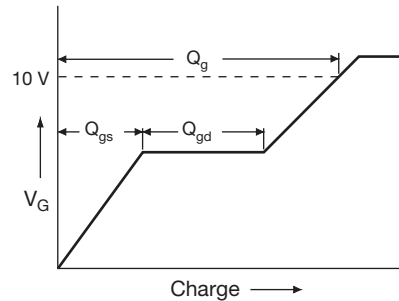


Fig. 17 - Basic Gate Charge Waveform

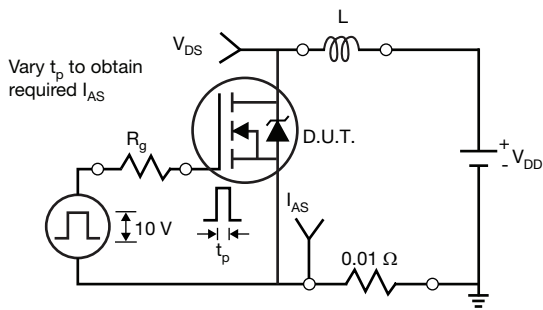


Fig. 15 - Unclamped Inductive Test Circuit

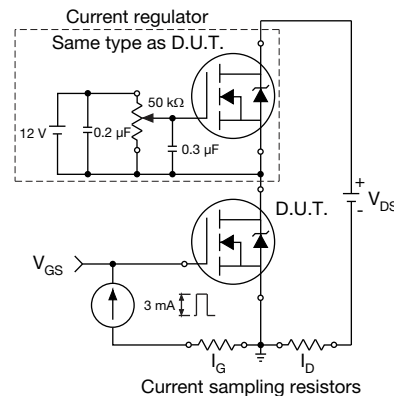


Fig. 18 - Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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