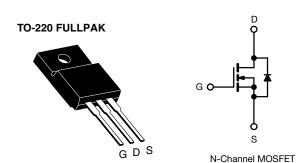
# Vishay Siliconix

# **D Series Power MOSFET**



PRODUCT SUMMARY				
V <sub>DS</sub> (V) at T <sub>J</sub> max.	550			
R <sub>DS(on)</sub> max. (Ω) at 25 °C	V <sub>GS</sub> = 10 V	1.5		
Q <sub>g</sub> max. (nC)	20			
Q <sub>gs</sub> (nC)	3			
Q <sub>gd</sub> (nC)	5			
Configuration	Sing	le		

### **FEATURES**

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance (Ciss)
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- · Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM): Ron x Qg
  - Fast switching
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

### **APPLICATIONS**

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding
  - Induction heating
  - Motor drives
- · Battery chargers

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF5N50D-E3

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub>	= 25 °C, unl	ess otherwis	se noted)		
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			$V_{DS}$	500	
Gate-Source Voltage			.,	± 30	V
Gate-Source Voltage AC (f > 1 Hz)			$V_{GS}$	30	
Continuous Drain Correct /T 150 °C) 6	V at 10 V	T <sub>C</sub> = 25 °C		5.3	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>e</sup>	V <sub>GS</sub> at 10 V	$T_C = 25 \degree C$ $T_C = 100 \degree C$	I <sub>D</sub>	3.4	Α
Pulsed Drain Current a			I <sub>DM</sub>	10	
Linear Derating Factor				0.24	W/°C
Single Pulse Avalanche Energy b			E <sub>AS</sub>	23	mJ
Maximum Power Dissipation			$P_{D}$	28.8	W
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Drain-Source Voltage Slope T <sub>J</sub> = 125 °C		dV/dt	24	V/no	
Reverse Diode dV/dt <sup>d</sup>			0.28	- V/ns	
Soldering Recommendations (Peak temperature) c For 10 s			300	°C	
Mounting Torque M3 screw			0.6	Nm	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b.  $V_{DD} = 50$  V, starting  $T_J = 25$  °C, L = 2.3 mH,  $R_q = 25$   $\Omega$ ,  $I_{AS} = 5$  Å.
- c. 1.6 mm from case.
- d.  $I_{SD} \le I_D$ , starting  $T_J = 25$  °C.
- e. Limited by maximum junction temperature.



# Vishay Siliconix

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	4.1	C/VV

PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static				•			
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> =	= 0 V, I <sub>D</sub> = 250 μA	500	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I <sub>D</sub> = 250 μA	-	0.58	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> =	· V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3	-	5	V
Gate-Source Leakage	I <sub>GSS</sub>	,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 100	nA
Zava Cata Valtaga Dvaia Cuwant		V <sub>DS</sub> =	= 500 V, V <sub>GS</sub> = 0 V	-	-	1	. ^
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 400 V	', V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	10	μA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 2.5 A	-	1.2	1.5	Ω
Forward Transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> :	= 20 V, I <sub>D</sub> = 2.5 A	-	1.8	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	$V_{GS} = 0 V$ ,		-	325	-	
Output Capacitance	C <sub>oss</sub>	]	V <sub>DS</sub> = 100 V,	-	34	-	
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		-	6	-	1
Effective Output Capacitance, Energy Related <sup>b</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		-	31	-	pF
Effective Output Capacitance, Time Related <sup>c</sup>	C <sub>o(tr)</sub>	$v_{DS} = 0$	v to 400 v, v <sub>GS</sub> = 0 v	-	41	-	
Total Gate Charge	Qg			-	10	20	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$I_D = 2.5 \text{ A}, V_{DS} = 400 \text{ V}$	-	3	-	nC
Gate-Drain Charge	Q <sub>gd</sub>			-	5	-	
Turn-On Delay Time	t <sub>d(on)</sub>			-	12	24	
Rise Time	t <sub>r</sub>	V <sub>DD</sub> =	400 V, I <sub>D</sub> = 2.5 A	-	11	22	, no
Turn-Off Delay Time	t <sub>d(off)</sub>	$R_g = 9.1 \Omega, V_{GS} = 10 V$		-	14	28	ns
Fall Time	t <sub>f</sub>			-	11	22	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		-	1.7	-	Ω
<b>Drain-Source Body Diode Characteristic</b>	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the		-	-	5	^
Pulsed Diode Forward Current	I <sub>SM</sub>	integral revers P - N junction		-	-	20	A
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °	C, I <sub>S</sub> = 4 A, V <sub>GS</sub> = 0 V	-	-	1.2	V
Reverse Recovery Time	t <sub>rr</sub>			-	320	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>		5 °C, I <sub>F</sub> = I <sub>S</sub> = 2.5 A, 100 A/µs, V <sub>B</sub> = 20 V	-	1.2	-	μC
Reverse Recovery Current	I <sub>RRM</sub>	u/ui =	100 AV 40, VR = 20 V	-	8	-	Α

#### Note

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .
- c.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

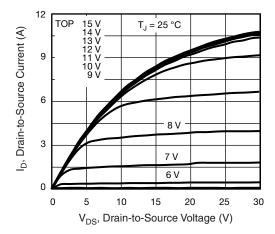


Fig. 1 - Typical Output Characteristics

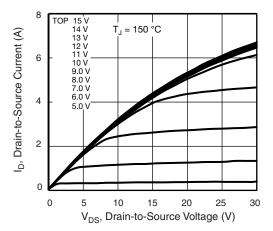


Fig. 2 - Typical Output Characteristics

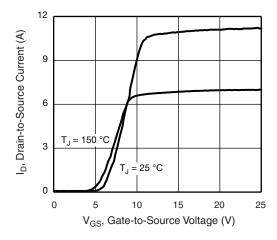


Fig. 3 - Typical Transfer Characteristics

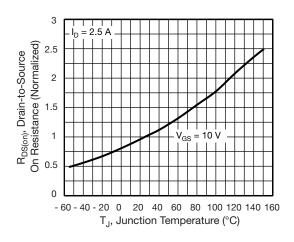


Fig. 4 - Normalized On-Resistance vs. Temperature

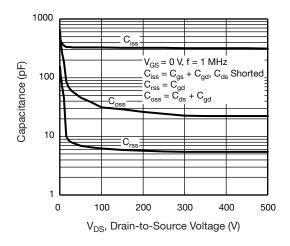


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

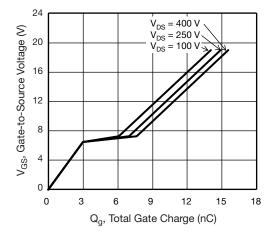


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



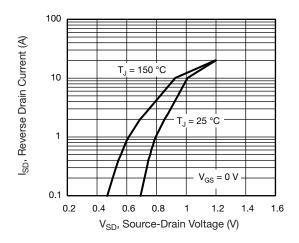


Fig. 7 - Typical Source-Drain Diode Forward Voltage

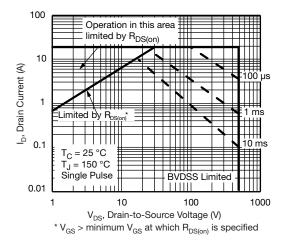


Fig. 8 - Maximum Safe Operating Area

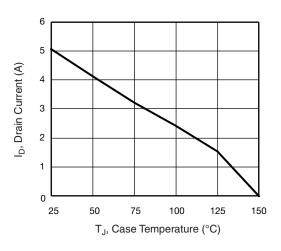


Fig. 9 - Maximum Drain Current vs. Case Temperature

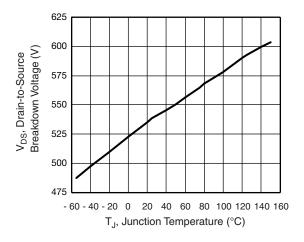


Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature

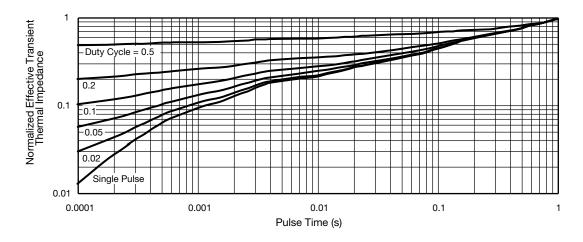


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

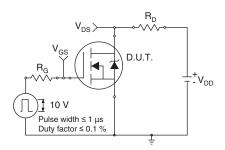


Fig. 12 - Switching Time Test Circuit

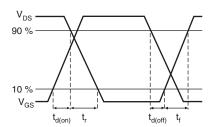


Fig. 13 - Switching Time Waveforms

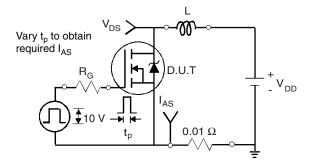


Fig. 14 - Unclamped Inductive Test Circuit

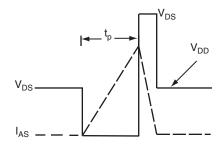


Fig. 15 - Unclamped Inductive Waveforms

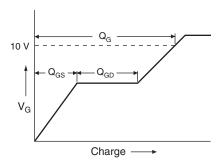


Fig. 16 - Basic Gate Charge Waveform

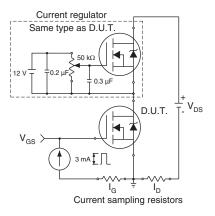
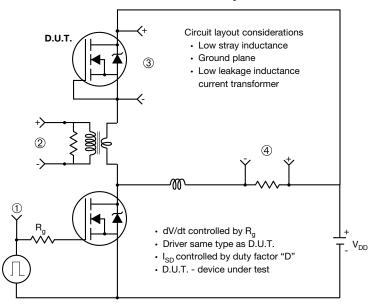


Fig. 17 - Gate Charge Test Circuit



## Peak Diode Recovery dV/dt Test Circuit



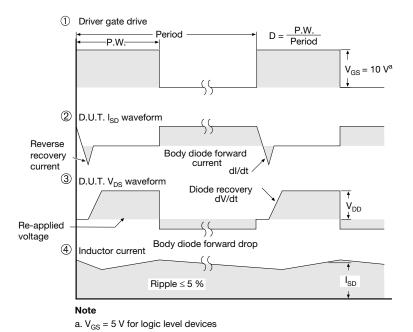


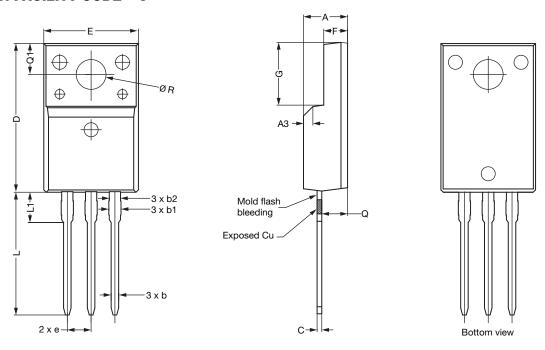
Fig. 18 - For N-Channel

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Vishay Siliconix

# **TO-220 FULLPAK (High Voltage)**

## **OPTION 1: FACILITY CODE = 9**



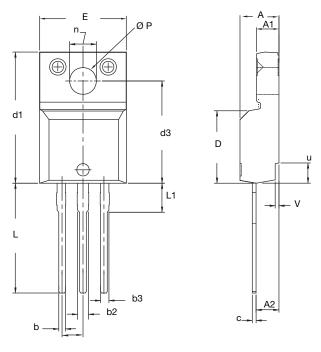
		MILLIMETERS	
DIM.	MIN.	NOM.	MAX.
Α	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
С	0.45	0.50	0.63
D	15.80	15.87	15.97
е		2.54 BSC	
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
ØR	3.08	3.18	3.28

#### **Notes**

- 1. To be used only for process drawing
- 2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
- 3. All critical dimensions should C meet  $C_{pk} > 1.33$
- 4. All dimensions include burrs and plating thickness
- 5. No chipping or package damage
- 6. Facility code will be the 1st character located at the 2nd row of the unit marking



## **OPTION 2: FACILITY CODE = Y**



	MILLIN	MILLIMETERS		HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
С	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
Е	10.360	10.630	0.408	0.419
е	2.54	BSC	0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
ØΡ	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019 DWG: 5972

#### Notes

- 1. To be used only for process drawing
- 2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
- 3. All critical dimensions should C meet  $C_{pk} > 1.33$
- 4. All dimensions include burrs and plating thickness
- 5. No chipping or package damage
- 6. Facility code will be the 1st character located at the 2nd row of the unit marking



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Vishay

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