Si7210 I²C Hall Effect Magnetic Position and Temperature Sensor Data Sheet

The Si7210 family of Hall effect magnetic sensors from Silicon Labs combines a chopper-stabilized Hall element with a low-noise analog amplifier, 13-bit analog-to-digital converter, and an I²C interface. Leveraging Silicon Labs' proven CMOS design techniques, the Si7210 family incorporates digital signal processing to provide precise compensation for temperature and offset drift.

Compared with existing Hall effect sensors, the Si7210 family offers industry-leading sensitivity, which enables use with larger air gaps and smaller magnets. The integrated 13-bit high-precision ADC delivers high output linearity with very low noise for the highest measurement accuracy. For battery-powered applications, the Si7210 family offers very low power consumption to improve operating life. For automotive applications, the Si7210 family is AEC-Q100 qualified.

The Si7210 family supports a bidirectional I²C interface which provides full configurability of the Hall effect sensor. At any time, the 13-bit magnetic field strength can be read through the I²C interface.

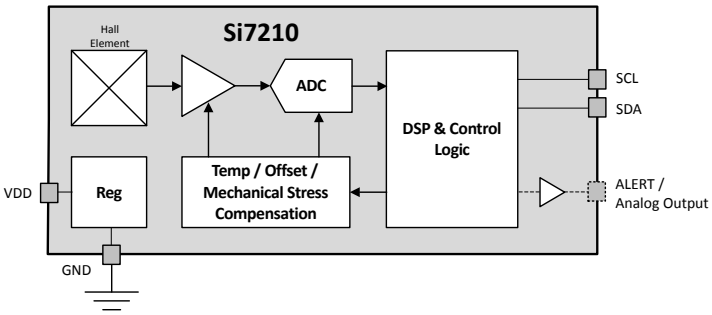
The Si7201 is offered in a 5-pin SOT23 or 8-pin DFN package. In the 5-pin package, the additional output pin is available, which can provide either a digital alert or a ratiometric analog output voltage corresponding to the measured field strength (see ordering guide). The digital alert function can be used as an interrupt to notify the MCU or other components when the magnetic field has exceeded a predefined threshold. For high-bandwidth field sensing, the ratiometric analog output is configurable with a bandwidth up to 20 kHz.

Applications:

- Mechanical position sensing in consumer, industrial, and automotive applications
- Replacement of reed switches
- Fluid level measurement
- Speed sensing - Utility meters
- Control knobs and selector switches

FEATURES

- High-Sensitivity Hall Effect Sensor
  - Adjustable Full Scale (Standard Offerings are ±20mT and ±200 mT Full Scale)
  - Integrated Digital Signal Processing for Temperature and Offset Drift Compensation
  - High-Precision 13-bit Signal Path
  - Output Bandwidth up to 20 kHz
  - Sensitivity Drift < ±3% overTemperature
- Digital I²C Interface
  - Four Selectable I²C Addresses
  - Optional Digital Alert Output
  - Optional Ratiometric Analog Output
- Wide 1.7 to 5.5 V Power Supply Voltage
- Temperature Sensor Data also available by I²C (accuracy ±1°C)
- Low 100 nA Sleep Mode Current Consumption
- AEC-Q100 Qualified for Automotive Applications
- Industry-Standard Packaging
  - Surface-Mount SOT23
  - 1.4 x 1.6 mm 8-pin DFN package (coming soon)



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1. Electrical Specifications

Unless otherwise specified, all min/max specifications apply over the recommended operating conditions.

Table 1.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply	V_{DD}		1.71		5.5	V
Temperature	T_A	E grade	-40		+125	°C

Table 1.2. General Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage high	V_{IH}	SCL, SDA pins	0.7 x V_{DD}	-	-	V
Input Voltage Low	V_{IL}	SCL, SDA pins	-	-	0.3 x V_{DD}	V
Input voltage range	V_{IN}	SCL, SDA with respect to ground	0		V_{DD}	V
Input Leakage	I_{IL}	SDA, SCL		< 0.1	1	µA
Output voltage low	V_{OL}	SCL, SDA I_{OL} = 3 mA V_{DD} > 2 V			0.4	V
		SCL, SDA I_{OL} = 2 mA V_{DD} > 1.7 V			0.2	V
		SCL, SDA I_{OL} = 6 mA V_{DD} > 2 V			0.6	V
Current Consumption	I_{DD}	Conversion in progress: 1.8 V 3.3 V 5.0 V		 3.9 5.2 6.6		mA
		Sleep Mode		100		nA
		Idle mode		360		µA
		Analog out enable (additive must be idle or conversion in progress)		450		µA
		Sleep timer enabled average at V_{DD} = 3.3 V		0.4		µA
Conversion time	T_{CONV}	Conversion time for first measurement in a burst[1]		11		µS
		Additional conversions in a burst		8.8		µS
Sleep time	T_{SLEEP}	Factory configurable from 1 to 200 msec ±20%				

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Idle time[2]	T_{IDLE}	slTime = 0x01 SlFast = 1	11.9	13.2	14.5	usec
		slTime = 0xFF SlFast = 0	185	206	227	msec
Wake up time	TWAKE	Time from V_{DD} > 1.7 V to first measurement			2	msec

Note:
1. Plus 9.4 µsec typical in idle state.
2. Part can go to either idle more or sleep mode between conversions. If part is in idle mode with slTime = 0x00 and slFast = 1 conversion are continuous at 8.8 µsec interval.

Table 1.3. Output Pin Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage low Output pin open drain or push pull	V_{OL}	I_{OL} = 3 mA V_{DD} > 2 V			0.4	V
		I_{OL} = 2 mA V_{DD} > 1.7 V			0.2	V
		I_{OL} = 6 mA V_{DD} > 2 V			0.6	V
Leakage Output high Output pin open drain	I_{OH}				1	µA
Output voltage high Output pin push pull	V_{OH}	I_{OH} = 2 mA V_{DD} >2.25 V	V_{DD} – 0.4			V
Slew rate Digital output mode	T_{SLEW}			5		$\%V_{DD}$/nS
Analog output mode parameters						
Offset[1]	B_{OFF}	V_{DD} = 5 V		±300		µT
Ratiometric gain error	RGE	Change in gain as function of supply for V_{DD} > 2.25.		±0.25		%/V
Total Harmonic Distortion	THD	Vout inside 20-80% of V_{DD}, V_{DD} > 2.5 V		0.15		%
Short circuit protection	I_{SS}	Output shorted to ground or V_{DD}		±15		mA

Note:
1. Deviation from $V_{DD}/2$. To get voltage offset, divide by gain typically 40 mT/V_{DD} or 400 mT/V_{DD}.

Table 1.4. I²C Interface Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}		0		400	kHz
Start condition hold time	t_{SDH}		0.6			µsec
LOW period of SCL	t_{SKL}		1.3			µsec
HIGH period of clock	t_{SKH}		0.6			µsec
Set up time for a repeated start	$t_{SU;STA}$		0.6			µsec
Data hold time	t_{DH}		0			
Data set up time	t_{DS}		100			nsec
Set up time for a STOP condition	t_{SPS}		0.6			µsec
Bus free time between STOP and START	t_{BUF}		1.3			µsec
Data valid time (SCL low to data valid)	$t_{VD;DAT}$				0.9	µsec
Data valid acknowledge time (time from SCL low to SDA low)	$t_{VD;ACK}$				0.9	µsec
Hysteresis		Digital input hysteresis SDA and SCL	7		17	$\%V_{DD}$
Suppressed pulse width[1]	tSP		50			nsec

Note:
1. Pulses up to and including 50 nsec will be suppressed.

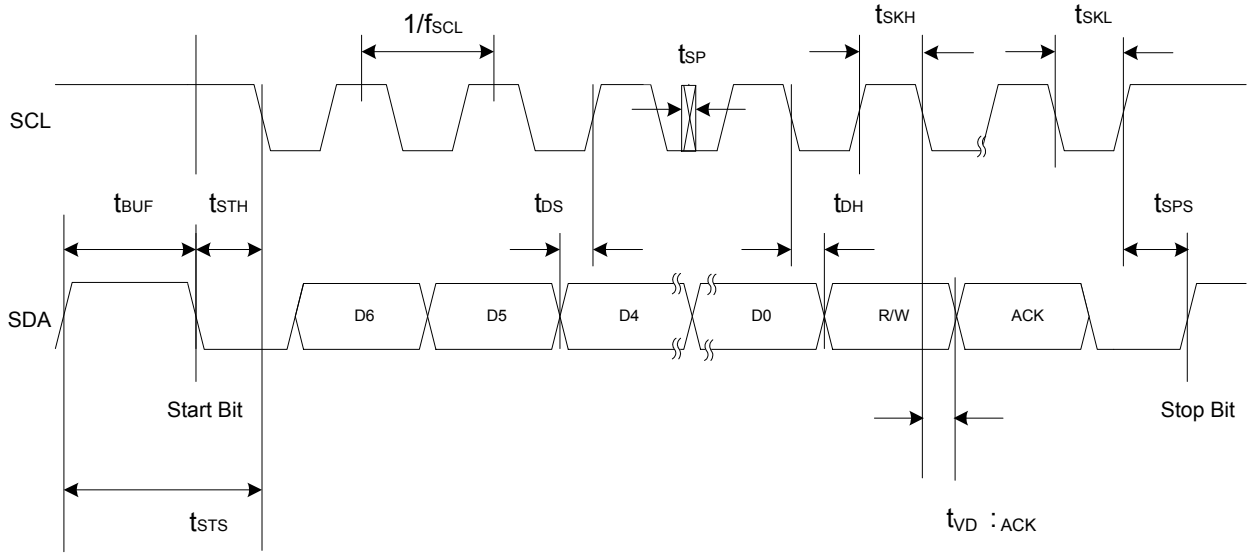


Figure 1.1. I²C Interface Timing

Table 1.5. Magnetic Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset (digital output mode)	B_{OFF}	20 mT scale Full temperature and V_{DD} range		±250	±400	µT
		0 - 70°C and 1.71 V to 3.6 V			±250	µT
Gain accuracy		0 - 70°C			5	%
		Full temperature range			8	%
RMS Noise[1]		room Temp, 20 mT range, V_{DD} = 5 V		30		µT rms

Note:
1. For a single conversion. This may be reduced by filtering.

Table 1.6. Temperature Compensation

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Gain variation with temperature		No compensation 0 - 70°C		< +/-0.05		%/°C
		Neodymium compensation		-0.12		%/°C
		Ceramic compensation		-0.2		%/°C

Table 1.7. Average Temperature Measurement Error

Parameter	Symbol	Test Conditon	Min	Typ	Max	Unit
Average temperature measurement error after gain and offset correction		-10 to +85°C			±1	°C

Table 1.8. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to air thermal resistance	θ_{JA}	JEDEC 4 layer board no airflow SOT23-5	212.8	°C/W
Junction to board thermal resistance	θ_{JB}	JEDEC 4 layer board no airflow SOT23-5	45	°C/W
Junction to air thermal resistance	θ_{JA}	JEDEC 4 layer board no airflow SOT23-3	254.6	°C/W

Parameter	Symbol	Test Condition	Value	Unit
Junction to board thermal resistance	θ_{JB}	JEDEC 4 layer board no airflow SOT23-3	54.8	°C/W

Table 1.9. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature under bias			-55		125	°C
Storage temperature			-65		125	°C
Voltage on I/O pins			-0.3		V_{DD}+0.3	V
Voltage on VDD with respect to ground			-0.3		TBD	V
ESD tolerance		HBM			2	kV
		CDM			1.25	kV

Note:

1. Absolute maximum ratings are stress ratings only, operation at or beyond these conditions is not implied and may shorten the life of the device or alter its performance.

2. Functional Description

The Si7210 family of parts are I2C programmable Hall effect magnetic position sensors. These parts digitize the component of the magnetic field in the z axis of the device (positive field is defined as pointing into the device from the bottom). The parts are normally used to detect the presence or absence of a magnet in security systems, as position sensors or for counting revolutions.

In addition to being able to control the conversion process and read the result of magnetic field conversions by I2C, the 5-pin packages offer an output pin. The output pin can act as an alert (push pull or open collector) which goes high or low when the magnetic field crosses a threshold. Alternatively the output pin can be configured as an analog output. In analog mode, the pin is nominally at $V_{DD}/2$ and goes high or low with the magnetic field. The output pin configuration is determined by the type of part ordered (this is not I2C configurable).

The parts are preconfigured for the magnetic field measurement range, sleep time, temperature compensation, tamper threshold, and digital filtering, and will wake into the preconfigured mode when first powered. The specific configuration, as well as the I2C address and output type (open collector or push pull), are determined by the part number. Magnetic field trip points are typically configured by I2C, and the part is allowed to go into its normal sleep and measurement cycle. If the bit `Usestore` is set to 1, the output pin trip points are retained in sleep mode. Data other than magnetic field trip points is not retained in sleep mode. If there is not a need to go to full sleep mode, the other parameters may be configured, and this data will be kept in idle mode.

Note: For parts that have an analog output, sleep mode is not an option. For this reason, analog output parts are only orderable in one configuration.

Following is a list of I2C interface configurable options:

- *Measurement range*. This is normally set so that after temperature compensation the full scale (15b unsigned) digital output is ±20.47 mT (0.00125 mT/bit) or ±204.7 mT (0.0125 mT/bit). (Note: 1 Gauss = 0.1 mT). For convenience these are referred to as the 20 mT and 200 mT scales.
- *Digital filtering*. To reduce noise in the output (normally 0.03 mT RMS on the 20 mT scale), digital filtering can be applied. The digital filtering can be done to a burst of measurements (FIR filter) or can be configured to average measurements in IIR style. The filtering can be done over a number of samples in powers of 2 (1,2,4,8,…) for up to 2^{12} (4096) samples.
- *Time between measurements* (or measurement bursts for the case of FIR filtering)
  - For lowest power, the part can be configured to sleep between measurements, if the time is long enough and it is not in analog output mode. However, remember some configuration data is lost in sleep mode.
  - For faster measurement rates and for analog output mode, the part is configured to idle between samples.
  - The part can also be configured to take a single measurement on command.
- *The digital output pin* (for parts that support this option)
  - Threshold at which the digital output will change for increasing field (Bop) and for decreasing field (Brp).
  - The direction in which the output pin goes in response to an increase in field
  - There is an option to take the magnitude of the field prior to the comparison so that the polarity is not field dependent
  - The settings will be retained in sleep mode.
  - A “tamper threshold”. This is intended to signal the presence of a strong magnet, which may indicate tampering. In the case of tamper detection, the output pin will go to its zero field value (which in security systems is normally an indication of door or window open).
- *The analog output pin* (for parts that support this option)
  - The direction the pin goes as magnetic field increases
- *Temperature compensation of the magnetic field response to compensate for the nominal drop in magnetic field output of common magnets with increasing temperature.*
- *An on chip coil that generates a large enough field to allow self-test of the sensor*
  - The coil can be turned on in either polarity

For greater precision in programming the part, a number of calibration data points are stored in memory (OTP).

- The nominal magnetic field output of the on-chip coil normalized to the power supply voltage
- Coefficients to be used for setting gain and temperature compensation

3. I2C Interface

The Si7210 complies with “fast” mode I2C operation and 7 bit addressing at speeds up to 400 kHz. The I2C address is factory programmed to one of 4 values 0x30, 0x31, 0x32, or 0x33 (0110000b through 0110011b).

At power-up the registers are initialized, as will be described in the register definitions, and then they can be read or written in standard fashion for I2C devices. A special sequence must be used to read OTP data, as will be described.

The host command for writing an I2C register is:

```
START Address W ACK register ACK data ACK STOP
```

The host command for reading an I2C register is:

```
START Address W ACK register ACK Sr Address R Data NACK* STOP
```

*NACK by host

Where:

START is SDA going low with SCL high

Sr is a repeated START

Address is 0x30 up to 0x33

0 indicates a write and 1 indicates a read

ACK is SDA low

Data is the Read or Write data

NACK is SDA high

STOP is SDA going high with SCL high

Writing or Reading of sequential registers can be supported by setting the `arautoinc` bit of register 0xC5 (see register description). In the case of a read sequence where the `arautoinc` bit has been set, the data can be ACK’d to allow reading of sequential registers. For example, a two byte read of the conversion data in registers 0xC1 and 0XC2 would be:

```
START Address W ACK 0xC1 ACK Sr Address ACK data ACK* data NACK* STOP
```

*ACK/NACK by host

To wake a part from sleep mode or to interrupt a measurement loop from idle mode,

send the sequence

```
START Address W ACK STOP
```

In this case, if the host continued with a register, the Si7210 would NACK which would be unexpected.

or use:

```
START Address R ACK data NACK STOP
```

*NACK by host

In this case the Si7210 will produce 0xFF for the data.

Allow 10 µsec between the ACK of the address and the next START for the Si7210 to wake from sleep. In most cases this will happen automatically due to the 400 KHz maximum speed of the I2C bus.

The sequence will put the part in idle mode with the `stop` bit set.

Note: It is recommended that the part be put in stop mode prior to changing data that will affect a measurement outcome.

To make a single conversion having woken the part, set the `oneburst` bit of register 0xC4 to 1 and the `stop` bit to 0. The `stop` bit resets to 1 by the time the measurement is complete.

To put the part back to sleep after reading the data, set `stop` bit to 0. The bit `sltimeena` is normally factory set to 1, so it does not need to be set. The bit `sleep` is not set.

To put the part to sleep with no measurements (sleep timer disabled), set the `sltimeena` bit to 0 and write the `sleep` bit to 1 and the `stop` bit to 0. In most cases `sltimeena` is factory set to 1 and, the `sltimeena` bit must be cleared on every subsequent wake up if this operation is desired.

If it is desired to re-enable the sleep timer having put the part to sleep with sleeptimer disabled, then wait 500 µsec after setting the sltimeena bit before putting the part to sleep.

4. Register Definitions

The Si7210 has 21 registers in locations 0xC0 – 0xE4.

Configuration data is loaded at start up from OTP data and can be modified by I2C writes.

Note: This data will be reloaded when the part wakes from sleep mode (other than 0xC6 and 0xC7 which are not reloaded if bit `Usestore` is set).

ADDR	7	6	5	4	3	2	1	0
0xC0	chipid (RO)				revid (RO)			
0xC1	Dspsigm							
0xC2	Dspsigl							
0xC3						dspsigsel		
0xC4	meas(RO)				Usestore	oneburst	stop	sleep
0xC5								arautoinc
0xC6	sw_low4field	sw_op						
0xC7	sw_fieldpolsel		sw_hyst					
0xC8	Sltime							
0xC9	sw_tamper						Slfast	sltimeena
0xCA	a0							
0xCB	a1							
0xCC	a2							
0xCD	df_burstsize			df_bw				df_iir
0xCE	a3							
0xCF	a4							
0xD0	a5							
0xE1	otp_addr							
0xE2	otp_data							
0xE3							otp_read_en	otp_busy(RO)
0xE4							tm_fg	

As can be seen many of the bit fields are not aligned with register boundaries. When writing a particular bit field, it is best to use a read, modify, write procedure to ensure that other bit fields are not unintentionally changed. That is, read the register, modify the bit field of interest while keeping other bits the same, and then write the register back. Unspecified bits should not be changed from the factory configuration.

4.1 Field Descriptions

4.1.1 Chip ID

`chipid (RO)` – This ID 0x1 for all Si7210 parts.

`revid (RO)` – This ID 0x1 for revision A.

4.1.2 Fields Associated with Reading DATA

`Dspsigm` – Bits [6:0] are the most significant byte of the last conversion result. The most significant bit is a “fresh” bit indicating the register has been updated since last read. Reading the `Dspsigm` register causes the register `Dspsigl` to be loaded with the least significant byte of the last conversion result.

`Dspsigl` – The least significant byte of the last conversion result. Read `Dspsigm` first to align the bytes. The complete 15b unsigned result is `256*Dspsigm[6:0]+Dspsigl[7:0]`. A result of 16384 means zero field. More negative results mean negative field, and more positive results mean more positive field. With the normal recommended gain settings, the magnetic field data is scaled to 1 LSB = 0.00125 mT (±20.47 mT full scale) or 1 LSB = 0.0125 mT (±204.7 mT full scale)

`Dspsigsel` – For magnetic field measurement dspsigsel is set to 100b (decimal 4). This is the power up value.

Setting `dspsigsel` to 0x01 will give the output of an internal temperature sensor. See also 5. Making Temperature Measurements.

`meas(RO)` – indicates a measurement is in process. In most cases this bit is not needed as the fresh bit of `Dspsigm` can be used instead.

`Oneburst` – Setting this bit initiates a single conversion. Set `stop` = 0 when setting `oneburst` = 1. The `Oneburst` bit will auto clear once the conversion initiates and the `stop` bit will be set to 1 when the conversion completes.

`stop` - Setting this bit causes the control state machine measurement loop to pause after the current measurement burst completes. Once set, clearing this bit restarts the measurement loop.

`sleep` - Setting this bit causes the part to enter sleep mode after the current measurement burst completes. Once set, clearing this bit restarts the measurement loop.

`arautoinc` – enables auto increment of the I2C register address pointer. This bit is not retained in sleep mode

4.1.3 Fields Associated with Configuring the Output Pin

`Usestore` – Setting this bit causes the current state of OTP registers for the `sw_op`, `sw_hyst`, `sw_low4field`, and `sw_fieldpolsel` bits to be saved and restored during the next sleep and wakeup sequence instead of using data read from the OTP.

Note: Allowing a part to enter sleep mode will result in reloading other parameters, such as the filtering data. This bit will also be retained in sleep mode.

`sw_low4field` - selects logic sense; output is low when the field is strong when the bit is set. Output is high when the field is strong when the bit is cleared.

`sw_op` – this 7 bit number sets the center point of the decision point for magnetic field high or low. The actual decision point is the center point plus or minus the hysteresis.

The 15b data that can be read from I2C is truncated to 13b prior to the logic that makes the decision. The middle of the decision point relative to full scale (13b signed or +/-4096 counts) is:

$$threshold = \left(16 + sw\_op\left[3:0\right]\right) \times 2^{swop[6:4]}$$

threshold = 0, when sw_op = 127

These numbers run from 16 to 3840. On the 20 mT scale each LSB of the 15b number is 0.00125 mT. In 13b representation the LSB is 0.005 mT/bit so the middle of the decision point can be programmed from 0.08 mT to 19.2 mT (16*0.005 to 3840*0.005).

Similarly, on the 200 mT scale, the middle point of the decision threshold can be programmed from 0.8 mT to 192 mT.

The special case of `sw_op = 127` is for “latches”. A Hall effect latch is like a Hall effect switch except the decision points are generally symmetrical around zero. A Hall effect latch is useful for detecting wide range of motion such as a garage door where there are magnets of opposite polarities at the extremes of travel.

`sw_fieldpolsel`

- 00b: absolute value of the field is taken before comparing to threshold (omnipolar)
- 01b: field is multiplied by -1 before being compared to (positive) threshold (unipolar operating in negative field region)
- 01b: field is multiplied by 1 before being compared to (positive) threshold (unipolar operating in positive field region). Also compatible with Latch operation.
- 11b: unused

Note: For analog output mode, the output pin is nominally at $V_{DD}/2$ and goes up and down with magnetic field. This setting can configure the direction the analog output pin moves with magnetic field

`sw_hyst` - the formula for switch hysteresis is:

$$hysteresis = \left(8 + sw\_hyst\left[2:0\right]\right) \times 2^{sw\_hyst[5:3]}$$

If `sw_op` = 127, (latch mode) the hysteresis is multiplied by 2

When `sw_hyst` = 63, the hysteresis is set to zero.

These numbers can range from 8 to 1792 or 16 to 3584 when the sensor is in “latch” mode with `sw_op` = 127.

On the 20 mT scale this corresponds to ±0.04 mT to ±8.96 mT hysteresis when the part is in switch mode and ±0.08 mT to ±17.92 mT in latch mode. On the 200 mT scale, these numbers are multiplied by 10.

Note that

$$Bop = (sw\_op + sw\_hyst) \times \frac{0.05mT}{bit}, \text{ or } = (sw\_op + sw\_hyst) \times \frac{0.5mT}{bit}$$

And

$$Brp = (sw\_op - sw\_hyst) \times \frac{0.05mT}{bit}, \text{ or } = (sw\_op - sw\_hyst) \times \frac{0.5mT}{bit}$$

So that

$$Bop - Brp = 2 \times sw\_hyst \times \frac{0.05mT}{bit}, \text{ or } = 2 \times sw\_op \times \frac{0.5mT}{bit}$$

`sw_tamper` – For the Si7210 if there is a strong magnetic field and the tamper threshold is exceeded, the output pin will go to the same value it would have been at if the measured field was zero. For a security application, if someone tried to "fool" the sensor by putting a strong magnet near it, the output indication would be the same as "door open" or low magnetic field indicting possible tampering.

The formula for the tamper threshold is:

$$tamper = (16 + sw\_tamper[3:0]) \times 2^{sw\_tamper[5:4]+5}$$

The tamper feature is disabled if `sw_tamper` = 63

This formula can give numbers ranging from 512 to 7936 (which is greater than the full scale of the part. Generally any setting of switch tamper(5:4) = 3 (11b) effectively disables the tamper feature as well. With switch tamper = 101111b the tamper threshold is 3968 which is 96.895 % of full scale. On the 20 mT scale a setting of 000000b (threshold = 512) gives a tamper threshold of 2.65 mT and a setting of 101111b (threshold = 3968) gives a tamper threshold of 19.84 mT. On the 200 mT scale these numbers are multiplied by 10.

Examples:

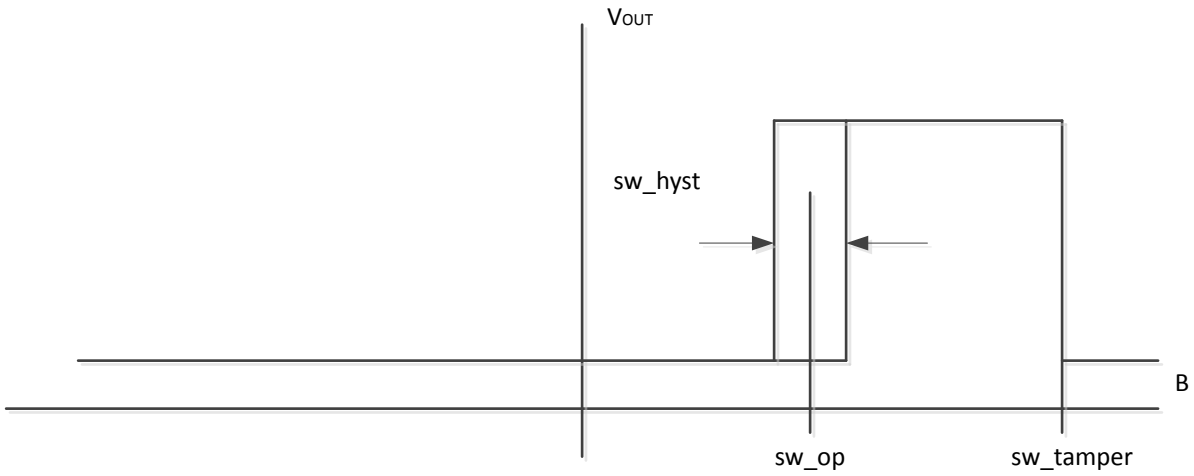


Figure 4.1. Unipolar Switch with Tamper

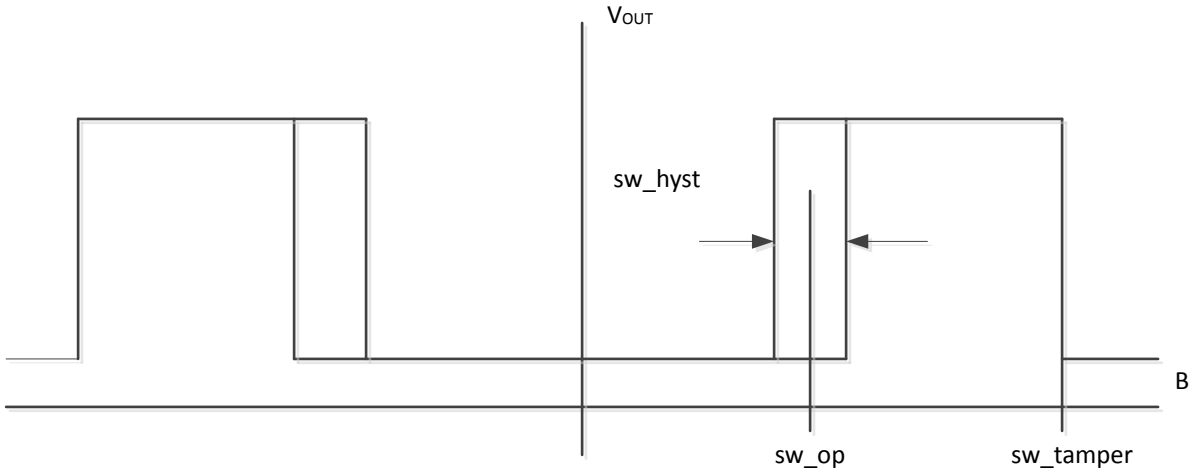


Figure 4.2. Omnipolar Switch with Tamper

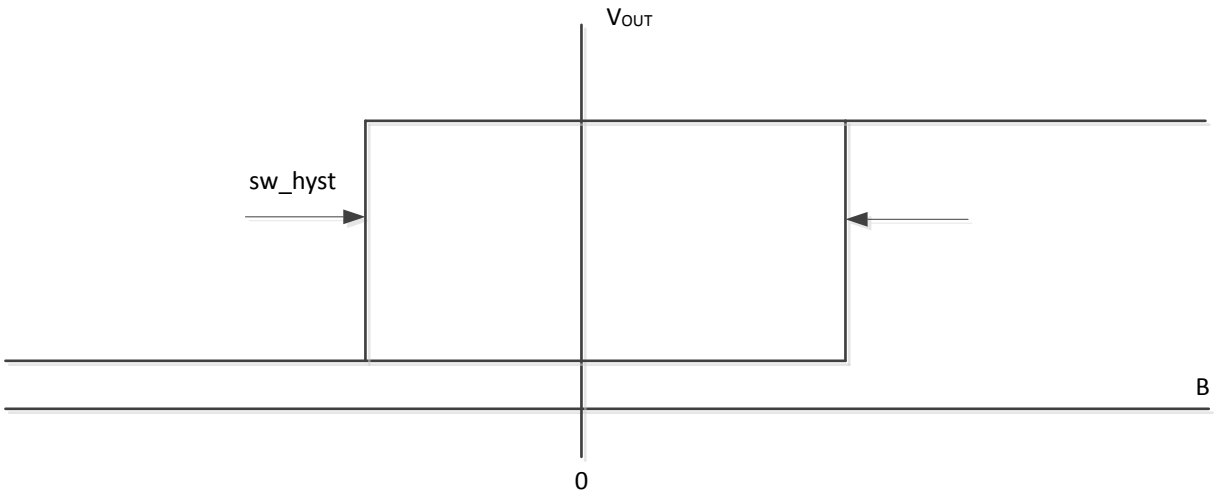


Figure 4.3. Latch

4.1.4 Registers Associated with Control of Sleep or Idle Time

`slTime` - Controls duration of sleep or IDLE interval.

Note: For the case of sleep between measurements (`slTimeena` = 1), the sleep time is not user configurable and it is recommended that this register should not be changed. The register will be reloaded every time a measurement is made when the part wakes from sleep.

The idle counter duration is

$$t_{idle} = (32 + slTime[4:0]) \times \frac{2^{8-6\times slFast+slTime[7:5]}}{10MHz}$$

For the idle counter, `SlFast` =1 and `slTime` = 0 overrides to mean actual zero idle time. The AFE runs continuously and a new sample is taken every 7 µsec.

See Figure 4.4 Idle Time on page 16 for a graphical plot of how idle time varies with the setting of `slTime`. Idle times are variable from 11 µsec to 172 msec nominally. Idle times are ±10%.

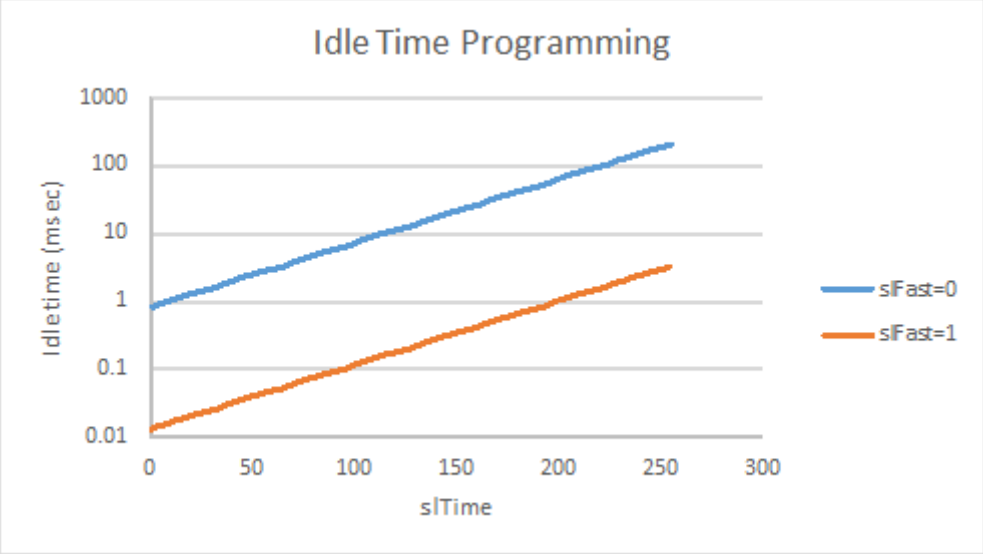


Figure 4.4. Idle Time

`slFast` - When set, causes a reduction in programmed sleep and idle times as in the above equations.

`slTimeena` – Enables the sleep timer. 0 means the part goes into complete sleep once the sleep bit is set. 1 means the parts will wake a factory set interval between 1 and 200 msec, make a measurement, set the output pin value and return to sleep.

Analog output parts should not be put to sleep between measurements as this would disable the analog output.

The sleep time is not user configurable. This is determined by the part number ordered and is factory adjustable in the range of 1 to 20 msec ±20%.

4.1.5 Registers Associated with Setting the Output Scale

`a0,a1,a2,a3,a4,a5` - These parameters are associated with the trimming of the part and setting the analog measurement range. 6 sets of these parameters are stored in OTP for the 2 standard ranges of ±20 mT and ±200 mT and the 3 standard temperature compensations as in Table 1.6 Temperature Compensation on page 6.

Parts are shipped pre-configured for a given output scale. To change the output scale, copy these 5 numbers from OTP to I2C memory. (See also section on OTP memory.)

4.1.6 Registers Associated with Adding Digital Filtering

`df_burstsize` - Rather than taking a single sample, each time the part wakes up, the Si7210 can be configured to take a burst of measurements. The time required to take one measurement is 7 µsec plus 2.3 µsec of overhead for a total of 9.3 µsec. Each additional measurement takes 7 µsec. In IIR mode, the number of measurements in a burst is $2^{\texttt{df\_burstsize}}$ so this is 1,2,4,8,… up to 128 samples. Normally, in IIR mode df_burstsize is set to 0.

`df_bw` – The number of samples to average is $2^{\texttt{df\_bw}}$. This can be 1,2,4,8,…up to 4096. In FIR mode the number of samples per burst is controlled by df_bw

In FIR mode the average is the sum of the samples divided by the number of samples.

$$output(T) = \frac{\sum_{t=T+1-2^{df\_bw}}^{T} sample(t)}{2^{df\_bw}}$$

In IIR mode, the averaging is done using:

$$output(T) = \frac{\left(2^{dfw} - 1\right)}{2^{dfw}} \times output(T-1) + \frac{1}{2^{dfw}} \times sample(T)$$

`df_iir` = 0 means the averaging is done FIR style, 1 means the averaging is done IIR style

4.1.7 Registers to Read OTP Data

The following are used for reading the OTP data:

`otp_addr` - is the address of the data to read

`otp_data` - is the data once read

`otp_read_en` - must be set to 1 to initiate a read; this bit is auto cleared

`otp_busy` – indicates the OTP is busy. For normal I2C reads, the data will be available by the time the read enable bit is set and the data is read, so in most cases this bit is not needed.

The table below is the map for OTP memory. Registers 0x04 – 0x0F correspond to the I2C registers and are loaded at power up or wake from sleep. If the bit `Usestore` is set, then the first two registers are not reloaded on a wake from sleep.

OTP BYTE	7	6	5	4	3	2	1	0
0x04	sw_low4field	sw_op						
0x05	sw_fieldpolsel		sw_hyst					
0x06	sltime							
0x08	sw_tamper						slfast	sltimeena
0x09	power up a0							
0x0A	power up a1							
0x0B	power up a2							
0x0C	df_burstsize			df_bw				df_iir
0x0D	power up a3							
0x0E	power up a4							
0x0F	power up a5							
0x14	Base part number dropping the “Si72”, for example 01 for Si7201							
0x15	Variant according to data sheet represented in hex., for example, variant 50 is 0x32							
0x16 – 0x17	Reserved							
0x18 – 0x1B	4 byte serial number							
0x1C	Reserved							
0x1D	Temperature sensor offset adjustment							
0x1E	Temperature sensor gain adjustment							
0x20	On chip field generator calibration. This is a signed integer BperVcal in the range of ±127.							
0x21 - 0x26	a0 – a5 for 20 mT scale and no magnet temperature compensation							
0x27 - 0x2C	a0 - a5 for 200 mT scale and no magnet temperature compensation							
0x2D - 0x32	a0 – a5 for 20 mT scale at 25°C -0.12%/°C magnet temperature compensation (Neodymium)							
0x33 - 0x38	a0 – a5 for 200 mT scale at 25°C -0.12%/°C magnet temperature compensation (Neodymium)							
0x39 - 0x3E	a0 – a5 for 20 mT scale at 25°C -0.2%/°C magnet temperature compensation (Ceramic)							
0x3F - 0x44	a0 – a5 for 200 mT scale at 25°C -0.2%/°C magnet temperature compensation (Ceramic)							

4.1.8 Control of On-Chip Test Coil

`tm_fg` - Test Field Generator Coil

tm_fg	Current in coil
00b	None
01b	Positive direction
10b	Negative direction
11b	None

Avoid transitions between states 1 & 2, due to a possible short term high current spike.

The nominal magnetic field output of the on chip generator varies with coil current. The coil current varies with coil resistance and power supply voltage, so the nominal magnetic field output varies according to

$$Bout = BperVnom \times \left(1 + \frac{BperVcal}{256}\right) \times V_{DD}$$

BperVnom is [TBD in the range of 20 mT]

This can be used to calculate the expected magnetic field from the test coil for a given V_{DD}. This is somewhat temperature dependent so the actual measured field will vary according to the accuracy of the part as well as temperature. Generally, as the coil is turned on and off the measured variation in field should be within ±25% of expectation based on the calculated field generation.

5. Making Temperature Measurements

Every magnetic field conversion has an associated temperature measurement. During magnetic field measurement cycles, this data is used for compensating the hall sensor data to keep the desired temperature coefficient of magnetic field measurement.

The temperature data is available by setting the `dspsigsel` field of register 0xC3 to 0x01.

Once the `dspsigsel` field is set, the temperature sensor data is read from registers 0xC1 and 0xC2 as 15b unsigned number (see also 4.1.2 Fields Associated with Reading DATA).

The temperature sensor data can be read after one conversion or after a burst of conversions.

Note: The temperature sensor data is not averaged after performing a burst. Only the magnetic field data is averaged.

The data in 0xc1 and 0xc2 is combined into a 12 bit signed number:

$$value = 32 \times Dspigm[6:0] + (Dspisigl[7:0] >> 3)$$

$$Temperature\_raw = -2.1 \times 10^{-6} value^2 + 0.1522 \times value - 273$$

The data read in this way does not have offset and gain correction applied. The offset and gain correction is stored in registers 0x1D and 0x1E which are read as signed integers.

$$Offset = \frac{signed\_value(0x1D)}{16}$$

$$Gain = 1 + \frac{signed\_value(0x1E)}{2048}$$

And finally

$$Temperature = gain \times (Temperature\_raw) + offset$$

Typically, the gain and offset terms are calculated only once and then are saved. The temperature measurement circuit has noise and quantization errors of approximately ±0.3°C. Adding averaging to the calculated temperature will reduce these errors.

6. Pin Description

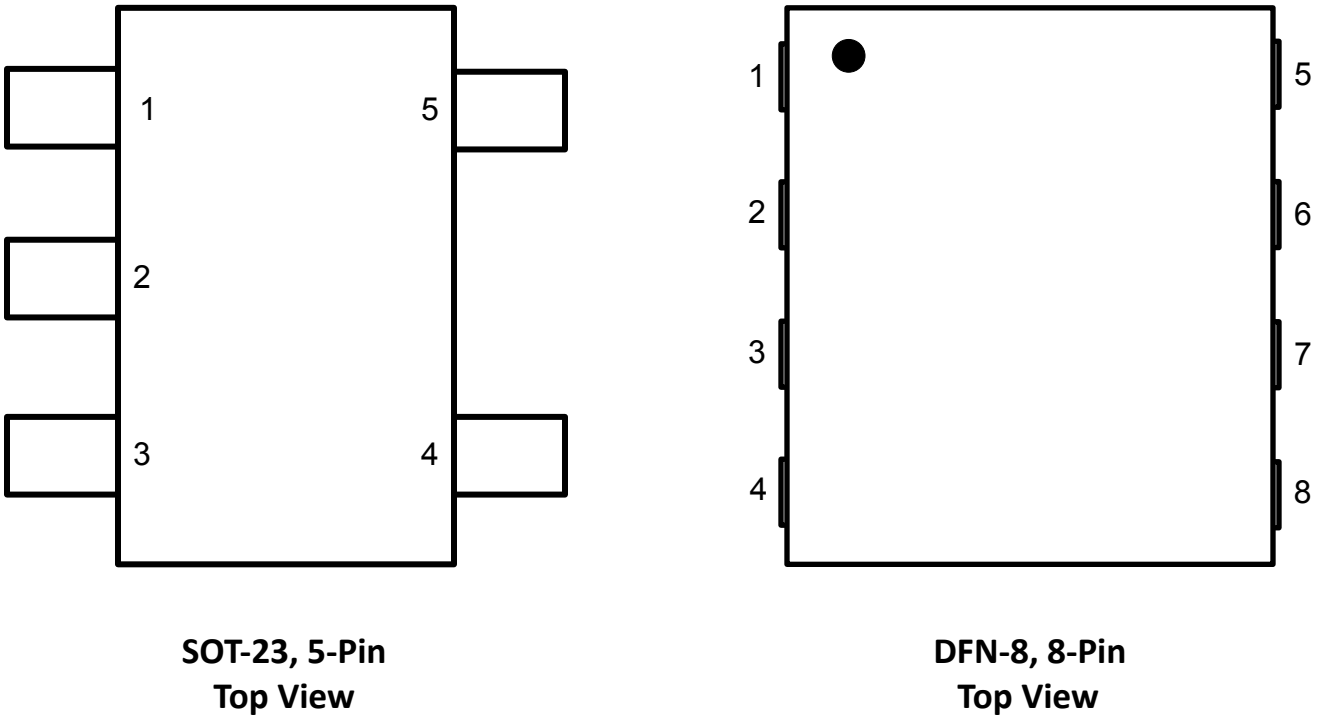


Figure 6.1. Pin Assignments

Table 6.1. Five-Pin

Pin name	Pin number	Description
SDA	1	I²C data
GND	2	Ground
SCL	3	I²C clock
V_{DD}	4	Power +1.7 to +5.5 V
ALERT/VOUT	5	Analog or digital ouput

Table 6.2. Eight-Pin

Pin name	Pin number	Description
GND	1, 5	Ground
SCL	2	I²C SCL
NC	3, 7	Not connected
SDA	4	I²C SDA
OUT	6	OUTPUT pin

7. Ordering Guide

Part Number	Deafault Output Polarity (high field)	IDD (typ. @3.3V)	Default BOP, BRP	Sleep/ Idle Time	Temper-ature Com-pensa-tion	Temper-ature accura-cy	Tamper Thresh-old	Digital Filtering	I2C Ad-dress	VDD	Pack-age	Temper-ature Rating
Si7210-B-00-IV(R)	High (push-pull)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) | BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±1.0 °C	19.84 mT	None	0x30	1.7 - 5.5 V	SOT23-5	-40°C - 125°C
Si7210-B-01-IV(R)	Low (open drain)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) | BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±1.0 °C	19.84 mT	None	0x30	1.7 - 5.5 V	SOT23-5	-40°C - 125°C
Si7210-B-02-IV(R)	Low (push-pull)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) | BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±4.0 °C	19.84 mT	None	0x31	1.7 - 5.5 V	SOT23-5	-40°C - 125°C
Si7210-B-03-IV(R)	Low (push-pull)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) | BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±4.0 °C	None	None	0x32	1.7 - 5.5 V	SOT23-5	-40°C - 125°C
Si7210-B-04-IV(R)	Low (push-pull)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) | BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±4.0 °C	None	None	0x33	1.7 - 5.5 V		

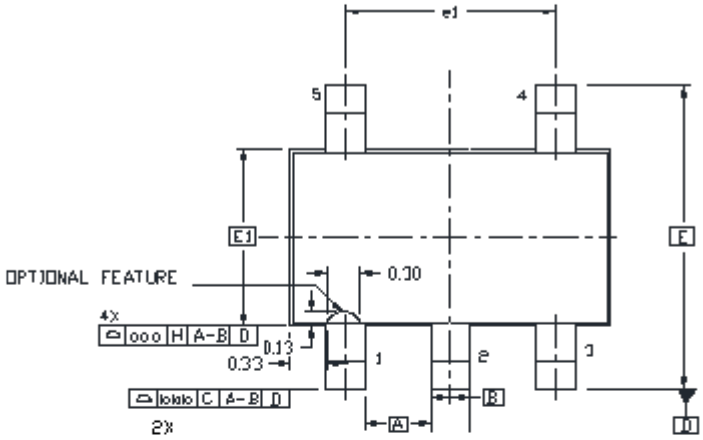
Part Number	Deafault Output Polarity (high field)	IDD (typ. @3.3V)	Default BOP, BRP	Sleep/ Idle Time	Temper-ature Com-pensa-tion	Temper-ature accura-cy	Tamper Thresh-old	Digital Filtering	I2C Ad-dress	VDD	Pack-age	Temper-ature Rating
Si7210-B-05-IV(R)	Low (push-pull)	0.4 µA	BOP = ±2.15 mT (max) BRP = ±0.35 mT (min) | BOP - BRP| = 0.8 mT (typ)	200 msec (sleep)	None	±4.0 °C	None	None	0x33	1.7 - 5.5 V	SOT23-5	-40°C - 125°C

Note:

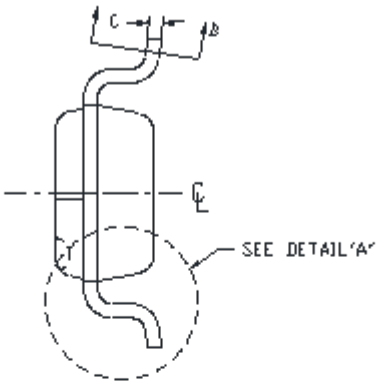
1. All I2C parts have the base part number Si7210. A is the die revision. The next two digits are used with this look up table to give more specific information. E is the temperature range (-40 to +150°C). M or V is the package type (DFN or SOT23) the optional (R) is the designator for tape and reel (xx pieces per reel). Parts not ordered by the full reel will be supplied in cut tape.
2. North pole of a magnet at the bottom of a SOT23 package is defined as positive field.

8. Package Outline

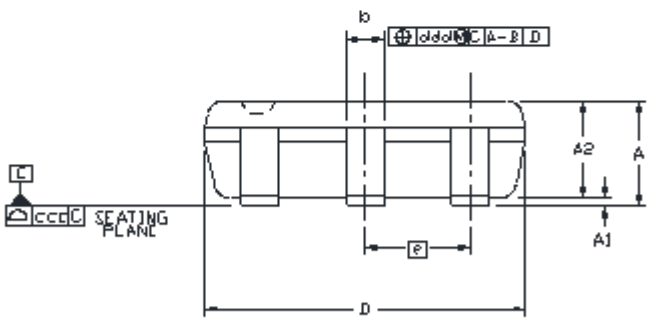
8.1 SOT23 3-Pin Package



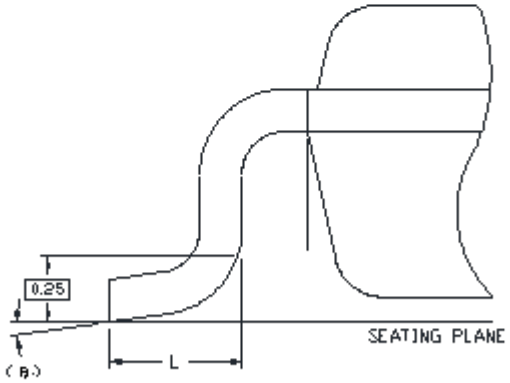
TOP VIEW
6 LEAD



END VIEW



SIDE VIEW
6 LEAD



DETAIL "A"

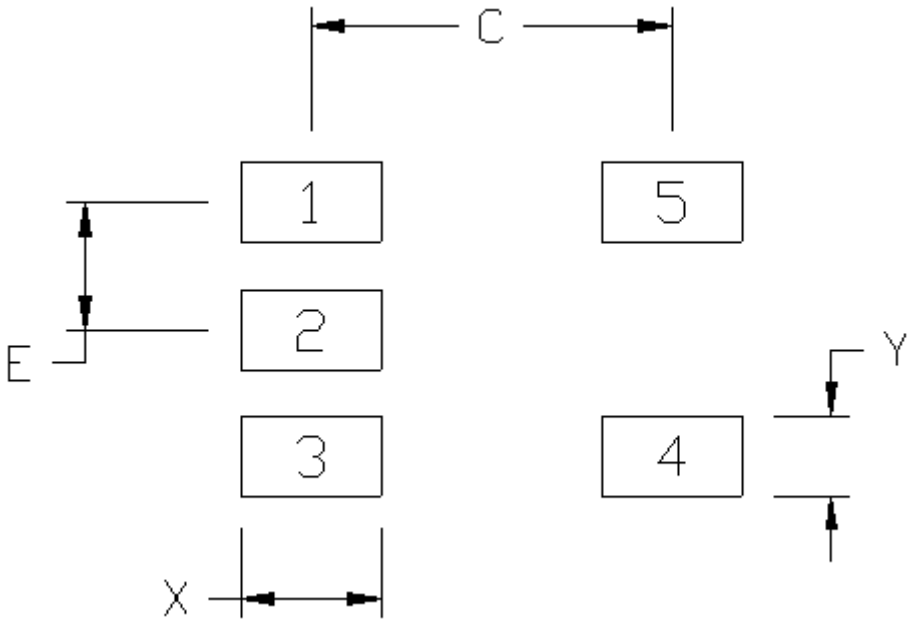
Dimension	MIN	MAX
A	--	1.25
A1	0.00	0.10
A2	0.85	1.15
b	0.30	0.50
c	0.10	0.20
D	2.90 BSC	
E	2.80 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L2	0.25 BSC	
θ	0°	8°
aaa	0.15	
bbb	0.15	
ccc	0.10	
ddd	0.20	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-193, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

9. Land Patterns

9.1 SOT23 Five-Pin PCB Land Pattern



Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

Note:

General

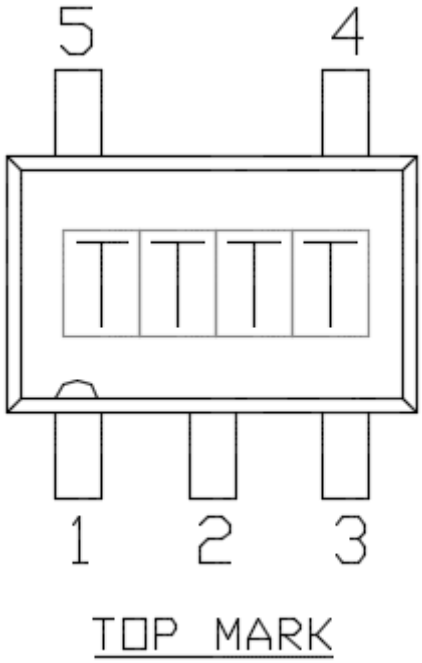
1. 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

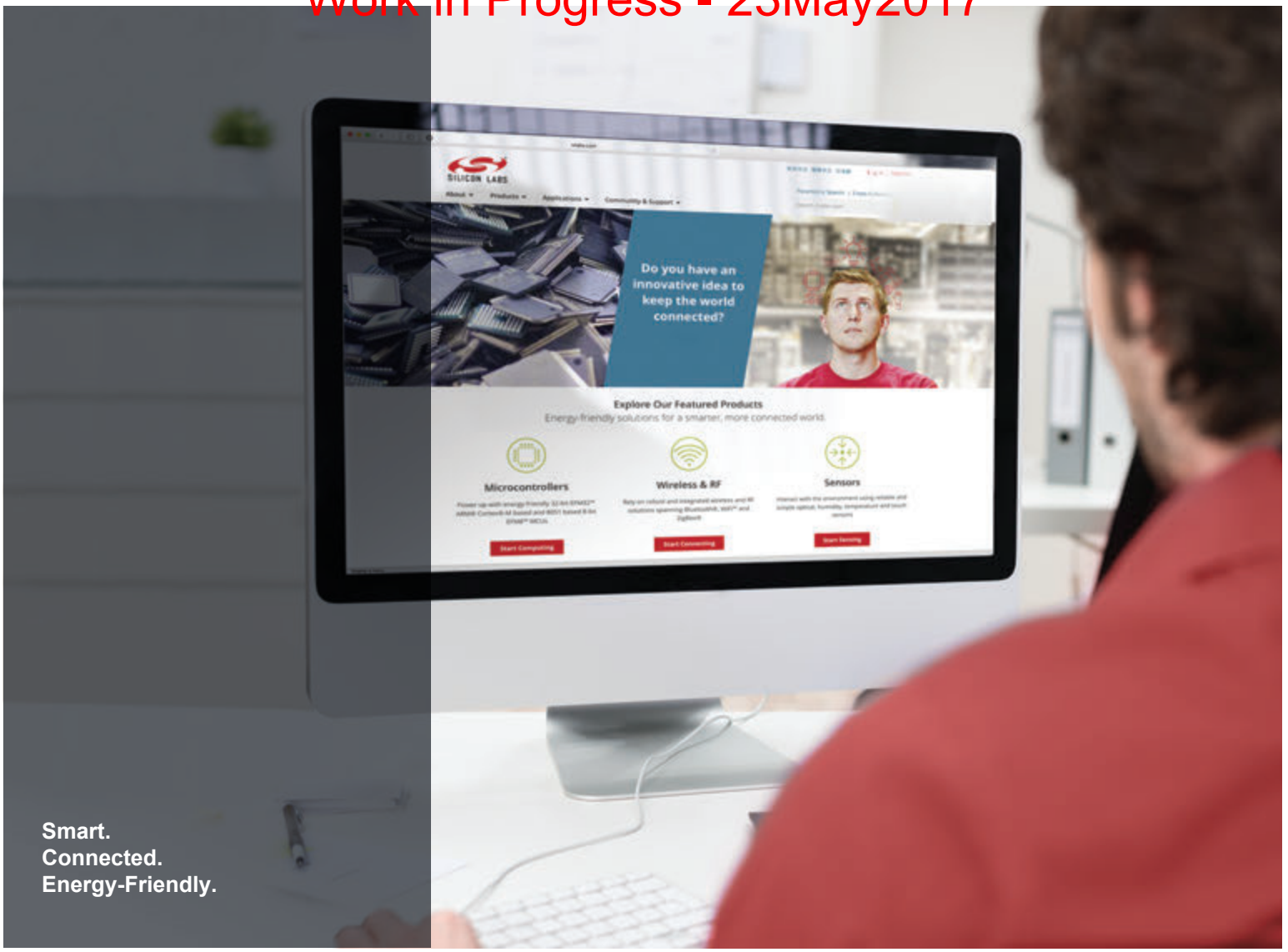
Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

10. Top Marking

10.1 SOT23 5-Pin Topmarking





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