swissbit®

Product Data Sheet

Industrial microSDHC / SDXC Memory Card

S-45u Series

UHS-I Interface, MLC

Extended and Industrial Temperature Grade

durabit™

"the better MLC"

Date: April 29, 2021
Revision: 1.34

Made in Germany

Contents

S-45u Series – Industrial microSDHC / SDXC Memory Card 4 GBytes up to 128 GBytes

1. Product Summary

- **Capacities:** 4 GBytes, 8 GBytes, 16 GBytes, 32 GBytes, 64 GBytes, 128 GBytes
- **Form Factor:** Standard microSD Memory card form factor – 15.0mm x 11.0mm x 0.7mm (1.0mm)
- **Compliance[1]:** Fully compliant with SD Memory Card specification 2.0 and 3.0 and MICRO SD Memory Card Addendum 4.00
  - SDHC/SDXC default/high speed mode and UHS supported
  - Up to speed class 10 and U1 and according SD3.0 specification
  - FAT32 / exFAT preformatted
- **Performance:**
  - SD Default speed
  - SD High speed
  - SD UHS-I
  - Read Performance: Sequential Read up to 44 MBytes/s, Random Read IOPS up to 1,349
  - Write Performance: Sequential Write up to 22 MBytes/s, Random Write IOPS up to 966
- **Operating Temperature Range[2]:**
  - Extended: -25 °C to 85 °C
  - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:**
  - Extended: -25 °C to 100 °C
  - Industrial: -40 °C to 100 °C
- **Operating Voltage:** 2.7...3.6V normal operating voltage (Low-power CMOS technology)
- **Data Retention:** 10 Years @ Life Begin / 1 Year @ Life End
- **Humidity:** 85% RH @85°C 1000h
- **Electromagnetic Compatibility Test:** Radiated Emission; Radiated Immunity; Electrostatic Discharge

[1] The verification of host system and storage device compatibility is in customer's responsibility. Swissbit can provide guidance and support on request.

[2] High Temperature storage without operation reduces the data retention, in operation the data will be refreshed, if data error issues were detected

2. Product Features

- Optimized FW algorithms especially for high read access and long data retention applications
  - Patented power-off reliability technology
  - Wear Leveling technology
  - Write Endurance technology
  - Read Disturb Management
  - Data Care Management
  - Near miss ECC technology
  - Diagnostic features with Life Time Monitoring tool support
- High reliability
  - Designed for industrial market especially read intensive application like navigation, infotainment, POS/POI, medical and general boot medium use case
  - The product is optimized for long life cycle and provides excellent data retention in high temperature mission profiles.
  - Number of card insertions/removals 20,000
  - SIP (System In Package) process for extreme dust, water and ESD proof
  - Selected AEC-Q100 qualification
- Manufactured in a TS 16949 certified factory
- Controlled BOM & PCN process
- Customized options like CID registers, CPRM keys, firmware incl. settings and marking by projects
- In-Field Firmware Update[3]
- Swissbit Life Time Monitoring (SBLTM) Tool and SDK for SBLTM (on request)

[3] The support of In-Field FW update capabilities on host systems is recommended.

3. Ordering Information

Table 1: Standard Product List

Capacity	Temperature	
	Extended	Industrial
	Part Number	Part Number
4 GBytes	SFSD4096NxBM1ff-E-xx-2y1-STD	SFSD4096NxBM1ff-I-xx-2y1-STD
8 GBytes	SFSD8192NxBM1ff-E-xx-2y1-STD	SFSD8192NxBM1ff-I-xx-2y1-STD
16 GBytes	SFSD016GNxBM1ff-E-xx-2y1-STD	SFSD016GNxBM1ff-I-xx-2y1-STD
32 GBytes	SFSD032GNxBM1ff-E-xx-2y1-STD	SFSD032GNxBM1ff-I-xx-2y1-STD
64 GBytes	SFSD064GNxBM1ff-E-xx-2y1-STD	SFSD064GNxBM1ff-I-xx-2y1-STD
128 GBytes	SFSD128GNxBM1ff-E-xx-2y1-STD	SFSD128GNxBM1ff-I-xx-2y1-STD

x = product generation/configuration, ff = NAND flash and y = firmware revision

Table 2: Available Part Numbers, MLC NAND Flash 15nm (FW B)

Capacity	Temperature	
	Extended	Industrial
	Part Number	Part Number
4 GBytes	SFSD4096N3BM1T0-E-GE-2B1-STD	SFSD4096N3BM1T0-I-GE-2B1-STD
8 GBytes	SFSD8192N3BM1T0-E-GE-2B1-STD	SFSD8192N3BM1T0-I-GE-2B1-STD
16 GBytes	SFSD016GN3BM1T0-E-LF-2B1-STD	SFSD016GN3BM1T0-I-LF-2B1-STD
32 GBytes	SFSD032GN3BM1T0-E-HG-2B1-STD	SFSD032GN3BM1T0-I-HG-2B1-STD

Table 3: Available Part Numbers, MLC NAND Flash 15nm (FW D)

Capacity	Temperature	
	Extended	Industrial
	Part Number	Part Number
4 GBytes	SFSD4096N3BM1T0-E-GE-2D1-STD	SFSD4096N3BM1T0-I-GE-2D1-STD
8 GBytes	SFSD8192N3BM1T0-E-GE-2D1-STD	SFSD8192N3BM1T0-I-GE-2D1-STD
16 GBytes	SFSD016GN3BM1T0-E-LF-2D1-STD	SFSD016GN3BM1T0-I-LF-2D1-STD
32 GBytes	SFSD032GN3BM1T0-E-HG-2D1-STD	SFSD032GN3BM1T0-I-HG-2D1-STD

Table 4: Available Part Numbers, 3D NAND Flash (FW E)

Capacity	Temperature	
	Extended	Industrial
	Part Number	Part Number
16 GBytes	SFSD016GN4BM1MT-E-1E-2E1-STD	SFSD016GN4BM1MT-I-1E-2E1-STD
32 GBytes	SFSD032GN4BM1MT-E-2F-2E1-STD	SFSD032GN4BM1MT-I-2F-2E1-STD
64 GBytes	SFSD064GN4BM1MT-E-3F-2E1-STD	SFSD064GN4BM1MT-I-3F-2E1-STD
128 GBytes	SFSD128GN4BM1MT-E-4G-2E1-STD	SFSD128GN4BM1MT-I-4G-2E1-STD

4. Product Description

The microSD Memory Card is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The card operates in two basic modes:

- SDHC/SDXC and UHS-I card modes
- SPI mode

The micro SD Memory Card also supports SD Default and High Speed mode with up to 50MHz clock frequency as well as UHS-I modes DDR50, SDR12/25/50 with up to 100MHz clock frequency.
The cards are compliant with

- SD Memory Card Specification Part 1, Physical layer Specification V3.01
- SD Memory card Specification Part 2, File System Specification V3.00
- SD Memory card Specification Part 3, Security Specification V3.00
- MICRO SD Memory Card Addendum V4.00

The Card has an internal intelligent controller, which manages interface protocols, data storage and retrieval as well as hardware BCH Error Correction Code (ECC), defect handling, diagnostics and clock control.
The advanced wear leveling mechanism assures an equal usage of the Flash memory cells to extend the lifetime. The hardware BCH-code ECC allows to detect and correct up to 40 defect bits per 1kByte.
The controller performs control read operations and checks the consistence of the data. If an error of some bits is detected, the card refreshes all data in the flash cells to prevent data retention problems.

The card has a power-loss management feature to prevent data corruption after power-down.
The cards are RoHS compliant and lead-free.

Related Documentation

- Simplified specifications are available at (https://www.sdcard.org/)

4.1 Performance Specification

Table 5: Read/Write Performance FW B

Capacity[4]	Sequential Read (MB/s)	Sequential Write (MB/s)	Random Read 4k (IOPS)	Random Write 4k (IOPS)
4 GBytes	31	15	642	689
8 GBytes	32	14	698	671
16 GBytes	33	14	734	688
32 GBytes	33	13	729	679

Table 6: Read/Write Performance FW D

Capacity[4]	Sequential Read (MB/s)	Sequential Write (MB/s)	Random Read 4k (IOPS)	Random Write 4k (IOPS)
4 GBytes	39	14	1,183	942
8 GBytes	38	21	1,170	871
16 GBytes	39	22	1,225	908
32 GBytes	40	22	1,216	964

Table 7: Read/Write Performance FW E

Capacity[4]	Sequential Read (MB/s)	Sequential Write (MB/s)	Random Read 4k (IOPS)	Random Write 4k (IOPS)
16 GBytes	42	19	1,312	963
32 GBytes	41	19	1,349	966
64 GBytes	41	19	1,289	946
128 GBytes	44	19	1,310	943

4.2 Environmental Specifications

4.2.1 Recommended operating conditions

Table 8: Recommended Operating Conditions

Parameter	Value
Extended Operating Temperature	-25 °C to 85 °C
Industrial Operating Temperature	-40 °C to 85 °C

4.2.2 Recommended Storage Conditions

Table 9: Recommended Storage Conditions[5]

Parameter	Value
Extended Operating Temperature	-25 °C to 100 °C
Industrial Storage Temperature	-40 °C to 100 °C

[4] Performance measured with USB-SD Memory Card reader with Crystal Disk Mark test tool.

[5] High Temperature storage without operation reduces the data retention, in operation the data will be refreshed, if data error issues were detected

4.2.3 Humidity & EMC

Table 10: Humidity and EMC

Parameter	Value
Humidity (non-condensing)	85% RH @85°C 1000h
ESD	up to ±4 kV (contact discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, on each contact pad, non-operating up to ±15 kV, (air discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, isolated contact pad area, non-operating

4.2.4 Environmental conditions

Table 11: Environmental conditions

Parameter	Value
UV light exposure	UV: 254nm, 15Ws/cm2 according to ISO7816-1
X-Ray	0.1 Gy 70keV to 140KeV (ISO7816-1) according SDA
Durability	20,000 mating cycles
Drop Test	1.5m free fall
Bending / Torque	10N / 0.15Nm ±2.5° max
Mechanical Shock	1500G, 0.5ms, half sine wave ±xyz-axis, 4 pulses each non-operating, JESD22B110 Condition B
Vibration	50G, p-p, 20..2000Hz, sweep xyz-axis, 4 pulses each, non-operating, MIL-STD-883 M2007.3 Condition B

4.3 Regulatory Compliance

The S-45u devices comply with the regulations / standards listed in Table 12.

Table 12: Regulatory Compliance

Abbreviation	Regulation/ Standard
EMC	(EU) 2014/30 (FCC) 47 CFR Part 15
RoHS	(EU) 2011/65/EU with 2015/863 and 2017/2102
REACh	(EU) 1907/2006 and 207/2011
WEEE	(EU) 2012/19

4.4 Mechanical Specifications

Physical dimensions are detailed in the following Table 13.
Figure 1 illustrates the S-45u dimensions.

Table 13: Physical dimensions

Physical Dimensions		Unit
Length	15.0±0.1	mm
Width	11.0±0.1	
Thickness (Max)	0.7 (1.)±0.1	
Weight (Max Capacity)	0.4	g

4.5 Reliability and Endurance

Data reliability with effective error tolerance and data retention at the beginning and end of life is provided in the table below.

Table 14: Reliability

Parameter	Value[6]
Data Retention at beginning @ 40°C	10 years
Data Retention at life end (2k-3k PE cycles) @ 40°C	1 year

4.6 Geometry Specification

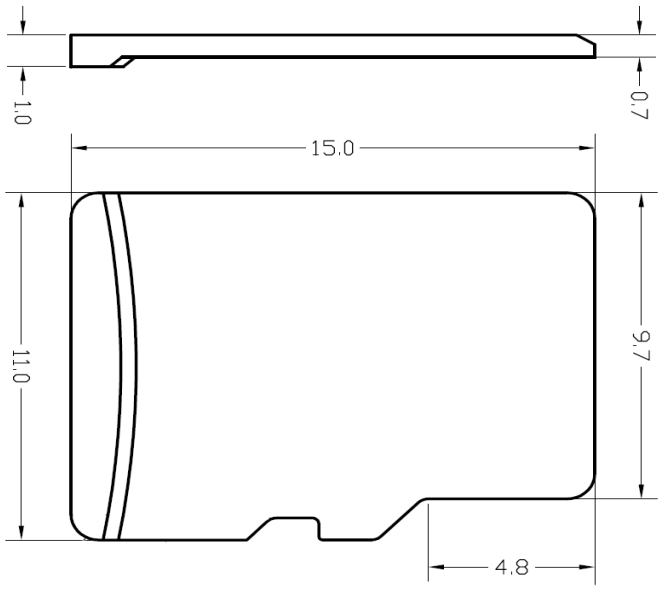
Table 15: Drive Geometry

Raw Capacity	Total LBA	User Addressable Bytes
	Decimal	(Unformatted)
4 GBytes	7,774,208	3,980,394,496
8 GBytes	15,802,368	8,090,812,416
16 GBytes	31,834,112	16,299,065,344
32 GBytes	62,333,952	31,914,983,424
64 GBytes	124,735,488	63,864,569,856
128 GBytes	250,609,664	128,312,147,968

5. Package Mechanical

NOTE: The microSD Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s).

Figure 1: Simplified mechanical dimensions



The dimensions and tolerances are according to the SD specification.

[6] After every power on the card reads the whole flash and performs a data refresh if necessary. Therefore, the data retention can be much longer in most use cases.

6. Electrical Interface

Figure 2: microSD memory Card shape and interface (bottom view)

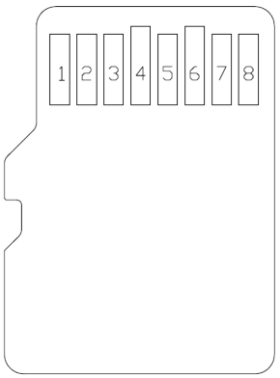


Table 16: Pin Assignment, Name and Description – SD Mode

Pin	Signal Name	Type[7]	Description
1	DAT2[8]	I/O/PP	Data Line [Bit 2]
2	CD/DAT3[9]	I/O/PP[10]	Card Detect/ Data Line [Bit 3]
3	CMD	PP	Command/Response
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]
8	DAT1[11]	I/O/PP	Data Line [Bit 1]

Table 17: Pin Assignment, Name and Description – SPI Mode

Pin	Signal Name	Type[7]	Description
1	RSV		
2	CS	I[10]	Chip Select (neg true)
3	DI	I	Data In
4	VDD	S	Supply voltage
5	SCLK	I	Clock
6	VSS	S	Supply voltage ground
7	DO	O/PP	Data Out
8	RSV		

[7] S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers
[8] DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).
[9] The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
[10] At power up this line has a 50k0hm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. The host should disconnect this pull-up during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.
[11] DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).

6.1 Power up / Power down behavior and reset

6.1.1 Power up

When the voltage is ramped up the controller is ready (internal reset pin released) if the voltage reaches 1.65V. The host can start with communication 1ms after 2.7V is reached according the SDA specification.
That should perform 74 clock cycles and start with the sequence CMD0, CMD8, ACMD41 until card is ready as described in the SD specification 3.01.

6.1.2 Power down

When the power falls below 2.6V the controller stops the communication to the flash, but enables the flash to finish a started flash program operation (if voltage drop is not fast).

When the host shuts down the power, the card VDD shall be lowered to less than 0.1 V for a minimum period of 1 ms before the card is powered on again.

After next initialization the controller checks the last written data for consistency and refreshes the data. Either the new or the old data (if the write operation could not be finished) are available.

6.1.3 Power drop

If the voltage drops below 2.6V and rises again, the card preforms a reset. The card must be initialized like after a power on.

6.1.4 Operation below minimum voltage

If the card initialization is performed below the specified voltage of 2.7V, the card may be detected as 1MB card with no useful data. In this case the host should power off and on the card and start initialization above 2.7V.

6.2 DC characteristics

Table 18: DC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{DD}	Operating Current Read		75	80	mA	@ 25°C
	Operating Current Write		70	80	mA	@ 25°C
	Background read and refresh[12]		70	80	mA	@ 25°C
	Pre-initialization Standby Current		5	15	mA	@ 25°C
	Post-initialization Standby Current[13]		2	9	mA	@ 25°C
			5	15	mA	@ 25°C
I_{LI}	Input Leakage Current	-2		2	µA	without pull up R
I_{LO}	Output Leakage Current	-2		2		

Table 19: microSD Memory Card recommended operation conditions

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Supply Voltage	Normal Operating Status	2.7	3.3	3.6	V
-	Power Up Time (from 0V to V_{DD} min)				250	Ms

6.3 Signal loading

According to SD specification

[12] The card can perform auto data read of the whole card to check for ECC errors and performs data refresh

[13] Before auto read the idle current is larger than the typical idle current after auto read

6.4 AC characteristics

6.4.1 Default speed mode (0-25MHz)

According to SD specification

6.4.2 High speed mode (0-50MHz)

According to SD specification

6.4.3 UHS modes

UHS modes were driven with a signal level of 1.8V.
The cards support following UHS-I modes:

Table 20: Supported UHS-I modes

Host request	Card Modes (to select by host)	max. Burst MB/s
SDR12	SDR12	up to 12.5
SDR25	SDR12, SDR25	up to 25
SDR50	SDR12, SDR25, SDR50	up to 50
DDR50	SDR12, SDR25, SDR50, DDR50	up to 50

7. Host access specification

The following chapters summarize how the host accesses the card.

7.1 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

7.1.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.
Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

7.2 SPI Bus Mode Protocol

The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.
While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.
The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.
The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The bidirectional CMD and DAT lines are replaced by unidirectional dataIn and dataOut signals.

Table 21: SPI Bus signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

7.2.1 Mode Selection

The microSD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in idle_state. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode.
If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.
The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available.
During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is Multimedia Card. In that case it should restart the card as Multimedia Card using CMD0 and CMD1.

7.3 Card registers

The microSD Memory Card has the following registers.

Table 22: microSD Memory Card registers

Register name	Bit width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA[14]	16	Relative Card Address	This register carries the card address is SD Card mode.
SSR	512	SD Status	information about the card proprietary features and vendor specific life time information

[14] RCA register is not available in SPI mode

Table 23: CID register

Register name	Bit width	Description	Typ. value
MID	8	Manufacture ID	0x5d
OID	16	OEM/Application ID	0x5342
PNM	40	Product Name	e.g."0008G"
PRV	8	Product Revision	oxgg
PSN	32	Product Serial Number	xxxxxxxx
–	4	Reserved	0x0
MDT	12	Manufacture Date	oxyym
CRC	7	Check sum of CID contents	chksum
–	1	Not used; always=1	1

Table 24: OCR register

OCR bit positon	VDD voltage windows	Typ. value	OCR bit position	VDD voltage window	Typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24	Switching to 1.8V accepted	1
13	2.5-2.6	0	25-29	Reserved	
14	2.6-2.7	0	30	Card Capacity Status (CCS)	*[15]
			31	0=busy; 1=ready	*[16]

[15] This bit is valid only when the card power up status bit is set

[16] This bit is set to LOW if the card has not finished the power up routine

Table 25: CSD register

Register name	Bits	Bit width	Description	Typ. value
CSD_STRUCTURE	127:126	2	CSD structure	01
–	125:120	6	Reserved	00000
TAAC	119:112	8	Data read access time 1	00001110
NSAC	111:104	8	Data read access time 2 (CLK cycle)	00000000
TRAN_SPEED	103:96	8	Data transfer rate	00110010 Default speed 00001011 SDR 50 or other values
CCC	95:84	12	Card command classes	010110110101
READ_BL_LEN	83:80	4	Read data block length	1001
READ_BL_PARTIAL	79	1	Partial blocks for read allowed	0
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0
READ_BLK_MISALIGN	77	1	Read block misalignment	0
DSR_IMP	76	1	DSR implemented	0
–	75:70	6	Reserved	000000
C_SIZE	69:48	22	Device size	xxx[17]
–	47	1	Reserved	0
ERASE_BLK_EN	46	1	Erase single block enable	1
SECTOR_SIZE	45:39	7	Erase sector size	1111111
WP_GRP_SIZE	38:32	7	Write protect group size	0000000
WP_GRP_ENABLE	31	1	Write protect group enable	0
–	30:29	2	Reserved	00
R2W_FACTOR	28:26	3	Write speed factor	010
WRITE_BL_LEN	25:22	4	Write data block length	1001[17]
WRITE_BL_PARTIAL	21	1	Partial blocks for write allowed	0
–	20:16	5	Reserved	00000
FILE_FORMAT_GRP	15	1	File format group	0 W(1)
COPY	14	1	Copy flag	0 W(1)
PERM_WRITE_PROTECT	13	1	Permanent write protection	0 W(1)
TMP_WRITE_PROTECT	12	1	Temporary write protection	0 W
FILE_FORMAT	11:10	2	File format	00 W(1)
–	9:8	2	Reserved	00 W
CRC	7:1	7	Checksum of CSD contents	xxxxxxx W
–	0	1	Always=1	1

Memory capacity = (C_SIZE+1) * 512kByte

W value can be changed with CMD27 (PROGRAM_CSD)
W(1) value can be changed ONCE with CMD27 (PROGRAM_CSD)

[17] Drive size and block sizes vary with card capacity

Table 26: SCR register

Field	Bits	Bit width	Typ. value	Remark
SCR_STRUCTURE	63:60	4	0000	SCR 1.01...2.00
SD_SPEC	59:56	4	0010	SD 2.0 or 3.0
DATA_STAT_AFTER_ERASE	55	1	1	data are 0xFF after erase
SD_SECURITY	54:52	3	011 100	2.00 (SDHC) 3.xx (SDXC)
SD_BUS_WIDTHS	51:48	4	0101	1 or 4 bit
SD_SPEC3	47	1	1	yes→ SD3.0
EX_SECURITY	46:43	4	0000	no extended security
Reserved	42:34	9	0	0
CMD_SUPPORT	33:32	2	11	CMD23 and CMD20 supported
Reserved	31:0	32	0	0

Table 27: RCA register

Field	Bit width	Typ. value
RCA	16	0x0000[18]

Table 28: SSR register

Field	Bits	Bit width	Typ. value	Remark
Data bus width	511:510	2	0x2[19]	4 bit width
Secured mode	509:509	1	0x0	not secured
Reserved for security	508:502	7	0x00	-
Reserved	501:496	6	0x00	-
SD card type	495:480	16	0x0000	Regular SD
Size protected area	479:448	32	0x03000000 0x04000000 ...	48MB 64MB ...
Speed class	447:440	8	0x04	Class 10
Move performance	439:432	8	0x05	5 MB/s
Allocation unit size	431:428	4	0x9	4 MB
Reserved	427:424	4	0x0	
Erase unit size	423:408	16	0x0001	1 AU
Erase unit timeout	407:402	6	0x01	1 second
Erase unit offset	401:400	2	0x1	1 second
UHS mode Speed Grade	399:396	4	0x1	UHS Grade1
Allocation unit size in UHS mode	395:392	4	0x9	4 MB
Reserved	391:312	80		
Data structure version identifier, currently 1	311:304	8	0x01	version 1
Number of manufacturer marked defect blocks	303:288	16	0x0008	8 initial BB
Number of initial spare blocks (worst chip)	287:272	16	0x0074	116 spare blocks

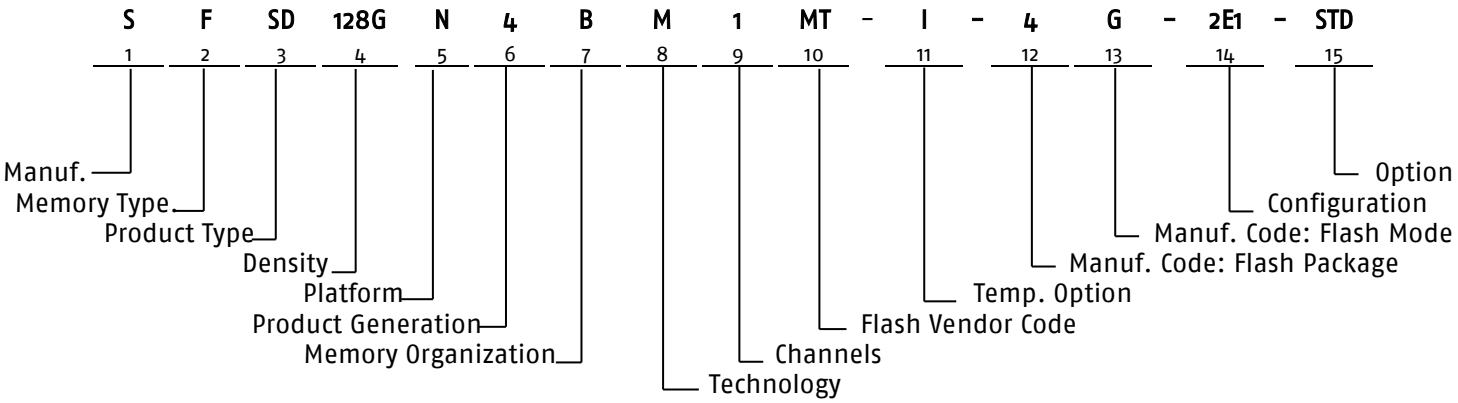
[18] After initialization the host can change the RCA register

[19] Value changes in operation

Number of initial spare blocks (sum over all chips)	271:256	16	0x0074	116 spare blocks
Percentage of remaining spare blocks (worst chip)	255:248	8	0x64[19]	100%
Percentage of remaining spare blocks (all chips)	247:240	8	0x64[19]	100%
Number of uncorrectable ECC errors (not including ECC errors during startup)	239:224	16	0x0000[19]	0 uncorrectable errors
Number of correctable ECC errors (not including ECC errors during startup)	223:192	32	0x0045074b[19]	4523851 correctable ECC errors
Lowest wear level class	191:176	16	0x0000[19]	0
Highest wear level class	175:160	16	0x0000[19]	0
Wear level threshold	159:144	16	0x003f	63 block erases per WL class
Total number of block erases	143:96	48	0x00...1ff0[19]	8176 block erase commands
Number of flash blocks, in units of 256 blocks	95:80	16	0x0008	2048 flash blocks
Maximum flash block erase count target, in wear level class units	79:64	16	0x00xx	Flash endurance xx WL classes
Power on count	63:32	32	0x00000003[19]	3x power on
Firmware version	31:0	32	0xYYMMDDXX	Firmware version

Bit 311:0 are vendor specific, example values in the table

8. Part Number Decoder



8.1 Manufacturer

Swissbit code	S

8.2 Memory Type

Flash	F

8.3 Product Type

SATA Interface	SD

8.4 Density

4 GBytes	4096
8 GBytes	8192
16 GBytes	016G
32 GBytes	032G
64 GBytes	064G
128G GBytes	128G

8.5 Platform

microSD Memory Card	N

8.6 Product Generation

8.7 Memory Organization

x8	B

8.8 Technology

S-45u Series	M

8.9 Channels

1 Flash channel	1

8.10 Flash Code

Toshiba / Kioxia	T0
Micron	MT

8.11 Temperature Option

Extended Temperature Range: -25 °C to 85°C	E
Industrial Temperature Range: -40 °C to 85 °C	I

8.12 Die Classification

MLC MONO (single die package)	G
MLC DDP (dual die package)	L
MLC TDP (triple die package)	J
MLC QDP (quad die package)	H
3D MLC MONO (single die package)	1
3D MLC DDP (dual die package)	2
3D MLC TDP (triple die package)	9
3D MLC QDP (quad die package	3
3D MLC ODP (oct die package)	4

8.13 Pin Mode

Single nCE & R/nB	E
Dual nCE & R/nB	F
Triple nCE & R/nB	K
Quad nCE & R/nB	G

8.14 Configuration XYZ

X = Configuration

Default, non UHS	1
UHS-I	2

Y = Firmware Revision

durabit version 1	A
durabit version 2	B
durabit version 5	E

Z = Features

Standard	1
2plane	2
pSLC	P

8.15 Option

Swissbit/Standard	STD

9. Swissbit Specification

9.1 Top view

Figure 3: S-45u top view

- Swissbit logo
- Density
- SD Speedclass 10 logo
- UHS Speedclass U1 logo
- microSDXC logo
- UHS-I interface logo

9.2 Bottom view

Figure 4: S-45u bottom view

- Part number
- Manufacturing date
- Lot code

10. Revision History

Table 29: Document Revision History

Date	Revision	Description	Revision Details
January 27, 2015	0.90	Initial preliminary release	–
September 28, 2015	1.00	Standby currents, busy times, RoHS, ACPEIP and WEEE declaration	Doc. req. no. 0784
February 24, 2016	1.10	Generation 3 added, current performance values, registers	–
July 4, 2016	1.20	Updated Chapter 4, 5, 6 and removed CE declaration	Doc. req. no. 1157
November 11, 2016	1.21	Corrected typo in chapter Environmental Conditions and updated specification layout	Doc. req. no. 1365
June 07, 2017	1.22	Formal layout changes	Doc. req. no. 1710
January 07, 2019	1.32	Updated feature icons, removed A19 variations, added new variations with firmware "E", updated performance values and part number decoder.	Doc. req. no. 2726
March 29, 2019	1.33	Added new variations and changed data sheet layout	Doc. req. no. 2894
April 29, 2021	1.34	Formal changes, updated power up/down behavior and regulatory compliance.	Doc. req. no. 4552