

PET1300-12-054NA



FEATURES

- High efficiency up to 94.0%
- Wide input voltage range: 90-264 V_{AC}
- Active power factor correction
- Always-On 10 W standby output (3.3V)
- Hot-plug capability
- Parallel operation with active current sharing
- Full digital control for circuit loop and power management
- High density design: 30.25 W/in3
- Compact form factor: 54.5 x 40.0 x 321.5 in mm
- PMBus[™] for control, programming and monitoring
- Fully protected (OTP, OCP, OVP, SCP)
- 4K Bytes of EEPROM for user information
- 2 Status LEDs: FAIL and OK with fault signalling
- Approved to the following Safety Standards: UL/CSA60950-1 2nd
 Ed, EN60950-1 2nd Ed, and IEC60950-1 2nd Ed
- Designed to meet Class A emissions per CISPR 22 and EN55022

DESCRIPTION

The **PET1300-12-054NA** is a 1300 Watt AC to DC power-factor-corrected (PFC) power supply that converts standard AC mains power into a main output of $12V_{DC}$ for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches. The PET1300-12-054NA meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

APPLICATIONS

- HIGH PERFORMANCE SERVERS
- ROUTERS
- SWITCHES



1 ORDERING INFORMATION

PET	1300	-	12	-	054	X	Α
Product Family PET Front-Ends	Power Level 1300 W	Dash	V1 Output 12 V	Dash	Width 54 mm	Airflow N: Normal R: Reversed	Input A: AC

2 OVERVIEW

The PET1300-12-054NA AC/DC power supply is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range and minimal linear derating of output power with input voltage and temperature, the PET1300-12-054NA maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow paths.

The PFC stage is an analogue solution; MCU is used to communicate with DSP chip on secondary side.

The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and hence it is ideally suited for operation in redundant power systems.

The always-on standby output, with selectable voltage level (3.3Volts), provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with front-panel LEDs. In addition, the power supply can be controlled and the fan speed set via the I²C bus. The I²C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I²C bus.

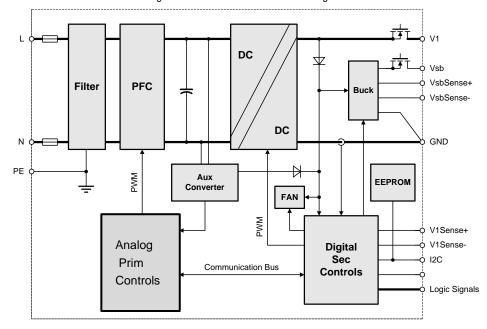


Figure 1: PET1300-12-054NA Block Diagram



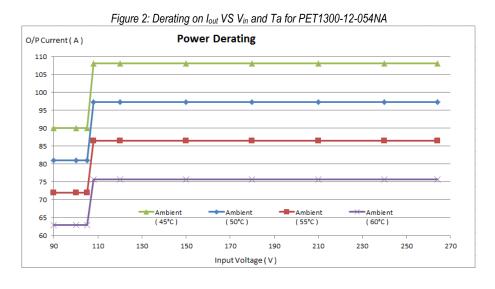
3 INPUT

General Condition: $T_A = 0... +60$ °C unless otherwise noted.

PARAME	TER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT	
V _{i nom}	Nominal Input Voltage		100		240	V _{AC}	
Vi	Input Voltage Ranges	Normal operating $(V_{i min} \text{ to } V_{i max})$	90		264	V _{AC}	
Dower	Dated Dawer (Figure 2)	Vin=90Vac-107.9Vac			1100	W	
Power	Rated Power (Figure 2)	Vin=108Vac-264Vac			1300	W	
l _{i max}	Max Input Current	Vin=110Vac/60Hz, Full load			13.6	Arms	
lip	Inrush Current Limitation	Vi min to Vi max, TNTC = 25°C			50	Ap	
Fi	Input Frequency		47	50/60	63	Hz	
PF	Power Factor	Vi nom, 50Hz, > 0.2 I1 nom		0.95		W/VA	
V _{i on}	Turn-on Input Voltage ¹⁾	Ramping up	85		90	V _{AC}	
V _{i off}	Turn-off Input Voltage ¹⁾	Ramping down	70		83	V _{AC}	
		V_{in} =230V,12V/21.6A,3.3V/0.6A T_{A} = 25°C		93.0			
η	Efficiency without Fan	V_{in} =230V,12V/54A,3.3V/1.5A T_{A} = 25°C		94.0		%	
	.	V_{in} =230V,12V/108A,3.3V/3A T_{A} = 25°C	V _{in} =230V,12V/108A,3.3V/3A T _A = 25°C		92.0		
Thold	Hold-up Time	After last AC zero point, V ₁ > 11.6V, V _{SB} within regulation, V _i = 230VAC, 12V/108A,3.3V/3A	10			ms	

¹⁾ The Front-End is provided with a minimum hysteresis of 3V during turn-on and turn-off within the ranges.

^{2) The} output power is linear derating to 70% full load if operation temperature increases from 45°C to 60°C as below curve.



Efficiency 94.50% 94.00% 93.50% 93.00% 92.50% 92.00% 91.50% Efficiency Data 91.00% ₩--- Platinum Limit 90.50% 90.00% 89.50% 20% 50% 100% Loading

Figure 3: Efficiency Measurement Curve



4 OUTPUT

General Condition: $T_a = 0 \dots +60$ °C unless otherwise noted.

	PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
		Main Output V₁				
V _{1 nom}	Nominal Output Voltage	0.5 ·/ _{1 nom} , T _{amb} = 25°C		12.0		V _{DC}
V _{1 set}	Output Setpoint Accuracy	0.5 11 nom, 7 amb - 25 C			+0.5	% V _{1 nom}
dV _{1 tot}	Total Regulation	V_{imin} to $V_{imax},0$ to 100% $\emph{I}_{1nom},\emph{T}_{amin}$ to \emph{T}_{amax}	-3		+3	% V _{1 nom}
P _{1 nom}	Nominal Output Power	$V_1 = 12 V_{DC}$		1296		W
I _{1 nom}	Nominal Output Current	$V_1 = 12 \text{ V}_{DC}, \text{ Vin} > = 108 \text{Vac}$		108		Adc
V 1 pp	Output Ripple Voltage	$V_{1 \text{ nom}}$, $I_{1 \text{ nom}}$, 20MHz BW			180	mVpp
dV _{1 Load}	Load Regulation	$V_i = V_{i \text{ nom}}, 0 - 100 \% I_{1 \text{ nom}}$		60		mV
dV1 Line	Line Regulation	$V_i = V_{i \text{ min}} V_{i \text{ max}}$		20		mV
الم	Current Sharing	when Bus load ≥ 27A			4.5	Α
dl _{share}	(abs (I1-I2), between any two units in parallel)	when Bus load < 27A			5.6	Α
dV_{dyn}	Dynamic Load Regulation	lout:10%60% of full load; 50%100% of full load	-0.6		0.6	V
T _{rec}	Recovery Time	$dI_1/dt = 1A/\mu s$, recovery within 1% of $V_{1 \text{ nom}}$		0.5	1	ms
t _{AC V1}	Start-up Time from AC				2	sec
tv1 rise	Rise Time	$V_1 = 1090\% V_{1 \text{ nom}}$		3		ms
CLoad	Capacitive Loading	T _a = 25°C			11000	μF
		Standby Output V _{SB}				
$V_{SB\;nom}$	Nominal Output Voltage	0.5 · / _{SB nom} . T _{amb} = 25°C		3.3		V _{DC}
V _{SB} set	Output Setpoint Accuracy	0.3 18B nom, 1 amb - 25 C	-1		+1	%V _{1nom}
dV _{SB tot}	Total Regulation	$V_{i min}$ to $V_{i max}$, 0 to 100% $I_{SB nom}$, $T_{a min}$ to $T_{a max}$	-1.5		+1.5	%V _{SBnom}
P _{SB nom}	Nominal Output Power	$V_{\rm SB}$ = 3.3 VDC , normal airflow		10		W
I _{SB nom}	Nominal Output Current	V _{SB} = 3.3 VDC, normal airflow		3		Adc
V _{SB pp}	Output Ripple Voltage	V _{SB nom} , I _{SB nom} , 20 MHz BW (See Section 5.1)			45	mVpp
dVsB	Droop	0 - 100 % / _{SB nom}		67		mV
dV _{SBdyn}	Dynamic Load Regulation	$\Delta I_{SB} = 50\% I_{SB \text{ nom}}, I_{SB} = 5 \dots 100\% I_{SB \text{ nom}},$	-3		3	%V _{SBnom}
Trec	Recovery Time	$d_{lo}/dt = 0.5 \text{ A/µs, recovery within 1% of } V_{1 \text{ nom}}$			250	μs
tac vsb	Start-up Time from AC				3	sec
t√SB rise	Rise Time	V _{SB} = 1090% V _{SB nom}		4	20	ms
C_{Load}	Capacitive Loading	T _{amb} = 25°C			1000	μF



5 PROTECTION

General Condition: $T_a = 0 \dots +60 \, ^{\circ}\text{C}$ unless otherwise noted.

	PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input Fuses (L+N)	Not user accessible, quick-acting (F)		16		Α
V _{1 OV}	OV Threshold V ₁		13.5		14.5	V_{DC}
<i>t</i> ov v1	OV Latch Off Time V ₁				1	ms
V _{SB OV}	OV Threshold V _{SB}		3.6		4.3	V_{DC}
tov vsb	OV Latch Off Time V _{SB}				1	ms
h	Current Limit V1	$V_i > =108 \text{ VAC}, T_a < 45^{\circ}\text{C}$	112	115	117	۸۰۰
I _{V1 lim}	Current Limit VI	V_i < =108 VAC, T_a < 45°C (refer to Figure 4)				A _{DC}
I _{sb lim}	Current Limit V1 T _{amb} = 25°C	Standby output can recovery.			4.5	Α
lv1 sc	Max Short Circuit Current V ₁			150		А
t _{V1} sc	Short Circuit Regulation Time	V_1 < 3V, time until I_{V1} is limited to < $I_{V1 \text{ sc}}$		2		ms
t√1 SC off	Short Circuit Latch Off Time	Time to latch off when in short circuit		500		ms
T _{SD}	Over Temperature On Heat Sinks	Automatic shut-down		115		°C

Typical OCP and OCP warning at $T_a = 0 \dots +60 \, ^{\circ}C$.

VIN (V)	OCP (A) 45°C	OCP WARNING (A) 45°C	OCP (A) 60°C	OCP WARNING (A) 60°C
90	95	93	66.5	64.5
100	97	95	67.9	65.9
108	115	113	80.5	78.5
110	115	113	80.5	78.5
120	115	113	80.5	78.5
264	115	113	80.5	78.5

Notes: The OCP and OCP warning are linear derating to 70% if operation temperature increases from 45° C to 60° C.

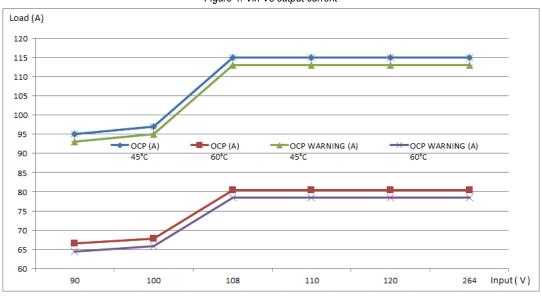


Figure 4: Vin Vs output current



6 SIGNALING AND CONTROL

6.1 FRONT LEDS

The front-end has 2 front LEDs showing the status of the supply. LED number one is green which indicates presence of AC power, LED number two is bi-colored: green and yellow, which indicates DC power presence or fault. For the position and states of the LEDs see *Table 1*.

Table 1: LED Status

POWER SUPPLY CONDITION	GREEN (OK) LED STATUS	AMBER (FAIL) LED STATUS
No AC power to all power supplies	OFF	OFF
Power Supply Failure (includes over voltage, over current, over temperature and fan failure)	OFF	ON
Power Supply Warning events where the power supply continues to operate (high temperature, high power and slow fan)	OFF	1Hz Blinking
AC Present/ 3.3VSB on (PSU OFF)	1Hz Blinking	OFF
Power Supply ON and OK	ON	OFF

^{*}When unit see fan failure, unit will shut down and can only be restarted by using PSON_L signal or AC input power recycling or PMBus commands. Refer to software spec. for detail.

6.2 ELECTRICAL CHARACTERISTICS

General Condition: $T_a = 0 \dots +60$ °C unless otherwise noted.

PARAMETER		DESCRIPTION/CONDITION	MIN	NOM	MAX	UNIT
	PSKILL_H/P	SON_L/PRESENT_L				
V _{IL}	Input Low Level Voltage		0		0.8	V
V _{IH}	Input High Level Voltage		2.0		3.6	V
I _{IL, H}	Maximum Input Sink or Source Current		0		1	mA
R _{puSKILL_} H	Internal Pull Up Resistor on PSKILL_H			10		kΩ
R _{puPSON_L}	Internal Pull Up Resistor on PSON_L			10		kΩ
R _{puPRESENT_L}	Internal Pull Up Resistor on PRESENT_L			None		kΩ
RLOW	Resistance Pin to SGND for Low Level		0		1	kΩ
Rhigh	Resistance Pin to SGND for High Level		50			kΩ
	PWC	K_H Output				
V _{ext}	Maximum External Pull Up Voltage				3.6	V
Vol	Output Low Level Voltage	I _{sink} < 2 mA	0		0.4	V
V _{OH}	Output High Level Voltage	/source < 0.5 mA	2.4		3.6	V
R _{puPWOK_} H	Internal Pull Up Resistor on PWOK_H			None		kΩ
	ACC	K_H Output	'	'		
V _{ext}	Maximum External Pull Up Voltage				3.6	V
VoL	Output Low Level Voltage	I _{sink} < 2 mA	0		0.4	V
V _{OH}	Output High Level Voltage	/source < 0.5 mA	2.4		3.6	V
П риАСОК_Н	Internal Pull Up Resistor on ACOK_H			None		kΩ
	SMB_A	LERT_L Output				
V _{ext}	Maximum External Pull Up Voltage				12	V
V _{OL}	Output Low Level Voltage	Isink < 2 mA	0		0.4	V
I _{OH}	Maximum High Level Leakage Current				10	uA
R _{puSMB_ALERT_L}	Internal Pull Up Resistor on SMB_ALERT_L			None		kΩ



6.3 GRAPHICAL USER INTERFACE

Power-One provides with its "Power-One I²C Utility" a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PET1300-12-054NA Front-End. The utility can be downloaded on www.power-one.com and supports both the PSMI and PMBus™ protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

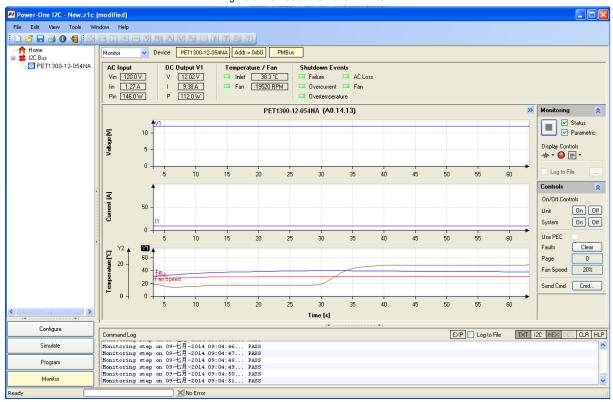


Figure 5: I²C Bus to DSP and EEPROM

Table 2: Accuracy for PMBus

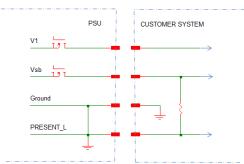
COMMOND	10% ~ 20% FULL LOAD	20% ~ 100% FULL LOAD	REMARK
Read_lin	<0.5 A	+/-3%	It is for corresponding to max input current
Read_lout	+/-2%	+/-2%	It is for corresponding to max output current
Read_Vin	+/-3%	+/- 2.5 V	
Read_Vout	+/-2%	+/-2%	
Read_Pin		+/-15%	It is for corresponding to max input power
Read_Pout	+/-3%	+/-3%	It is for corresponding to max output power



6.4 PRESENT_L

The PRESENT_L is an output signal and it is used to sense the number of power supplies in the system (operational or not). This signal is connected to the power supply's output ground. Electrical characteristics see 6.2.

Interconnect diagram of PRESENT_L signal

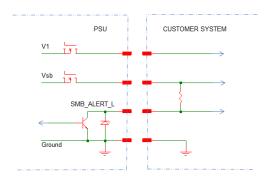


6.5 SMB_ALERT_L

The SMB_ALERT_L is an output signal and shall be an open collector with the pull-up resistor located at the receiving end and shall capable of sinking up to 4 mA.

This signal indicates that the power supply is experiencing a problem that the user should investigate. This may be asserted due to Critical events or Warning events. See PMBUS specification for further details.

Interconnect diagram of SMB_ALERT_L signal



6.6 PSKILL H

This is an input signal and is used to force the 12V main output off if the supply is removed from the system. At the system level this pin will be connected to the output return directly. When this input is low the power supply will operate. If the input is floating the 12V main output will turn off while the 3.3VSB will remain on. This signal overrides all other on-and-off signals. On the power supply connector, this pin is shorter than the others so it is a last-make and first-break contact. See below Table 3 for Logic Table.

Interconnect diagram of PSKILL_H signal

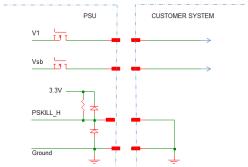




Table 3: PS_KILL Signal Characteristics

Signal Type:	Accepts a ground input from the system.		
Input Signal to the power supply	Pull-up to 3.3VSB located in the power supply.		
PS_KILL = Low, PS_ON = Low	ON		
PS_KILL = Open, PS_ON = Low or Open	OFF		
PS_KILL = Low, PS_ON = Open	OFF		
	MIN	MAX	
Source current, Vps_kill =Low		4mA	

6.7 PSON L

The PS_ON_L signal is an input signal used to remotely turn on/off the power supply. PS_ON_L is an active LOW signal that turns on the 12V main output. In the low state this input will not source more than 4mA of current. The 12V output will be disabled when this input is driven HIGH, or open circuited. See Table 4 for Logic Table.

Interconnect diagram of PSON_L signal

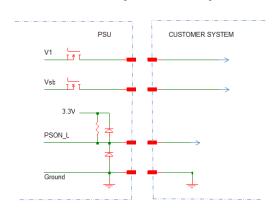


Table 4: PS_ON_L Signal Characteristics

Signal Type: Input signal to the power supply	Accepts an open collector/drain input from the system. Pull-up to 3.3VSB located in power supply.		
PS_ON_L = Low, PS_KILL = Low	ON		
PS_ON_L = Open, PS_KILL = Low or Open	OFF		
PS_ON_L = Low, PS_KILL = Open	OFF		
	MIN	MAX	
Output Source Current, VPS_ON_L= Low 4mA		4mA	

6.8 PW_OK

PW_OK is an output signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When 12V main output is < 10.9V or > 13.2V, or if any of the outputs fail due to over current protection, over voltage protection, over temperature, or fan failure then this output will be driven LOW. In the event when AC mains power is lost, this signal will be driven LOW at least 20 msec before the +3.3VSB output is lost. The output will be an open collector/drain. The start of the PW_OK delay time shall be inhibited as long as any power supply's 12V output is in current limit. See Table 5.



Interconnect diagram of PW_OK signal

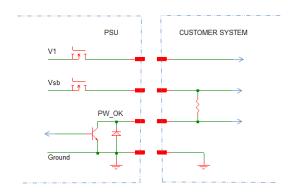


Table 5: PW_OK Signal Characteristics

Signal Type:	Open collector/drain (system side to provide pull-up, another pull-		
Output signal from the power supply	up to 3.3VSB could also be located in the power supply)		
PW_OK = High	Power OK		
PW_OK = Low	Power Not OK		
	MIN	MAX	
Input Sink current, PW_OK = Low		4mA	
Output Source current, PW_OK = High		2mA	

6.9 AC_OK

This signal is an output signal and will be asserted, driven HIGH, by the power supply to indicate that the input voltage meets the minimum requirements of Section 3.1.3. After falling outside the input voltage requirements for more than 20 msec, the signal must be driven LOW. The output will be an open collector/drain. See below Table 6.

Interconnect diagram of AC_OK signal

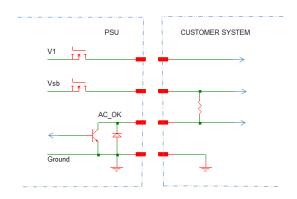


Table 6: AC_OK Signal Characteristics

Signal Type: Output signal from the power supply	Open collector/drain	Open collector/drain (system side to provide pull-up, another pull-up to 3.3VSB could also be located in the power supply)		
AC_OK = High	AC OK	AC OK		
AC_OK = Low	AC Low (Not OK)	AC Low (Not OK)		
	MIN	MAX		
Input Sink current, AC_OK = Low		4mA		
Output Source current, AC_OK = High		2mA		

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6.10 Current Sharing

All outputs shall be capable of operating in a redundant current share mode. A maximum of 6 power supplies may be operated in parallel. All outputs shall incorporate an isolation device (Or-ing MOSFET or diode) for fault isolation. Filter capacitors that are located after the isolation device shall be of high reliability and shall be de-rated sufficiently to minimize failures. The 3.3V output current sharing shall be of a droop type. The +12V current sharing shall be a single wire type, active current sharing. Connecting the Ishare (current share) pins of each power supply together shall enable the current share feature. Shorting or opening of a current share pin shall not cause the output voltage to go out of steady state regulation. For 12V output the Ishare (load sharing) voltage shall be a linear function Ishare [V] = 8 x lout/108 (with 8 V at 108A) for a single power supply (~74mV/A).

At light load, the load share becomes difficult because of low feedback signal. Refer to Table 2 for current sharing accuracy. The current balance accuracy is calculated as: 2*|I1-I2|/ (I1+I2), where the I1 is the PSU1 load current and I2 is the PSU2 load current.

6.11 Remote Sense

The outputs specified shall incorporate remote sense and will compensate for specified load cable drop. In the event of loss of remote sense, all outputs shall revert to internal sense so as to limit the outputs to less than 105% of nominal.

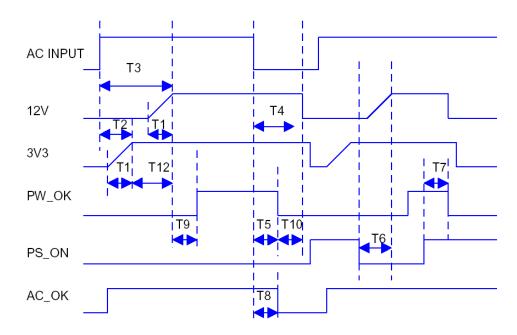


7 TIMING DIAGRAM AND TABLE

Unless defined otherwise, all control signals shall be TTL compatible with respect to the output return and shall be isolated from the primary circuit and be SELV rated. All input signals shall be driven from an open collector with the pull-up resistor located in the power supply and shall be capable of sourcing up to 4 mA. General LVTTL signal levels are specified in below table except where explicitly specified otherwise.

Table 7: Low-Voltage TTL (LVTTL) voltage levels

PARAMETER	SYMBOL	MIN	MAX	UNITS
Output High Voltage	Voh	2.4	3.6	V
Output Low Voltage	Vol	0	0.4	V
Input High Voltage	Vih	2.0	3.6	V
Input Low Voltage	Vil	0	0.8	V



PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/COMMENTS
T1 (Tout_rise)	0.5		100	msec	Output voltage rise time from each main output
T2 (Tsb_on_delay)			2500	msec	Delay from AC being applied to 3V3 being within regulation
T3 (Tac_on_delay)			3000	msec	Delay from AC being applied to all output voltages being within regulation
T4 (Tvout_holdup)	10			msec	Time all output voltages, including 3V3, stay within regulation after loss of AC
T5 (Tpw_ok_holdup)	5			msec	Delay from loss of AC to de-assertion of PW_OK
T6 (Tps_on_delay)	5		400	msec	Delay from PS_ON_L active to output voltages within regulation limits
T7 (Tps_on_pw_ok)			50	msec	Delay from PS_ON_L de-active to PW_OK being de-asserted
T8 (Tac_ok_off)			20	msec	Delay from loss of AC input to de-assertion of AC_OK
T9 (Tpw_ok_on)	100		1000	msec	Delay from output voltages within regulation limits to PW_OK asserted at turn on
T10 (Tpw_ok_off_12V)	1		700	msec	Delay from PW_OK de-asserted to 12VDC dropping out of regulation limits
T11 (Tpw_ok_off_3V3)	20			msec	Delay from PW_OK de-asserted to 3V3 dropping out of regulation limits
T12 (Tsb_vout)	50		1000	msec	Delay from 3V3 being in regulation to 12VDC being in regulation at AC turn on.
T13 (Tac_ok_on)			1500	msec	Delay from AC being applied to assertion of AC_OK

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8 IMMUNITY

NOTE: Most of the immunity requirements are derived from EN 55024:1998/A2:2003.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point	A
g	(metallic case, LEDs, connector body)	
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point	A
g	(non-metallic user accessible surfaces)	
Radiated Electromagnetic Field	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation,	A
Tradiated Electromagnetic Field	1 µs Pulse Modulation, 10 kHz2 GHz	<i>n</i>
	IEC / EN 61000-4-4, level 3	
Burst	AC port ±2 kV, 1 minute	A
	DC port ±1 kV, 1 minute	
	IEC / EN 61000-4-5	
Surge	4kV CM	A
	2kV DM	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 80 MHz	A
	IEC/EN 61000-4-11	
Valtage Dine and Interputions	1: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration 10 ms	A
Voltage Dips and Interruptions	2: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration 20 ms	V _{SB} : A, V ₁ : B
	3: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration >20 ms	V _{SB} , V ₁ : B

8.1 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
	EN55022 / CISPR 22: 0.15 30 MHz, QP and AVG, single unit	Class A
Conducted Emission	EN55022 / CISPR 22: 0.15 30 MHz, QP and AVG, 2 units in rack system	Class A
	EN55022 / CISPR 22: 30 MHz 1 GHz, QP, single unit	Class A
Radiated Emission	EN55022 / CISPR 22: 30 MHz 1 GHz, QP, 2 units in rack system	Class A
Harmonic Emissions	IEC61000-3-2, Vin = 115 VAC / 60 Hz, & Vin = 230VAC/ 50 Hz, 100% Load	Class A
Acoustical Noise	46 dBA at 1 meter, 25°C, 50% Load	-
AC Flicker	IEC61000-3-3, Vin = 230 VAC / 60 Hz, 100% Load	Pass

9 SAFETY/APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, UL 60950, CCC and BSMI. Input-to-output electric strength tests should not be repeated in the field. Power-One will not honor any warranty claims resulting from electric strength field tests.

	PARAMETER	DESCRIPTION / CONDITION	MIN NOM MAX	UNIT
	Agency Approvals	UL 60950-1 Second Edition CAN/CSA-C22.2 No. 60950-1-07 Second Edition IEC 60950-1:2005 EN 60950-1:2006 CCC BSMI	Approved by independent body (see CE Declaration)	
		Input (L/N) to case (PE)	Basic	
	Isolation Strength	Input (L/N) to output	Reinforced	
		Output to case (PE)	Functional	
d c	Creepage / Clearance	Primary (L/N) to protective earth (PE)		mm
uc uc	Creepage / Creatance	Primary to secondary	According to	mm
		Input to case	According to	
	Electrical Strength Test	Input to output	safety standard	kVac
		Output and Signals to case		



10 ENVIRONMENTAL

	PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T _A	Ambient Temperature	V _{i min} to V _{i max} , I _{1 norm} , I _{SB nom}	0		+60	°C
Ts	Storage Temperature	Non-operational	-40		+85	°C
	Altitude	Operational, above Sea Level	-		10,000	Feet
Na	Audible Noise	$V_{i=230Vac}$, 50% $I_{o nom}$, $T_{A} = 25^{\circ}$ C		42		dBA

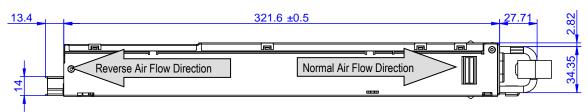
Note: Refer to Figure 2 for Derating

11 MECHANICAL

	PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
		Width	54.1	54.5	54.9	
	Dimensions	Height	39.6	40.0	40.4	mm
		Depth	321.1	321.6	322.1	
М	Weight			1.09		kg

Otherwise stated, Tolerance: 0.5mm - 120mm: ±0.3mm; 120mm - 400mm: ±0.5mm

Figure 6: Side View 1



NOTE: A 3D step file of the power supply casing is available on request.

Figure 7: Top View

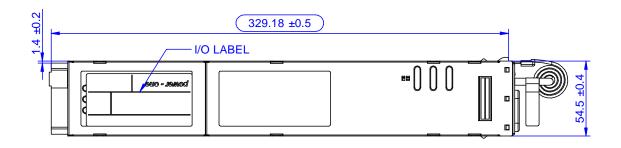


Figure 8: Side View 2

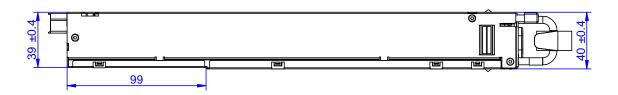
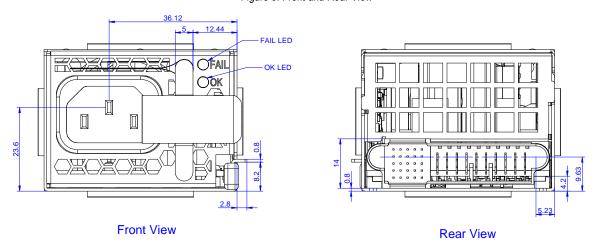
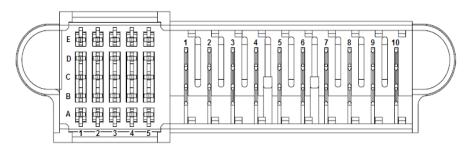




Figure 9: Front and Rear View



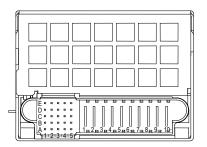
12 CONNECTIONS



Unit: Tyco Electronics P/N 1926736-2 or FCI 10122460-002LF

Counter part: Tyco Electronics P/N 2-1926739-5 or FCI 10108888-R10253SLF (Power-one P/N: ZES.00672)

PIN	NAME	DESCRIPTION		
		Output		
6, 7, 8, 9, 10	V1	+12 VDC main output		
1, 2, 3, 4, 5	PGND	Power ground (return)		
	C	Control Pins		
A1, B1, C1, D1, E1	VSB	Standby positive output (+3.3 V)		
A2, B2	SGND	Signal ground (return)		
C2	NC	Reserved		
D2	NC	Reserved		
E2	NC	Reserved		
A3	PS_KILL	Power supply kill (lagging pin)		
В3	NC	Reserved		
C3	SDA	I ² C data signal line		
D3	V1_SENSE_R	Main output negative sense		
E3	V1_SENSE	Main output positive sense		
A4	SCL	I ² C clock signal line		
B4	PS_ON_L	Power supply on input (connect to A2/B2 to turn unit on)		
C4	ALERT_L	SMB Alert signal output		
D4	ISHARE	12V current share signal (LS)		
E4	AC_OK	AC input OK signal		
A5	A0	Address 0		
B5	NC	Reserved		
C5	PW_OK	Power OK signal output (lagging pin)		
D5	A1	Address 1		
E5	E5 PRESENT_L Power supply present (lagging pin)			





13 ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	Power-One I ² C Utility Windows XP/Vista/7 compatible GUI to program, control and monitor PET Front-Ends (and other I ² C units)	N/A	www.power-one.com
Evaluation board	Dual Connector Board Connector board to operate 2 PET units in parallel. Includes an on-board USB to I ² C converter (use <i>Power-One</i> I ² C Utility as desktop software).	VRA.00333.0	Power-One

14 PMBUS COMMNUCATION

14.1 ADDRESS SELECT

Table 8: Address Select

A2	A 1	Α0	UNIT ADDRESS	EEPROM ADDRESS
0	0	0	0xB0	0xA0
0	0	1	0xB2	0xA2
0	1	0	0xB4	0xA4
0	1	1	0xB6	0xA6

NOTE: A2= 1 is not implemented.

14.2 PMBUS COMMANDS

NOTE:

Reference: PMBus Power System Management Protocol Specification Part II – Command Language Revision 1.1.

Commands not included in the table below are Not Implemented.

Feature that are <u>To Be Defined (TBD)</u>, or <u>Not Implemented</u> are shaded.

R = Read-Only; RW = Read/Write; W = Write-Only

Table 9: PMBus Commands

COMMAND NAME BIT NAME	CODE	BIT	VALUE	ACCESS	DATA BYTES	REMARKS
PAGE	00h		-	RW	1	Page 0 applies to +12V output Page 1 applies to +3.3V output Other Page values are considered invalid and will generate an INVALID_DATA error.
OPERATION	01h				1	
		7-6	-	RW		0b00 = OFF 0b10 = ON (Default)
		5-0	0d	R		Not Implemented
CLEAR_FAULTS	03h		-	W	0	Clear all bits in all status registers.
CAPABILITY	19h			R	1	
PACKET_ERROR_CHECKING		7	0b1			Supported
MAXIMUM_BUS_SPEED		6-5	0b01			400kHz
SMBALERT#		4	0b1			Supported
RESERVED		3-0	0b0000			Reserved
VOUT_MODE	20h		-	R	1	
MODE		7-5	0b000			Linear
PARAMETER		4-0	0b10111			N = -9
FAN_CONFIG_1_2	3Ah			R	1	



COMMAND NAME BIT NAM	E CODE	BIT	VALUE	ACCESS	DATA BYTES	REMARKS
		7	0b1			Fan1 Installed
		6	0b0			Fan1 Commanded in Duty Cycle
		5-4	0b01			Fan1 (2) Tachometer Pulses per Revolution
		3	0b0			Fan2 Not Installed
		2	0b0			Don't Care
		1-0	0b00			Don't Care
FAN_COMMAND_1	3Bh		-	RW	2	MIN = 0 → 0% MAX = 100 → 100% Values outside limits will generate INVALID_DATA error. Write request is executed only if the desired Fan speed is greater than what is required by the PSU. Fan Speed = FAN_COMMAND*21000RPM/100
STATUS_BYTE	78h			R	1	STATUS bits remain set, even if the fault or warning is removed. They are reset by: CLEAR_FAULTS Command AC Recycle PSON Recycle
BUSY		7	0b0			Not Implemented
OFF		6	-			
VOUT_OV		5	-			
IOUT_OC		4	-			
VIN_UV		3	-			
TEMPERATURE		2	-			
CML		1	-			
NONE_OF_THE_ABOVE		0	0b0	_		Not Implemented
STATUS_WORD	79h			R	2	
VOUT		F	-			
IOUT/POUT		E	-			
INPUT MFR		D C	-			
POWER_GOOD#		В	-			
FANS		A	-			
OTHER		9	_			
UNKNOWN		8	0b0			Not Implemented
STATUS_BYTE		7-0	-			See STATUS_BYTE
STATUS_VOUT	7Ah	1-0	_	R	1	OCC OTATOO_BITE
VOUT_OV_FAULT	7741	7	-	, , ,	<u>'</u>	Asserts when an OV fault condition is detected on V1 output. SMB Alert Mask = 1 (Default)
VOUT_OV_WARNING		6	0b0			Not Implemented
VOUT_UV_WARNING		5	0b0			Not Implemented
VOUT_UV_FAULT		4	-			Asserts when an UV fault condition is detected on V1 output. SMB Alert Mask = 1 (Default)
VOUT_MAX_WARNING		3	0b0			Not Implemented
TON_MAX_FAULT		2	-			Asserts when V1 output is not in regulation 3s after PSON and AC is applied. SMB Alert Mask = 1 (Default)
TOFF_MAX_WARNING		1	0b0			Not Implemented
PWR_ON_TRACKING_ERROR		0	0b0			Not Implemented
STATUS_IOUT IOUT_OC_FAULT	7Bh	7	-	R	1	Asserts when an OC fault condition is detected on V1 output. SMB Alert Mask = 1 (Default)
IOUT_OC_FAULT_LV		6	0b0			Not Implemented
IOUT_OC_WARNING		5	0b0			Asserts when an OC warning condition is detected on V1 output. SMB Alert Mask = 0 (Default)



COMMAND NAME	CODE	BIT	VALUE	ACCESS	DATA	REMARKS
BIT NAME	UUDL			7.00200	BYTES	
IOUT_UC_FAULT		4	0b0			Not Implemented
ISHARE_FAULT		3	0b0			Not Implemented
PIN_LIMITING_MODE		2	0b0			Not Implemented
POUT_OP_FAULT		1	0b0			Not Implemented
POUT_OP_WARNING		0	0b0			Not Implemented
STATUS_INPUT	7Ch			R	1	
VIN_OV_FAULT		7	0b0			Not Implemented
VIN_OV_WARNING		6	0b0			Not Implemented
VIN_UV_WARNING		5	0b0			Not Implemented
VIN_UV_FAULT		4	0b0			Not Implemented
						Asserts when the PSU is disabled
UNIT_OFF_VIN_LOW		3	-			because of low input voltage.
						SMB Alert Mask = 1 (Default)
IIN_OC_FAULT		2	0b0			Not Implemented
IIN_OC_WARNING		1	0b0			Not Implemented
PIN_OP_WARNING		0	0b0			Not Implemented
STATUS_TEMPERATURE	7Dh			R	1	
						Asserts when an OT fault condition is
OT_FAULT		7	_			detected.
		,				SMB Alert Mask = 1 (Default)
						Asserts when an OT warning condition is
OT_WARNING		6	_			detected.
0						SMB Alert Mask = 1 (Default)
UT_WARNING		5	0b0			Not Implemented
UT_FAULT		4	0b0			Not Implemented
RESERVED		3-0	0b0000			Reserved
STATUS_CML	7Eh	0.0	000000	R	1	reserved
STATUS_CIVIL	711			IX		Asserts when the System tries to access unsupported commands, write to
INVALID_COMMAND		7	-			supported commands with read-only access, or read supported commands with write-only access.
INVALID_DATA		6	-			SMB Alert Mask = 0 (Default) Asserts when the System tries to write invalid data (including when PEC byte is incorrect) to supported commands with write access. SMB Alert Mask = 0 (Default)
						Asserts when the received PEC byte is
PEC_FAIL		5	_			incorrect.
_						SMB Alert Mask = 0 (Default)
MEMORY_FAULT		4	0b0			Not Implemented
PROCESSOR_FAULT		3	0b0			Not Implemented
RESERVED		2	0b0			Reserved
OTHER_COMM_FAULT		1	0b0			Asserts when the communication between monitoring components inside the PSU is lost. SMB Alert Mask = 0 (Default)
OTHER_MEMORY_FAULT		0	0b0			Not Implemented
STATUS_OTHER	7Fh			R	1	
RESERVED		7	0b0			Reserved
RESERVED		6	0b0			Reserved
INPUT A FUSE		5	0b0			Not Implemented
INPUT A FUSE		4	0b0			Not Implemented
INPUT A ORING		3	0b0			Not Implemented
		2	0b0			
INPUT B ORING OUTPUT ORING		1	-			Not Implemented Asserts when a fault is detected on the V1 ORing device.
						SMB Alert Mask = 0 (Default)
		0	0b0			Reserved
RESERVED		U	UUU			1 1 C 3 C 1 V C U
RESERVED STATUS MFR SPECIFIC	80h	U	UDU	R	1	Reserved
RESERVED STATUS_MFR_SPECIFIC RESERVED	80h	7	0b0	R	1	Reserved



COMMAND NAME BIT NAME	CODE	BIT	VALUE	ACCESS	DATA BYTES	REMARKS
RESERVED		5	0b0			Reserved
RESERVED		4	0b0			Reserved
VSB_UV_FAULT		3	-			Asserts when an UV fault condition is detected on Vsb output. SMB_Alert Mask = 0 (Default)
VSB_OV_FAULT		2	-			Asserts when an OV fault condition is detected on Vsb output. SMB_Alert Mask = 0 (Default)
PHASE_SHARE_FAULT		1	-			Asserts when there is a current imbalance between DCDC Phases. SMB_Alert Mask = 0 (Default)
HOLDUP_FAULT		0	-			Asserts when V1 goes out of regulation if Bulk voltage level is reduced. SMB_Alert Mask = 0 (Default)
STATUS_FANS_1_2	81h			R	1	
FAN1_FAULT		7	-			Asserts when a Fan fault condition is detected. SMB Alert Mask = 1 (Default)
FAN2_FAULT		6	0b0			Not Implemented
FAN1_WARNING		5	0b0			Not Implemented
FAN2_WARNING		4	0b0			Not Implemented
FAN1_SPEED_OVERRIDE		3	-			Asserts when the Fan is running according to the speed defined by the System. SMB Alert Mask = 0 (Default)
FAN2_SPEED_OVERRIDE		2	0b0			Not Implemented
AIR_FLOW_FAULT		1	0b0			Not Implemented
AIR_FLOW_WARNING		0	0b0			Not Implemented
READ_VIN	88h		-	R	2	Linear Format, N = -1
READ_IIN	89h		-	R	2	Linear Format, N = -6
READ_VOUT	8Bh		-	R	2	Linear Format, N = -9 Refer to Section 8.3.1 of PMBus Spec Part II Revision 1.1
READ_IOUT	8Ch		-	R	2	Linear Format, N = -3
READ_TEMPERATURE_1	8Dh		-	R	2	Linear Format, N = -2 Inlet Temperature
READ_TEMPERATURE_2	8Eh		-	R	2	Linear Format, N = -2 Outlet Temperature
READ_TEMPERATURE_3	8Fh		-	R	2	Linear Format, N = -2 ORing FET Temperature
READ_FAN_SPEED_1	90h		-	R	2	Linear Format, N = 5
READ_POUT	96h		-	R	2	Linear Format, N = 1
READ_PIN	97h		-	R	2	Linear Format, N = 1
MFR_ID	99h		-	R	CNT+9	ID = POWER-ONE Format: ASCII
MFR_MODEL	9Ah		-	R	CNT+16	MODEL = PET1300-12-054NA Format: ASCII
MFR_REVISION	9Bh		-	R	CNT+3	REVISION = vvv Format: ASCII
MFR_LOCATION	9Ch		-	R	2	LOCATION = xx Format: ASCII
MFR_DATE	9Dh		-	R	CNT+4	DATE = yyww Format: ASCII
MFR_SERIAL	9Eh		-	R	CNT+18	SERIAL = xxzzzzzzzzvvvuuuuu Format: ASCII
CALIBRATION_POINTER	C0h		-	RW	2	For Power-One Use Only
CALIBRATION_DATA	C1h		-	RW	2	For Power-One Use Only
CALIBRATION_COMMAND_	C2h		-		2	For Power-One Use Only
RESERVED		F-1	0d	R		Reserved
COMMIT_TO_FLASH		0	-	RW		0 = No Action 1 = Commit RAM to Flash
READ_VSTBY	C3h		-	R	2	For Power-One Use Only Same format as READ_VOUT



COMMAND NAME BIT NAME	CODE	BIT	VALUE	ACCESS	DATA BYTES	REMARKS
READ_ISTBY	C4h		-	R	2	For Power-One Use Only Same format as READ_IOUT
READ_VOUT_INT	C5h		-	R	2	For Power-One Use Only Same format as READ_VOUT
BOOTLOADER_STATUS_REQUEST	C7h			RW	2	For Power-One Use Only
BOOTLOADER_PAGE_DATA	C8h		-	W	-	For Power-One Use Only
PRODUCT_ID_NUMBER	C9h			R	2	For Power-One Use Only Refer to Table 3
FW_REV	CAh			R	2	For Power-One Use Only
SEC_DSP_MAJOR		F-C	-			M = 0 to 9
SEC_DSP_MINOR		B-8	-			m = 0 to 9 i.e: Mm = $25 \rightarrow$ Revision 2.5
PRI_DSP_MAJOR		7-4	-			M = 0 to 9
PRI_DSP_MINOR		3-0	-			m = 0 to 9 i.e: Mm = 13 → Revision1.3
SEC_CTRL1	CCh			R		For Power-One Use Only
SEC_CTRL2	CDh			R		For Power-One Use Only
SEC_STAT	CEh			R		For Power-One Use Only
PRI_STAT	CFh			R		For Power-One Use Only
MFR_SPECIFIC_00 (PSU_CONTROL)	D0h				2	
RESERVED		F-1	0d	R		Reserved
EEPROM_WP		0	-	RW		EEP Write-Protect (WP) Control 0 = Enable WP (Default) 1 = Disable WP
MFR_SPECIFIC_05 (FW_VERSION)	D5h		-	R	8	Format: xx.xx.xx (e.g. 01.02.01). The length is fixed at 8 Ascii characters. Each field will be an Ascii value stored in one byte. * For example: aa.bb.cc, where aa is development stage (P0, P1 A0); bb is primary mcu firmware revision (00 ~ 99); cc is secondary mcu firmware revision (00 ~ 99). NO BYTE COUNT
MFR_SPECIFIC_09 (SMB_ALERT_MASKING)	D9h		-	RW	7	Refer to Table 4 NO BYTE COUNT

Table 10: Product ID Number

BIT(S)	DESCRIPTION	REMARKS
F-A	Product Family	TBD
9-8	Communication Protocol	0b00 = Reserved 0b01 = Reserved 0b10 = PMBus 0b11 = Reserved
7-0	Product Part Number	TBD



Table 11 SMB_ALERT Masking

BYTE	BYTE DESCRIPTION	BIT	BIT DESCRIPTION	DEFAULT
0	GLOBAL_MASK	7	Not Implemented	-
		6	Not Implemented	-
		5	Not Implemented	-
		4	Not Implemented	-
		3	Not Implemented	-
		2	Not Implemented	-
		1	Not Implemented	-
		0	Global Mask. Clear to disable SMB_ALERT	1
1	STATUS_VOUT	7	VOUT_OV_FAULT Mask	1
		6	Not Implemented	-
		5	Not Implemented	-
		4	VOUT_UV_FAULT Mask	1
		3	Not Implemented	-
		2	TON_MAX_FAULT Mask	1
		1	Not Implemented	-
		0	Not Implemented	-
2	STATUS_IOUT	7	IOUT_OC_FAULT Mask	1
		6	Not Implemented	-
		5	Not Implemented	-
		4	Not Implemented	-
		3	Not Implemented	-
		2	Not Implemented	_
		1	Not Implemented	
		0	Not Implemented	-
3	STATUS_TEMPERATURE	7	OT_FAULT Mask	1
3	STATUS_TEMPERATURE			
		6	OT_WARNING Mask	1
		5	Not Implemented	-
		4	Not Implemented	-
		3	Not Implemented	-
		2	Not Implemented	-
		1	Not Implemented	-
		0	Not Implemented	-
4	STATUS_INPUT	7	Not Implemented	-
		6	Not Implemented	-
		5	Not Implemented	-
		4	Not Implemented	-
		3	UNIT_OFF_VIN_LOW Mask	1
		2	Not Implemented	-
		1	Not Implemented	-
		0	Not Implemented	-
5	STATUS_FANS_1_2	7	FAN1_FAULT Mask	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		6	Not Implemented	-
		5	Not Implemented	-
		4	Not Implemented	-
		3	FAN1_SPEED_OVERRIDE Mask	0
		2	Not Implemented	-
		1	Not Implemented	_
		0	Not Implemented	-
6	STATUS_CML	7	INVALID_COMMAND Mask	0
U	STATUS_CIVIL	6	INVALID_COMMAND Mask INVALID_DATA Mask	0
		5	PEC_FAIL Mask	0
		4	Not Implemented	-
		3	Not Implemented	-
		2	Not Implemented	-
		1	Not Implemented	-
		0	Not Implemented	-

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