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NTE27C512–12D
NTE27C512–15D
Integrated Circuit
512 Kbit (64Kb x 8) UV EPROM

Description:

The NTE27C512 is a 512Kbit UV EPROM in a 28–Lead DIP type package ideally suited for microprocessor systems requiring large programs and is organized as 65,536 by 8 bits. This device has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Features:

- 5V ±10% Supply Voltage in Read Operation
- Access Time: 45ns
- Low Power "CMOS" Consumption:
  - Active Current 30mA
  - Standby Current 100μA
- Programming Voltage: 12.75V ±0.25V
- Programming Time of Around 6 Seconds

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} . . . . . –2 to +7V
Input or Output Voltage (Except A9, Note 2), V_{IO} . . . . . –2 to +7V
A9 Voltage (Note 2), V_{A9} . . . . . –2 to +13.5V
Program Supply Voltage, V_{PP} . . . . . –2 to +14V
Ambient Operating Temperature Range, T_A . . . . . –40° to +125°C
Temperature Under Bias Range, T_{BIAS} . . . . . –50° to +125°C
Storage Temperature Range, T_{STG} . . . . . –65° to +150°C

Note 1. Except for the rating "Operating Temperature Range", stresses above those listed in the table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Note 2. Minimum DC voltage on the input or output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Device Operation:

The modes of operation of the NTE27C512 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9.

Read Mode:

The NTE27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least $t_{AVQV}-t_{GLQV}$.

Operating Modes:

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q7–Q0
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi–Z
Program	V_{IL} Pulse	V_{PP}	X	Data Input
Program Inhibit	V_{IH}	V_{PP}	X	Hi–Z
Standby	V_{IH}	X	X	Hi–Z

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ±0.5V.

Capacitance: (T_A = +25°C, f = 1MHz, Note 3 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	12	pF

Note 3. Sampled only, not 100% tested.

Standby Mode:

The NTE27C512 has a standby mode which reduces the supply current from 30mA to 100μA. The NTE27C512 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control:

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. The lowest possible memory power dissipation,

b. Complete assurance that output bus connection will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Read Mode DC Characteristics: (T_A = 0° to +70°C, V_{CC} = 5V ±5% or 5V ±10%, V_{PP} = V_{CC}, Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	$0V \le V_{IN} \le V_{CC}$	–	–	±10	μA
Output Leakage Current	I_{LO}	$0V \le V_{OUT} \le V_{CC}$	–	–	±10	μA
Supply Current	I_{CC}	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz	–	–	30	mA
Supply Surrent (Standby) TTL	I_{CC1}	$\overline{E} = V_{IH}$	–	–	1	mA
CMOS	I_{CC2}	$\overline{E} > V_{CC} - 0.2V$	–	–	100	μA
Program Current	I_{PP}	$V_{PP} = V_{CC}$	–	–	10	μA
Input Low Voltage	V_{IL}		–0.3	–	0.8	V
Input High Voltage	V_{IH}	Note 5	2	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
Output High Voltage TTL	V_{OH}	I_{OH} = –1mA	3.6	–	–	V
CMOS		I_{OH} = –100μA	V_{CC}–0.7	–	–	V

Note 4. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
Note 5. Maximum DC voltage on output is V_{CC} +0.5V.

System Considerations:

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1μF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7μF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Read Mode AC Characteristics: (T_A = 0° to +70°C, V_{CC} = 5V ±5% or 5V ±10%, V_{PP} = V_{CC}, Note 4 unless otherwise specified)

Parameter	Symbol	Alt.	Test Conditions	Min	Typ	Max	Unit
Address Valid To Output Valid NTE27C512–12D	t_{AVQV}	t_{ACC}	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	–	–	120	ns
NTE27C512–15D				–	–	150	ns
Chip Enable Low To Output Valid NTE27C512–12D	t_{ELQV}	t_{CE}	$\overline{G} = V_{IL}$	–	–	120	ns
NTE27C512–15D				–	–	150	ns

Note 4. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Read Mode AC Characteristics (Cont'd): (T_A = 0° to +70°C, V_{CC} = 5V ±5% or 5V ±10%, V_{PP} = V_{CC}, Note 4 unless otherwise specified)

Parameter	Symbol	Alt.	Test Conditions	Min	Typ	Max	Unit
Output Enable Low To Output Valid NTE27C512–12D	t_{GLQV}	t_{OE}	$\overline{E}$ = V_{IL}	–	–	50	ns
NTE27C512–15D				–	–	60	ns
Chip Enable High To Output Hi–Z NTE27C512–12D	t_{EHQZ}	t_{DF}	$\overline{G}$ = V_{IL}, Note 3	0	–	40	ns
NTE27C512–15D				0	–	50	ns
Output Enable High To Output Hi–Z NTE27C512–12D	t_{GHQZ}	t_{DF}	$\overline{E}$ = V_{IL}, Note 3	0	–	40	ns
NTE27C512–15D				0	–	50	ns
Address Transition To Output Transition	t_{AXQX}	t_{OH}	$\overline{E}$ = V_{IL} , $\overline{G}$ = V_{IL}	0	–	–	ns

Note 3. Sampled only, not 100% tested.

Note 4. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Programming Mode DC Characteristics: (T_A = +25°C, V_{CC} = 6.25V ±0.25V, V_{PP} = 12.75V ±0.25V, Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	$V_{IL} \le V_{IN} \le V_{IH}$	–	–	±10	µA
Supply Current	I_{CC}		–	–	50	mA
Program Current	I_{PP}	$\overline{E}$ = V_{IL}	–	–	50	mA
Input Low Voltage	V_{IL}		–0.3	–	0.8	V
Input High Voltage	V_{IH}		2	–	V_{CC}+0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
Output High Voltage, TTL	V_{OH}	I_{OH} = –1mA	3.6	–	–	V
A9 Voltage	V_{ID}		11.5	–	12.5	V

Note 4. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Margin Mode AC Characteristics: (T_A = +25°C, V_{CC} = 6.25V ±0.25V, V_{PP} = 12.75V ±0.25V, Note 4 unless otherwise specified)

Parameter	Symbol	Alt.	Test Conditions	Min	Typ	Max	Unit
V_{A9} High To V_{PP} High	t_{A9HVPH}	t_{AS9}		2	–	–	µs
V_{PP} High To Chip Enable Low	t_{VPHEL}	t_{VPS}		2	–	–	µs
V_{A10} High To Chip Enable High (Set)	t_{A10HEH}	t_{AS10}		1	–	–	µs
V_{A10} Low To Chip Enable High (Reset)	t_{A10HEH}			1	–	–	µs
Chip Enable Transition To V_{A10} Transition	t_{EXA10X}	t_{AH10}		1	–	–	µs
Chip Enable Transition To V_{PP} Transition	t_{EXVPX}	t_{VPH}		2	–	–	µs
V_{PP} Transition To V_{A9} Transition	t_{VPXA9X}	t_{AH9}		2	–	–	µs

Note 4. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Programming Mode AC Characteristics: (T_A = +25°C, V_{CC} = 6.25V ±0.25V, V_{PP} = 12.75V ±0.25V, Note 4 unless otherwise specified)

Parameter	Symbol	Alt.	Test Conditions	Min	Typ	Max	Unit
Address Valid To Chip Enable Low	t_{AVEL}	t_{AS}		2	–	–	μs
Input Valid To Chip Enable Low	t_{QVEL}	t_{DS}		2	–	–	μs
V_{CC} High To Chip Enable Low	t_{VCHEL}	t_{VCS}		2	–	–	μs
V_{PP} High To Chip Enable Low	t_{VPHEL}	t_{OES}		2	–	–	μs
V_{PP} Rise Time	t_{VPLVPH}	t_{PRT}		50	–	–	ns
Chip Enable Program Pulse Width (Initial)	t_{ELEH}	t_{PW}		95	–	105	μs
Chip Enable High To Input Transition	t_{EHQX}	t_{DH}		2	–	–	μs
Chip Enable High To V_{PP} Transition	t_{EHVPX}	t_{OEH}		2	–	–	μs
V_{PP} Low To Chip Enable Low	t_{VPLEL}	t_{VR}		2	–	–	μs
Chip Enable Low To Output Valid	t_{ELQV}	t_{DV}		–	–	1	μs
Chip Enable High To Output Hi–Z	t_{EHQZ}	t_{DFP}	Note 3	0	–	130	ns
Chip Enable High To Address Transition	t_{EHAX}	t_{AH}		0	–	–	ns

Note 3. Sampled only, not 100% tested.

Note 4. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Programming:

When delivered (and after each erasure for UV EPROM), all bits of the NTE27C512 are in the “1” state. Data is introduced by selectively programming “0”s into the desired bit locations. Although only “0”s will be programmed, both “1”s and “0”s can be present in the data word. The only way to change a “0” to a “1” is by die exposure to ultraviolet light (UV EPROM). The NTE27C512 is in the programming mode when V_{PP} input is at 12.75V $\overline{E}$ is pulsed to V_{IL}. The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ±0.25V.

Program Inhibit:

Programming of multiple NTE27C512s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}V_{PP}$ of the parallel NTE27C512 may be common. A TTL low level pulse applied to an NTE27C512’s $\overline{E}$ input, with V_{PP} at 12.75V, will program that NTE27C512. A high level $\overline{E}$ input inhibits the other NTE27C512s from being programmed.

Program Verify:

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

Erasure Operation:

The erasure characteristics of the NTE27C512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000–4000Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical NTE27C512 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NTE27C512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the NTE27C512 window to prevent unintentional erasure.

Erasure Operation (Cont'd):

The recommended erasure procedure for the NTE27C512 is exposure to short wave ultraviolet light-which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15W−sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000μW/cm^2 power rating. The NTE27C512 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Pin Connection Diagram