



PL485 Datasheet

Scope

This document is an overview of the main features of the PL485 microprocessor. The sole reference documents for product information on the PL485 are listed in [Reference Documents](#).

Introduction

The PL485 is a fully programmable Power Line Communication (PLC) System On Chip (SOC). It is able to run any narrowband-PLC (NB-PLC) protocol in the frequency band up to 500 kHz. By means of selecting the proper firmware, the PL485 is able to support applications requiring basic connectivity (point to point, star) or complex PLC networks (mesh topologies with routing).

Microchip provides firmware examples for basic PLC connectivity, as well as implementations of state-of-the-art PLC protocols such as ITU-T G.9903 (G3-PLC[®]) and ITU-T G.9904 (PRIME[®]). The PL485 is a future-proof modem able to support the evolution of the implemented NB-PLC standards.

Reference Documents

Type	Document Title	Available	Ref. No.
Data sheet	PL360 Datasheet	www.microchip.com	70005364
Data sheet	SAM G55J Datasheet	www.microchip.com	11289

Table of Contents

Scope.....	1
Introduction.....	1
Reference Documents.....	1
1. Features.....	3
2. Applications.....	5
3. Block Diagram.....	6
4. Chip Identifier.....	7
5. Package and Ballout.....	8
5.1. Packages.....	8
5.2. Ballout.....	8
5.3. Recommended SAMG55-PL360 Connection.....	10
6. Electrical Characteristics.....	11
6.1. Decoupling.....	11
6.2. Power Sequences.....	11
6.3. Thermal Characteristics.....	11
6.4. Power Consumption.....	11
7. Mechanical Characteristics.....	12
7.1. 121-Ball TFBGA.....	12
8. Recommended Mounting Conditions.....	16
9. Marking.....	17
10. Ordering Information.....	18
11. Revision History.....	19
11.1. Rev A - 12/2019.....	19
11.2. Rev B - 03/2020.....	19
The Microchip Website.....	20
Product Change Notification Service.....	20
Customer Support.....	20
Microchip Devices Code Protection Feature.....	20
Legal Notice.....	20
Trademarks.....	21
Quality Management System.....	21
Worldwide Sales and Service.....	22

1. Features

- Programmable Narrow-Band Power Line Communication (NB-PLC) system on chip
- Complies with FCC, CENELEC, ARIB and K.60 regulations
- Embedded NB-PLC modem:
 - PLC front-end integrated, including PGA and digital transmission level control
 - High performance, programmable engine dedicated to PLC PHY and MAC real-time tasks with dedicated SRAM memory
 - Cryptographic engine supporting AES 128, 192, 256
 - Modem secure boot implemented, comprising PLC binary authentication (AES-128 CMAC) and decryption (AES-128 CBC)
- Fully programmable, standard ARM[®] 32-bit Cortex[®]-M4 core running the upper protocol layers and user application:
 - ARM Cortex-M4 with up to 16 Kbytes SRAM on I/D bus providing 0 wait state execution at up to 100 MHz⁽¹⁾
 - Memory Protection Unit (MPU)
 - DSP Instructions
 - Floating Point Unit (FPU)
 - Thumb[®]-2 instruction set
- Memories:
 - Up to 512 Kbytes embedded Flash
 - Up to 176 Kbytes embedded SRAM
 - 8 Kbytes ROM with embedded boot loader, single-cycle access at full speed
- System:
 - Embedded voltage regulator for single-supply operation
 - Power-on reset (POR) and Watchdog for safe operation
 - Quartz or ceramic resonator oscillators: 3 to 20 MHz with clock failure detection and 32.768 kHz for RTT or system clock
 - High-precision 8/16/24 MHz factory-trimmed internal RC oscillator. In-application trimming access for frequency adjustment
 - Slow clock internal RC oscillator as permanent low-power mode device clock
 - PLL range from 48 MHz to 100 MHz for device clock
 - PLL range from 24 MHz to 48 MHz for USB device and USB OHCI
 - Up to 30 peripheral DMA (PDC) channels
 - 256-bit General-Purpose Backup Registers (GPBR)
 - 15 external interrupt lines
- Peripherals⁽²⁾:
 - 8 flexible communication units supporting:
 - USART
 - SPI
 - Two-wire Interface (TWI) featuring TWI masters and high-speed TWI slaves
 - Crystal-less USB 2.0 Device and USB Host OHCI with On-chip Transceiver
 - 2 Inter-IC Sound Controllers (I2S)
 - 1 Pulse Density Modulation Interface (PDMIC) (supports up to two microphones)
 - 2 three-channel 16-bit Timer/Counters (TC) with capture, waveform, compare and PWM modes
 - 1 48-bit Real-Time Timer (RTT) with 16-bit prescaler and 32-bit counter
 - 1 RTC with calendar and alarm features
 - 1 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)

- I/O⁽²⁾:
 - Up to 48 I/O lines with external interrupt capability (edge or level), debouncing, glitch filtering and on-die series resistor termination. Individually programmable open-drain, pull-up and pull-down resistor and synchronous output
 - Two PIO Controllers provide control of up to 48 I/O lines
- Analog:
 - One 8-channel ADC, resolution up to 12 bits, sampling rate up to 500 ksps
- Package: available in TFBGA-121
- Temperature Range: Industrial (-40°C to +85°C)

Note:

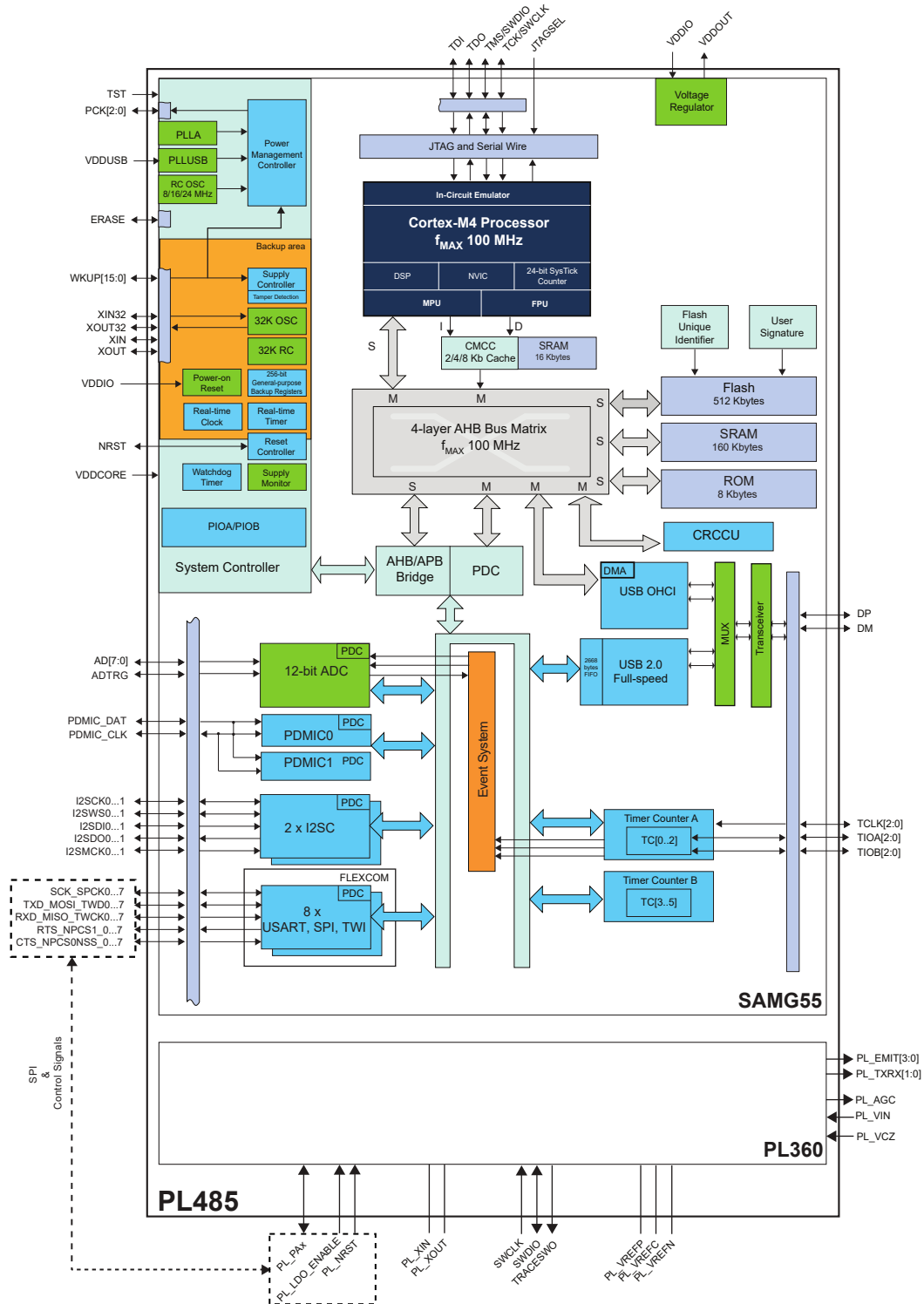
1. 100 MHz with VDDCOREXT100 or with VDDCORE trimmed by regulator.
2. Communication between SAMG55 and PL360 blocks requires some peripherals and GPIOs which will not be available for other uses. Please, refer to section [5.3 Recommended SAMG55-PL360 Connection](#) for more information about connection between SAMG55 and PL360 blocks.

2. Applications

- IoT and Industrial: Smart Lighting, Fire and alarm systems, Solar, Home Automation
- Internet of Energy: Advanced Metering Infrastructure, Smart Grid, Home/Building Energy Management Systems (HEMS/BEMS), Heating, Ventilation and Air Conditioning (HVAC)

3. Block Diagram

Figure 3-1. PL485 Block Diagram



4. Chip Identifier

Table 4-1. Chip ID Registers

Chip Name	CHIPID_CIDR	CHIPID_EXID
SAM G55J19	0x2457_0AE1	0x0

5. Package and Ballout

5.1 Packages

The PL485 is available in the packages listed in the following table:

Table 5-1. PL485 Packages

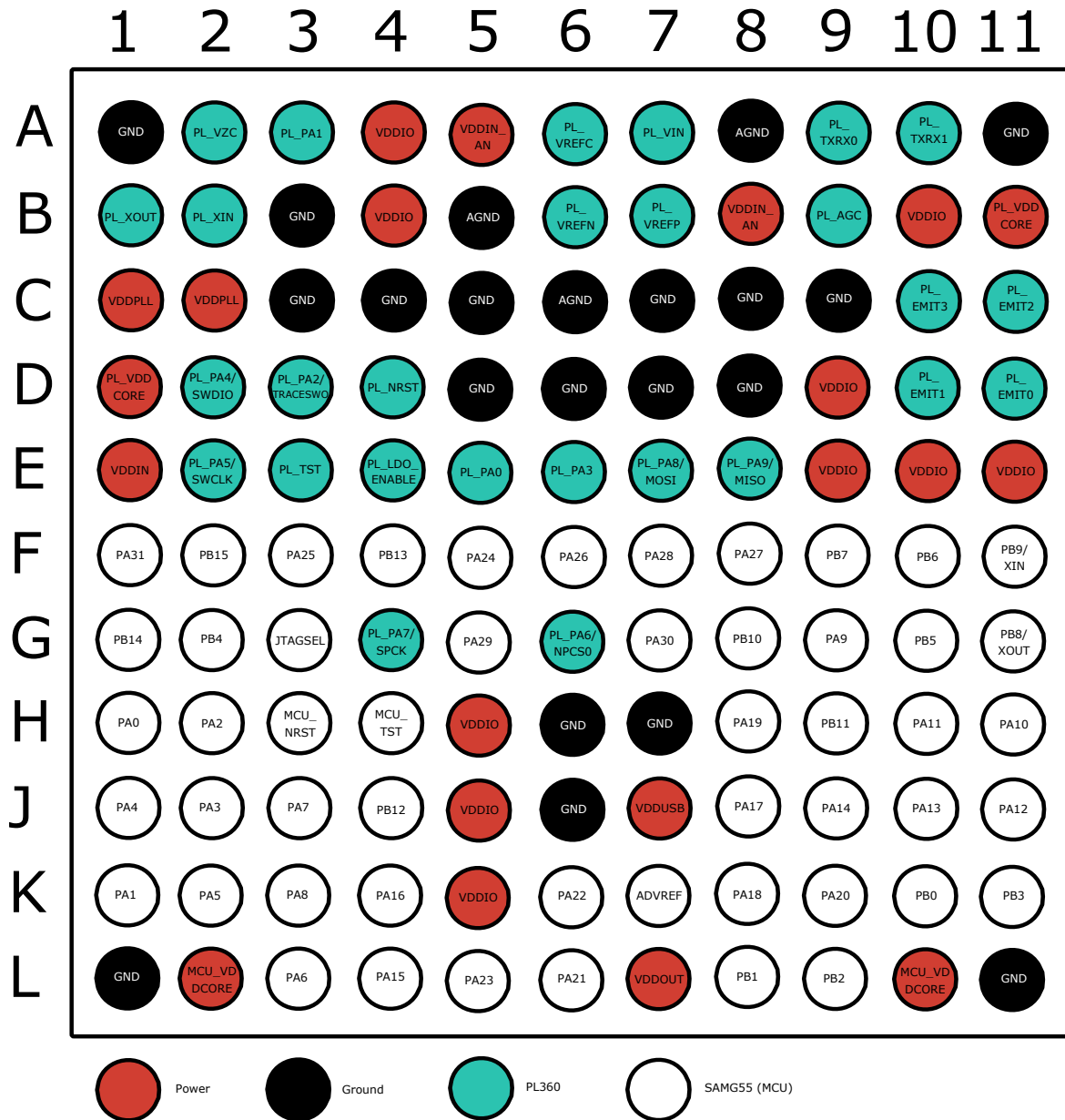
Package Name	Ball Count	Ball Pitch	Package Size
TFBGA121	121	0.80 mm	10 x 10 mm ²

5.2 Ballout

Table 5-2. PL485 Ballout

A1	GND	C3	GND	E5	PL_PA0	G7	PA30	J9	PA14
A2	PL_VZC	C4	GND	E6	PL_PA3	G8	PB10	J10	PA13
A3	PL_PA1	C5	GND	E7	PL_PA8/MOSI	G9	PA9	J11	PA12
A4	VDDIO	C6	AGND	E8	PL_PA9/MISO	G10	PB5	K1	PA1
A5	VDDIN_AN	C7	GND	E9	VDDIO	G11	PB8/XOUT	K2	PA5
A6	PL_VREFC	C8	GND	E10	VDDIO	H1	PA0	K3	PA8
A7	PL_VIN	C9	GND	E11	VDDIO	H2	PA2	K4	PA16
A8	AGND	C10	PL_EMIT3	F1	PA31	H3	MCU_NRST	K5	VDDIO
A9	PL_TXRX0	C11	PL_EMIT2	F2	PB15	H4	MCU_TST	K6	PA22
A10	PL_TXRX1	D1	PL_VDDCORE	F3	PA25	H5	VDDIO	K7	ADVREF
A11	GND	D2	PL_PA4/SWDIO	F4	PB13	H6	GND	K8	PA18
B1	PL_XOUT	D3	PL_PA2/TRACESWO	F5	PA24	H7	GND	K9	PA20
B2	PL_XIN	D4	PL_NRST	F6	PA26	H8	PA19	K10	PB0
B3	GND	D5	GND	F7	PA28	H9	PB11	K11	PB3
B4	VDDIO	D6	GND	F8	PA27	H10	PA11	L1	GND
B5	AGND	D7	GND	F9	PB7	H11	PA10	L2	MCU_VDDCORE
B6	PL_VREFN	D8	GND	F10	PB6	J1	PA4	L3	PA6
B7	PL_VREFP	D9	VDDIO	F11	PB9/XIN	J2	PA3	L4	PA15
B8	VDDIN_AN	D10	PL_EMIT1	G1	PB14	J3	PA7	L5	PA23
B9	PL_AGC	D11	PL_EMIT0	G2	PB4	J4	PB12	L6	PA21
B10	VDDIO	E1	VDDIN	G3	JTAGSEL	J5	VDDIO	L7	VDDOUT
B11	PL_VDDCORE	E2	PL_PA5/SWCLK	G4	PL_PA7/SPCK	J6	GND	L8	PB1
C1	VDDPLL	E3	PL_TST	G5	PA29	J7	VDDUSB	L9	PB2
C2	VDDPLL	E4	PL_LDO_ENABLE	G6	PL_PA6/NPCS0	J8	PA17	L10	MCU_VDDCORE
								L11	GND

Figure 5-1. PL485 Ballout



5.3 Recommended SAMG55-PL360 Connection

The recommended connection in the PCB between balls of the PL485 to connect SAMG55 and PL360 internal blocks is:

Figure 5-2. Recommended SAMG55-PL360 PCB Connection

PL485 Ballout	PL360 Signal		SAMG55 Signal	PL485 Ballout
D4	PL_NRST	←→	PA25	F3
E3	PL_TST	←→	PB15	F2
E4	PL_LDO_ENABLE	←→	PB13	F4
E5	PL_PA0	←→	PA24	F5
E6	PL_PA3	←→	PA26	F6
E7	PL_PA8/MOSI	←→	PA28	F7
E8	PL_PA9/MISO	←→	PA27	F8
G4	PL_PA7/SPCK	←→	PA29	G5
G6	PL_PA6/NPCS0	←→	PA30	G7

This connection is configured by default in Microchip Powerline communication stacks. It is highly recommended to keep it as specified by this datasheet to guarantee proper operation of the PLC modem.

6. Electrical Characteristics

Please refer to PL360 and SAM G55J Datasheets for specific information about Electrical Characteristics.

6.1 Decoupling

For correct PLC transmission, a 4.7 μF decoupling capacitor must be added to each of the following VDDIO balls: D9, E9, E10 and E11.

Please refer to the reference datasheets for other Decoupling Requirements.

6.2 Power Sequences

Please refer to the reference datasheets for Power Sequences Considerations.

6.3 Thermal Characteristics

Table 6-1. Thermal Resistance Data

Symbol	Parameter	Condition	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	31.1	$^{\circ}\text{C}/\text{W}$
		1m/s	21.9	
		2m/s	19.6	
ψ_{JC}	Junction-to-top center of package thermal characterization	-	1.9	

θ_{JA} is calculated based on a standard JEDEC JESD51-5 defined environment (1.6mm thickness PCB, 4 copper layers, 76.2mm x 114.3mm board) and is not reliable indicator of a device's thermal performance in a non-JEDEC environment. The customer should always perform their own calculations/simulations to ensure that their system's thermal performance is sufficient.

6.4 Power Consumption

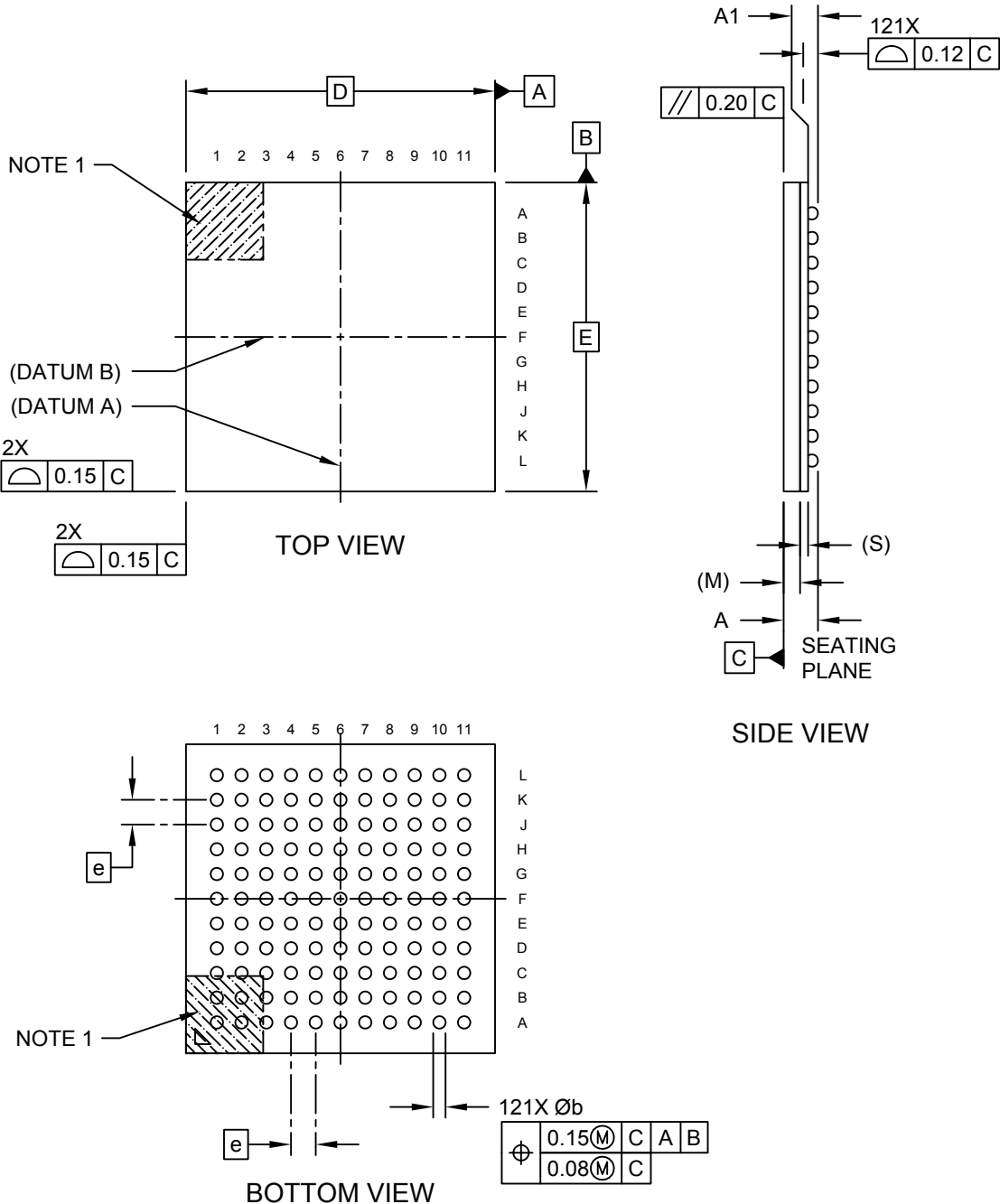
Please refer to the reference datasheets for Power Consumption.

7. Mechanical Characteristics

7.1 121-Ball TFBGA

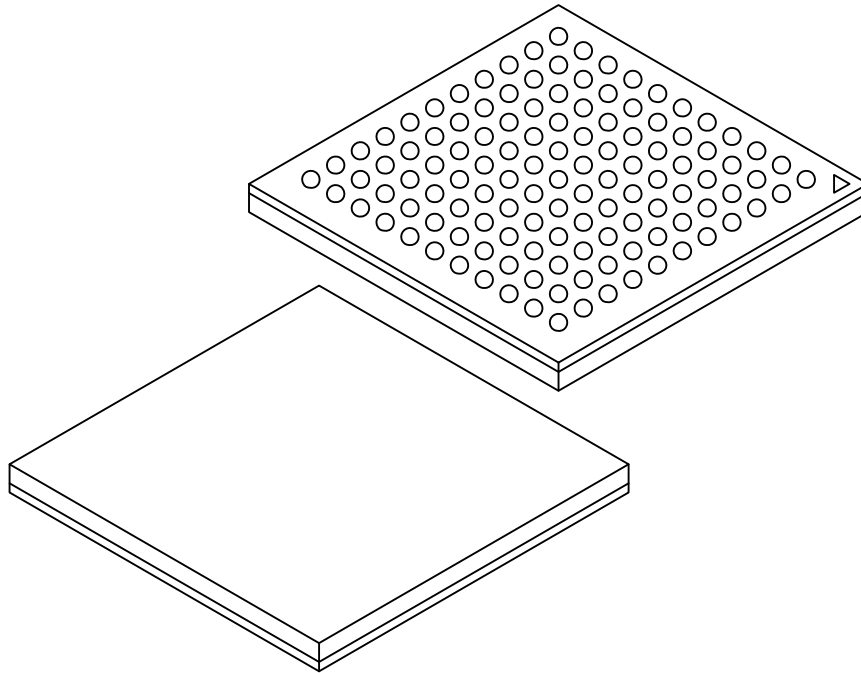
121-Ball Thin, Fine Pitch Ball Grid Array (AJA) - 10x10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



121-Ball Thin, Fine Pitch Ball Grid Array (AJA) - 10x10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	121		
Pitch	e	0.80 BSC		
Overall Height	A	-	-	1.20
Terminal (ball) height	A1	0.270	-	0.37
Substrate Thickness	S	0.26 REF		
Mold Cap Thickness	M	0.53 REF		
Overall Length	D	10.00 BSC		
Overall Width	E	10.00 BSC		
Terminal Width	b	0.38	0.40	0.48

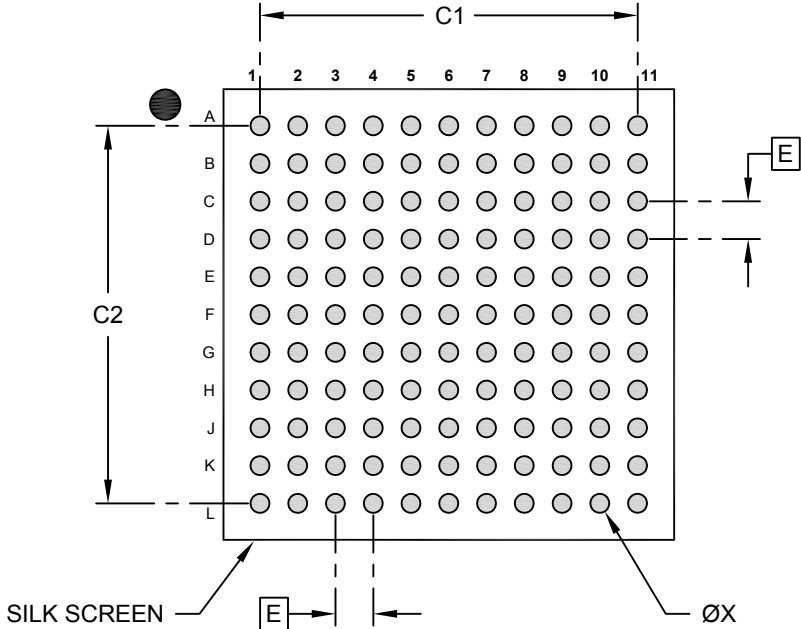
Notes:

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1216A Sheet 2 of 2

121-Ball Thin, Fine Pitch Ball Grid Array (AJA) - 10x10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.40

- Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3216A

Table 7-1. 121-Ball TFBGA Package Characteristics

Moisture Sensitivity Level	3
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Table 7-2. Package Reference

JEDEC Drawing Reference	NA
J-STD-609 Classification	e8

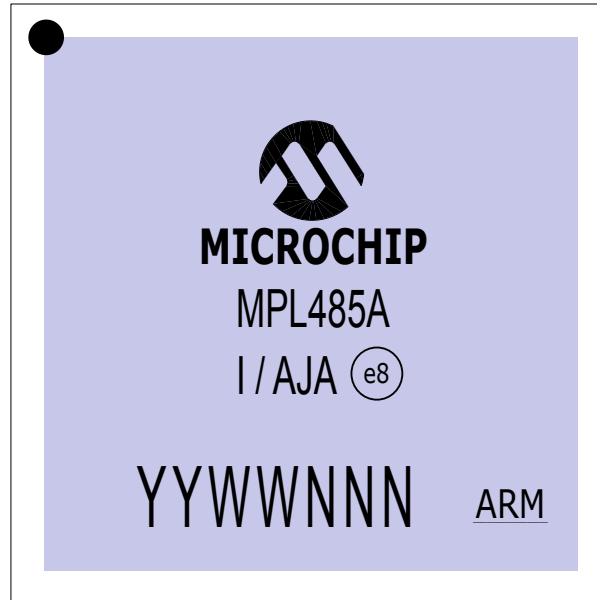
8. Recommended Mounting Conditions

Please refer to [AN233](#) application note in Microchip Web for more information.

9. Marking

All devices are marked with the Microchip logo and the ordering code.

Figure 9-1. TFBGA Marking



Where:

- M: Microchip logo
- MPL485A: Product name
- e8: Jedec code
- YYWWNNN: Traceability code
- ARM: ARM logo

10. Ordering Information**Table 10-1. Ordering Information**

Ordering Code	Package	Carrier Type	Package Type	Temperature Range
MPL485A-I/AJA	121 TFBGA	Tray	Pb-Free	Industrial (-40°C to 85°C)
MPL485AT-I/AJA	121 TFBGA	Tape and Reel	Pb-Free	Industrial (-40°C to 85°C)

11. Revision History

11.1 Rev A - 12/2019

Document	Initial release.
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11.2 Rev B - 03/2020

1. Features	Minor changes
5. Package and Ballout	Minor changes in 5.3 Recommended SAMG55-PL360 Connection section.
Document	Added section 6.3 Thermal Characteristics . Added section 6.4 Power Consumption .

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