



RT600

Dual-core microcontroller with 32-bit Cortex[®]-M33 and Xtensa HiFi4 Audio DSP CPUs; Up to 4.5 MB SRAM; FlexSPI with cache and dynamic decryption; High-speed USB device/host + Phy; 12-bit 1 Msamples/s ADC; Analog Comparator; Audio subsystems supporting up to 8 DMIC channels; SDIO/eMMC; AES/SHA/Crypto M33 coprocessor; PUF key generation

Rev. 1.1 — 3 March 2020

Product data sheet

1. General description

The RT600 is a family of dual-core microcontrollers for embedded applications featuring an Arm Cortex-M33 CPU combined with a Cadence Xtensa HiFi4 advanced Audio Digital Signal Processor CPU. The Cortex-M33 includes two hardware coprocessors providing enhanced performance for an array of complex algorithms. The family offers a rich set of peripherals and very low power consumption.

The Arm Cortex-M33 is a next generation core based on the ARMv8-M architecture that offers system enhancements, such as ARM TrustZone[®] security, single-cycle digital signal processing, and a tightly-coupled coprocessor interface, combined with low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M33 CPU employs a 3-stage instruction pipe and includes an internal prefetch unit that supports speculative branching. A hardware floating-point processor is integrated into the core. On the RT600, the Cortex-M33 is augmented with two hardware coprocessors providing accelerated support for additional DSP algorithms and cryptography.

The Cadence Xtensa HiFi 4 Audio DSP engine is a highly optimized audio processor designed especially for efficient execution of audio and voice codecs and pre- and post-processing modules. It supports four 32x32-bit MACs, some support for 72-bit accumulators, limited ability to support eight 32x16-bit MACs, and the ability to issue two 64-bit loads per cycle. There is a floating point unit providing up to four single-precision IEEE floating point MACs per cycle.

The RT600 provides up to 4.5 MB of on-chip SRAM (plus an additional 128 KB of tightly-coupled HiFi4 ram) and several high-bandwidth interfaces to access off-chip flash. The FlexSPI flash interface supports two channels and includes a 32 KB cache and an on-the-fly decryption engine. The RT600 is designed to allow the Cortex-M33 to operate at frequencies of up to 300 MHz and the HiFi4 DSP to operate at frequencies of up to 600 MHz.

1.1 Peripherals

The peripheral complement includes a FlexSPI flash interface with two channels, two SDIO/eMMC interfaces, a high-speed USB device/host with on-chip PHY, a 12-bit, 1 MSamples/sec ADC with temperature sensor, an analog comparator, AES256 and Hash engines with Physical Unclonable Function (PUF) key generation, a digital microphone



interface supporting up to eight channels and Voice Activation Detect, one I3C interface, one high-speed SPI interface and seven configurable serial interfaces that can be configured as a USART, SPI, I2C or I2S bus interface, each including a FIFO. When configured as USARTs the serial interfaces have the option to operate in deep-sleep mode using the 32 kHz oscillator or an external clock. There is a dedicated fractional baud rate generator for each of the serial interfaces.

Timing peripherals include one advanced, 32-bit SCTimer/PWM module, five general purpose 32-bit timer/counters with PWM capability, a 24-bit, multiple-channel multi-rate timer, two windowed watchdog timers, a system tick timer with capture capability, and a Real-time clock module with independent power and a dedicated oscillator. A common OS Event Timer is provided for synchronized event generation and timestamping between the two CPUs.

There are two general purpose DMA engines which can service most of the peripherals described in this section. The two DMA engines may be assigned to different CPUs and/or one may be used for secure operations, the other for non-secure.

Mailboxes and hardware semaphores are provided to facilitate inter-core communication. A variety of oscillators and PLLs are available as clock sources throughout the system.

1.2 Shared system SRAM

The entire system SRAM space of up to 4.5 MB is divided into up to 30 separate partitions, which are accessible to both CPUs, both DMA engines, and all other AHB bus masters. The HiFi4 CPU accesses the RAM via a dedicated 256-bit interface. Cache (with single-cycle access) is provided on this interface to improve performance. All other masters, including the Cortex-M33 processor and the DMA engines, access RAM via the main 32-bit AHB bus. These accesses are all single-cycle. Hardware interface modules arbitrate access to each RAM partition between the HiFi4 and the AHB bus.

Under software control, each of the 30 individual SRAM partitions can be used exclusively as code or as data, dedicated either CPU, or shared among the various masters. Each partition can be independently placed in a low-power retention mode or powered off entirely.

In addition to the shared SRAM, a total of 128 KB (64 KB code, 64 KB data) of local, Tightly-Coupled Memory (TCM) is provided for the exclusive use of the HiFi4 DSP processor. Access to this memory is single-cycle.

2. Features and benefits

- Control processor core
 - ◆ Arm Cortex-M33 processor, running at frequencies of up to 300 MHz.
 - ◆ Arm TrustZone.
 - ◆ Arm Cortex-M33 built-in Memory Protection Unit (MPU) supporting eight regions
 - ◆ Hardware Floating Point Unit (FPU).
 - ◆ Arm Cortex-M33 built-in Nested Vectored Interrupt Controller (NVIC).
 - ◆ Non-maskable Interrupt (NMI) input.

- ◆ Two coprocessors for the Cortex-M33: a hardware accelerator for fixed and floating point DSP functions (PowerQuad) and a Crypto/FFT engine (Casper). The DSP coprocessor uses a bank of four dedicated 2 KB SRAMs. The Crypto/FFT engine uses a bank of two 2 KB SRAMs that are also AHB accessible by the CPU and the DMA engine.
- ◆ Serial Wire Debug with eight break points, four watch points, and a debug timestamp counter. It includes Serial Wire Output (SWO) trace and ETM trace.
- ◆ Cortex-M33 System tick timer.
- DSP processor core:
 - ◆ Cadence Xtensa HiFi4 Audio DSP processor, running at frequencies of up to 600 MHz.
 - ◆ Hardware Floating Point Unit. Up to four single-precision IEEE floating point MACs per cycle.
 - ◆ Serial Wire Debug (shared with Cortex-M33 Control Domain CPU).
 - ◆ System tick timer.
- Triple I/O power:
 - ◆ Three independent supplies powering different clusters of pins to permit interfacing directly to off-chip peripherals operating at different supply levels.
- On-chip Memory:
 - ◆ Up to 4.5 MB of system SRAM accessible by both CPUs and all (dedicated and general purpose) DMA engines.
 - ◆ 128 KB of local, Tightly-Coupled Memory dedicated to the DSP CPU.
 - ◆ 96 KB (or more) of I & D cache for DSP accesses to shared system SRAM.
 - ◆ Additional SRAMs for USB traffic (8 KB), Cortex-M33 coprocessors (4 x 2 KB), SDIO FIFOs (2 x 512 B dual-port), PUF secure key generation (2 KB), and FlexSPI cache (32 KB).
 - ◆ 16 K bits of OTP fuses for factory and user configuration.
 - ◆ Up to 256 KB ROM memory for factory-programmed drivers and APIs.
 - ◆ System boot from SPI, I2C, UART, Octal/Quad SPI Flash, HS USB or eMMC via on-chip bootloader software included in ROM.
- Digital peripherals:
 - ◆ Two general purpose DMA engines, each with 32 channels and up to 25 programmable request/trigger sources.
 - Can be configured such that one DMA is secure and the other non-secure and/or one can be designated for use by the M33 CPU and the other by the DSP.
 - ◆ USB high-speed host/device controller with on-chip PHY and dedicated DMA controller.
 - ◆ FlexSPI flash interface with 32 KB cache and dynamic decryption for execute-in-place and supports DMA. The FlexSPI includes 2 ports: high speed channel A and lower speed channel B. Both ports support quad or octal operation.
 - ◆ An SD/eMMC memory card interface with dedicated DMA controller. Supports eMMC 5.0 with HS400/DDR operation (HS-400 is supported only on SD port 0).
 - ◆ Eight configurable universal serial interface modules (Flexcomm Interfaces). Each module contains an integrated FIFO and DMA support. Flexcomms 0 through 7 can be configured as:
 - A USART with dedicated fractional baud rate generation and flow-control handshaking signals. The USART can optionally be clocked at 32 kHz and

operated when the chip is in reduced power mode, using either the 32 kHz clock or an externally supplied clock. The USART also provides partial support for LIN2.2.

- An I²C-bus interface with multiple address recognition, and a monitor mode. It supports 400 Kb/sec Fast-mode and 1 Mb/sec Fast-mode Plus. It also supports 3.4 Mb/sec high-speed when operating in slave mode.
- An SPI interface.
- An I²S (Inter-IC Sound) interface for digital audio input or output. Each I²S supports up to four channel-pairs.
- ◆ One high-speed SPI interface (Flexcomm Interface 14 only) supporting 50 MHz operation.
- ◆ One additional I2C interface available on some device configurations (see specific device data sheet for more information). This interface is intended primarily for communication with an external power management device (PMIC), but can be used for other purposes when the application does not use an external PMIC.
- ◆ One I3C bus interface.
- ◆ One eSPI interface.
- ◆ A digital microphone interface supporting up to 8 channels with associated decimators and Voice Activation Detect. One pair of channels can be streamed directly to I²S. The DMIC supports DMA.
- ◆ One 32-bit SCTimer/PWM module (SCT). Multi-purpose timer with extensive event-generation, match/compare, and complex PWM and output control features.
 - Supports DMA and can trigger external DMA events.
 - Supports fractional match values for high resolution.
 - State machine capability.
 - 8 general-purpose inputs.
 - 10 general-purpose/PWM outputs
 - 16 matches or captures
 - 16 events
 - 32 states
- ◆ Five general purpose, 32-bit timer/counter modules with PWM capability.
 - Each timer supports four match outputs and four capture inputs.
 - Match register auto-reload from shadow registers.
 - It supports DMA and can trigger external DMA events.
- ◆ 24-bit multi-rate timer module with four channels, each capable of generating repetitive interrupts at different programmable frequencies.
- ◆ Two Windowed Watchdog Timers (WDT) with dedicated watchdog oscillator.
- ◆ Frequency measurement module to determine the frequency of a selection of on-chip or off-chip clock sources.
- ◆ Real-Time Clock (RTC) with independent power supply and dedicated oscillator. Integrated wake-up timer can be used to wake the device up from low-power modes. The RTC includes eight 32-bit general purpose registers which can retain content when power is removed from the rest of the chip.
- ◆ Ultra-low power micro-tick timer running from the watchdog oscillator with capture capability for timestamping. Can be used to wake the device up from low-power modes.
- ◆ 64-bit OS Event Timer common to the Cortex-M33 and DSP processors with individual match/capture and interrupt generation logic.
- ◆ CRC engine block can calculate a CRC on supplied data using one of three standard polynomials. The CRC engine supports DMA.

- ◆ AES256 encryption module. The Random Number Generator can be used to create keys. Key storage is in OTP. The AES supports DMA.
- ◆ Physical Unclonable Function (PUF) key generation module.
- ◆ SHA1/SHA2 Secure Hash Algorithm module. Supports secure boot, uses a dedicated DMA controller.
- ◆ Cryptography hardware coprocessor attached to Cortex-M33 CPU.
- Analog peripherals:
 - ◆ One 12-bit ADC with sampling rates of 1 Msamples/sec and an enhanced ADC controller. It supports up to 12 single-ended channels or 6 differential channels. The ADC supports DMA.
 - ◆ Temperature sensor.
 - ◆ Analog comparator.
- I/O peripherals:
 - ◆ Up to 147 general purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors. Ports can be written as words, half-words, bytes, or bits. The number of GPIOs depends on the device package.
 - ◆ Individual GPIO pins can be used as edge and level sensitive interrupt sources, each with its own interrupt vector.
 - ◆ All port0 and port1 GPIO pins can contribute to a one of two GPIO interrupts, with selection of polarity and edge vs level triggering.
 - ◆ A group of up to 8 GPIO pins can be selected for boolean pattern matching, which can generate interrupts and/or drive a pattern-match output.
 - ◆ Adjustable output drivers.
 - ◆ JTAG boundary scan.
- Clock generation unit:
 - ◆ Crystal oscillator with an operating range of 1 MHz to 25 MHz.
 - ◆ Internal 48 or 60 MHz IRC oscillator. Trimmed to $\pm 1\%$ accuracy.
 - ◆ Internal 16 MHz IRC oscillator. Trimmed to $\pm 3\%$ accuracy.
 - ◆ Internal 1 MHz low-power oscillator with 10% accuracy. Serves as the watchdog oscillator and clock for the OS Event Timer and the SysTick. Also available as the system clock.
 - ◆ 32 kHz real-time clock (RTC) oscillator that can optionally be used as a system clock.
 - ◆ Selectable on-chip crystal load capacitors.
 - ◆ Main System PLL:
 - Allows CPU operation up to the maximum rate without the need for a high frequency crystal. May be run from the 16 MHz IRC, the 48/60 MHz IRC, or the crystal.
 - Second PLL output using an independent fractional divider provides an alternate high-frequency clock source for the DSP CPU if the required frequency differs from the main system clock.
 - Two additional PLL outputs, each using independent fractional dividers, providing alternative clock input sources to a number of peripherals.
 - ◆ Audio PLL for the audio subsystem.
 - ◆ 480 MHz USB PLL (internal to the USB PHY).
 - ◆ Clock output function with divider that can reflect any of the internal clock sources.
- Power control:

- ◆ Main power supply is 1.8 V +/- 5%.
- ◆ Analog supply is 1.71 V - 3.6 V.
- ◆ Triple VDDIO supplies (can be shared or independent): 1.71 V - 3.6 V.
- ◆ USB Supply: 3.0 V - 3.6 V.
- ◆ Reduced power modes:
 - Sleep mode: Clock shut down for each CPU independently.
 - Deep-sleep mode: User selectable configuration via PDSLEEPCFG.
 - Deep power-down mode: Power removed from the entire chip except in the always-on domain.
 - Full deep power-down mode: same as deep power-down mode, but external power can be removed (except for VDD_AO18).
 - Each individual SRAM partition can be independently powered-off or put into a low-power retain mode. Individual SRAMs can also have their clocks stopped when not actually in use in order to save power.
 - Ability to operate the synchronous serial interfaces in sleep or deep-sleep mode as a slave or USART clocked by the 32 kHz RTC oscillator.
 - Wake-up from low-power modes via interrupts from various peripherals including the RTC and the OS/Event timer.
- ◆ RBB/FBB to provide additional control over power/performance trade-offs.
- ◆ Power-On Reset (POR).
- Operating temperature range -20 °C to +70 °C
- Available in VFBGA176, WLCSP114, and FOWLP249 packages.

3. Applications

■ Consumer

■ Audio

4. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-----------------|----------|--|-----------|
| | Name | Description | Version |
| MIMXRT685SFFOB | FOWLP249 | Fan-Out Wafer-Level Packaging; 249 balls; 7 x 7 x 0.76 mm | SOT2003-1 |
| MIMXRT685SFVKB | VFBGA176 | thin fine-pitch ball grid array package; 176 balls; body 9 x 9 x 0.98 mm | SOT1850-1 |
| MIMXRT685SFAWBR | WLCSP114 | wafer level chip-size package; 114; 4.235 x 4.235 x 0.525 mm | SOT2019 |
| MIMXRT633SFFOB | FOWLP249 | Fan-Out Wafer-Level Packaging; 249 balls; 7 x 7 x 0.76 mm | SOT2003-1 |
| MIMXRT633SFVKB | VFBGA176 | thin fine-pitch ball grid array package; 176 balls; body 9 x 9 x 0.98 mm | SOT1850-1 |
| MIMXRT633SFAWBR | WLCSP114 | wafer level chip-size package; 114; 4.235 x 4.235 x 0.525 mm | SOT2019 |

4.1 Ordering options

Table 2. Ordering options 4

| Type number | Package Name | M33 | HiFi4 DSP | SRAM/MB | Security Features | FlexSPI A Interface | FlexSPI B Interface | RTC | USB ISP mode ^[1] | Flexcomm Interfaces (0 to 7) | High Speed SPI (Flexcomm 14) | PMIC I2C (Flexcomm 15) ^[3] | GPIO |
|-----------------|--------------|-----|-----------|---------|-------------------|---------------------|---------------------|-----|-----------------------------|------------------------------|------------------------------|---------------------------------------|------|
| MIMXRT685SFFOB | FOWLP249 | Yes | Yes | 4.5 | Yes | Yes | Yes | Yes | Yes | 8 | Yes | Yes | 147 |
| MIMXRT685SFVKB | VFBGA176 | Yes | Yes | 4.5 | Yes | Yes | Yes | Yes | Yes | 6 | Yes | Yes | 96 |
| MIMXRT685SFAWBR | WLCSP114 | Yes | Yes | 4.5 | Yes | Yes | No | No | No | 7 ^[2] | Yes | No | 65 |
| MIMXRT633SFFOB | FOWLP249 | Yes | Yes | 3 | Yes | Yes | Yes | Yes | Yes | 8 | Yes | Yes | 147 |
| MIMXRT633SFVKB | VFBGA176 | Yes | No | 3 | Yes | Yes | Yes | Yes | Yes | 6 | Yes | Yes | 96 |
| MIMXRT633SFAWBR | WLCSP114 | Yes | No | 3 | Yes | Yes | No | No | No | 7 ^[2] | Yes | No | 65 |

- [1] On WLCSP114 package, USB ISP mode is not supported. VBUS pin is not available on the WLCSP114 package. To detect VBUS connection, user can connect a GPIO pin to the USB connector's VBUS. When a rising edge occurs on the GPIO pin, software should set bit 10 (FORCE_VBUS) and bit 16 (DCON) in the DEVCMDSTAT register.
- [2] On WLCSP114 package, Flexcomm interface 6 can only be used as UART peripheral or I2C peripheral
- [3] This interface is intended primarily for communication with an external power management device (PMIC), but can be used for other purposes when the application does not use an external PMIC.

5. Marking

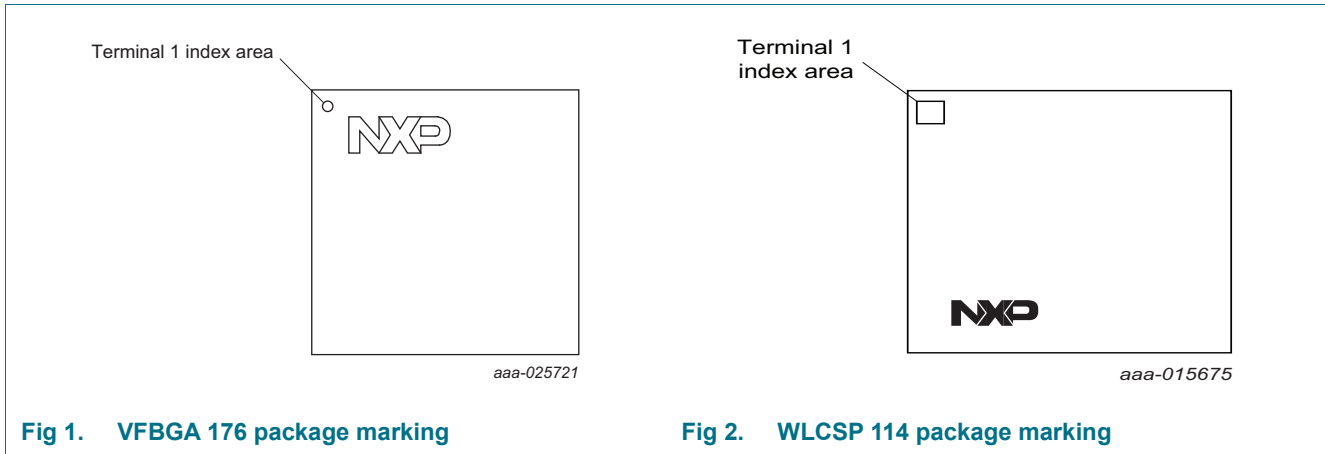


Fig 1. VFBGA 176 package marking

Fig 2. WLCSP 114 package marking

The MIMXRT6xxSFAWBR WLCSP114 production samples has the following top-side package marking:

- First line: MRT6xxSFAW[R]R
- Second line: xxxxxx xx
- Third line: xxxxyyww
- Fourth line: xxx-xxx
 - yyww: Date code with yy = year and ww = week

The MIMXRT6xxSFVKB VFBGA176 production samples has the following top-side package marking:

- First line: MRT6xxSFV
- Second line: K[R] xxxx
- Third line: xyyww
- Fourth line: xxxxx
 - yyww: Date code with yy = year and ww = week

The MIMXRT6xxSFFOB FOWLP249 production samples has the following top-side package marking:

- First line: MRT6xxSFFOB
- Second line: xxxxxx
- Third line: xxxxxx
- Fourth line: xxxxyyww
 - yyww: Date code with yy = year and ww = week

Table 3. Device revision table

| Revision identifier | Revision description [R] |
|---------------------|--------------------------|
| B | Initial device revision |

6. Block diagram

Figure 3, Figure 4, and Figure 5 shows the RT600 block diagram. On Figure 4, shaded blocks support general purpose DMA or blocks include dedicated DMA control.

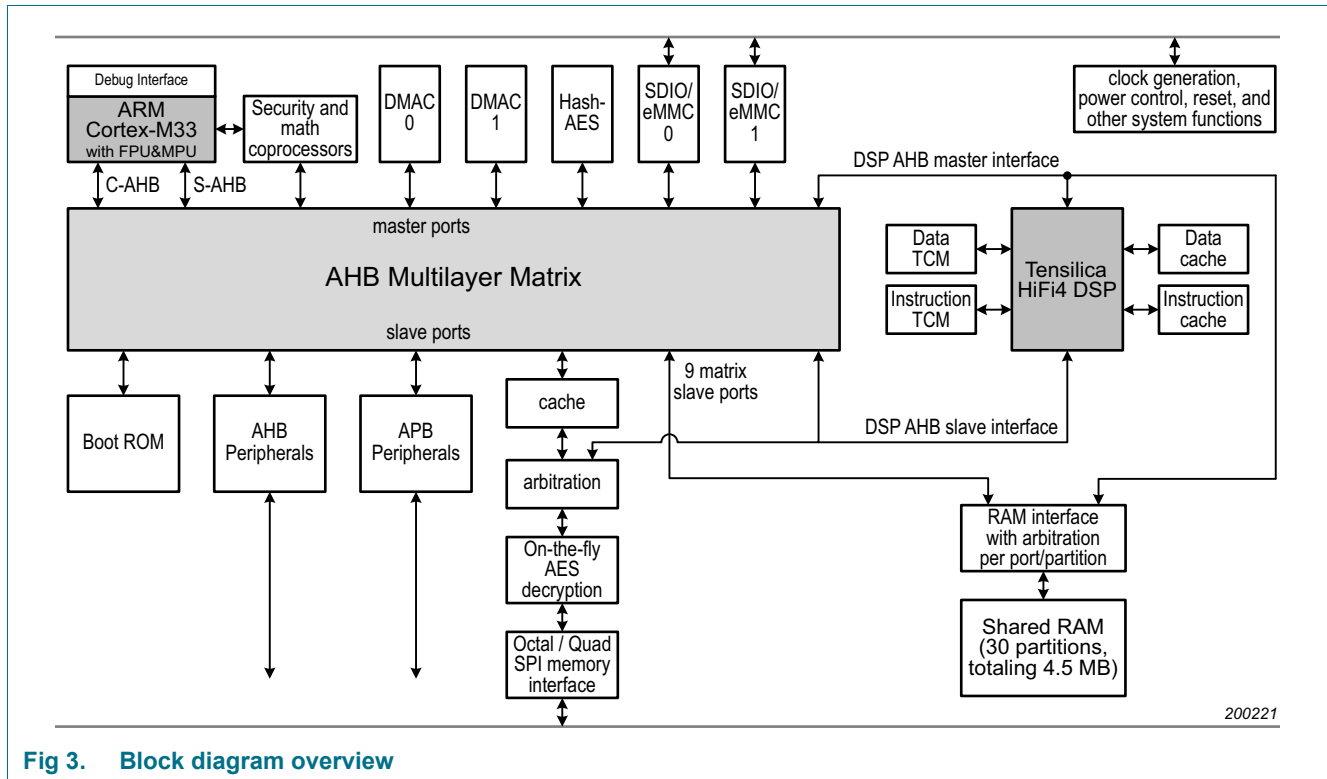


Fig 3. Block diagram overview

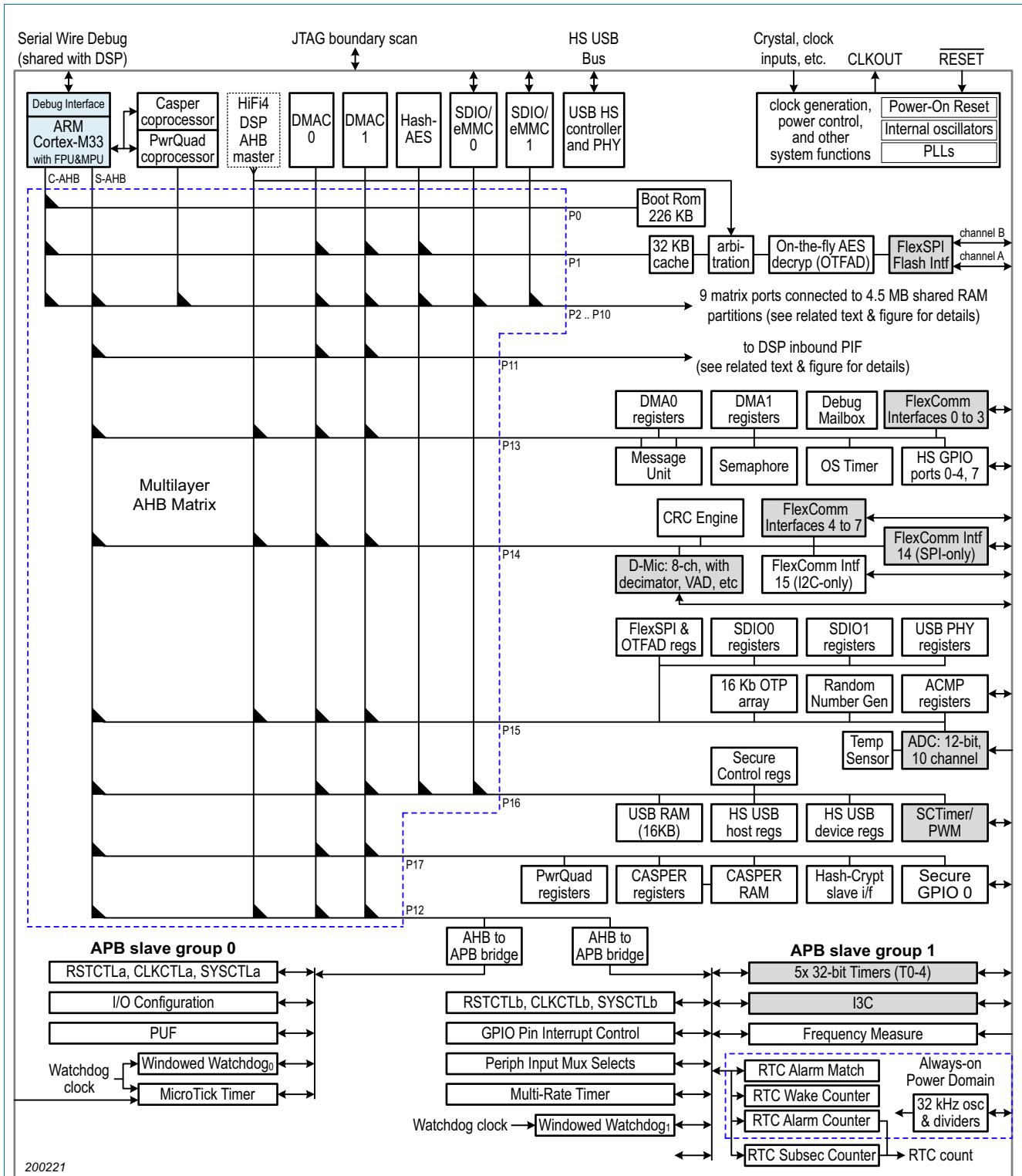


Fig 4. Block diagram - Cortex-M33 view (Not all features are available in all packages. Flexcomm Interfaces 0 through 7 each include USART, SPI, I2C, and I2S functions. Grey-shaded blocks indicate peripherals that provide DMA requests or are otherwise able to trigger DMA transfers. Hash-AES and SDIO include a dedicated DMA function.)

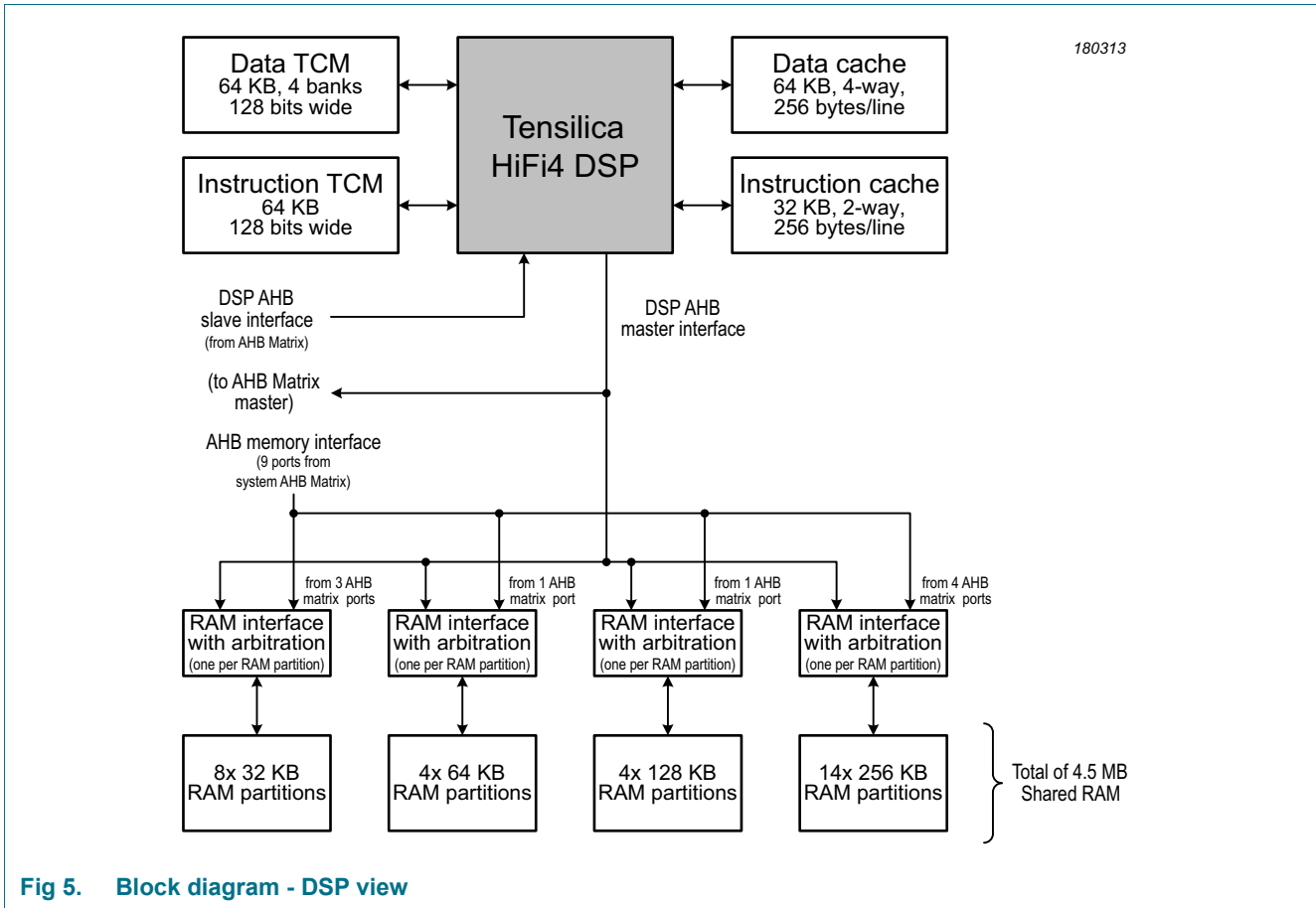


Fig 5. Block diagram - DSP view

7. Pinning information

[Table 4](#) shows the pin functions available on each pin, and for each package. These functions are selectable using IOCON control registers.

Some functions, such as ADC or comparator inputs, are available only on specific pins when digital functions are disabled on those pins. By default, the GPIO function is selected except on pins PIO2_25 and PIO2_26, which are the serial wire debug pins. This allows debug to operate through reset.

All GPIO pins have all pull-ups and pull-downs turned off at reset. This prevents power loss through pins prior to software configuration. All GPIO pins are fail safe up to 3.6 V when VDDIO supply = 0 V except following pins (PIO1_19 to PIO1_31, PIO2_0 to PIO2_8, PIO0_21, PIO0_22, PIO_23 pins).

The state of pins PIO1_15, PIO1_16, and PIO1_17 at Reset determine the boot source for the part or if the ISP handler is invoked.

The JTAG functions TRST, TCK, TMS, TDI, and TDO, are selected on pins PIO0_7 to PIO0_11 by hardware when the part is in boundary scan mode.

Table 4. Pin description

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|--------|----------------|----------------|----------------|---------------------|---------------------------------|------|------------|--|
| | | | | | | | | |
| PIO0_0 | H3 | G1 | H17 | [2] | Z | I/O | 0 | PIO0_0 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FC0_SCK — Flexcomm 0: USART, SPI, or I2S clock. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER0_MAT0 — 32-bit CTimer0 match output 0. |
| | | | | | | | 5 | I2S_BRIDGE_CLK_IN — Allows I2S bypass by re-routing this function to a pin that includes the I2S_BRIDGE_CLK_OUT function. |
| | | | | | | | 6 | GPIO_INT_BMAT — Output of the pin interrupt pattern match engine. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_0 — Secure GPIO pin. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|--------|----------------|----------------|----------------|--|-----------------|------|------------|--|
| | | | | | | | | |
| PIO0_1 | H2 | G2 | H16 | | Z | I/O | 0 | PIO0_1 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC0_TXD_SCL_MISO_WS — Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved |
| | | | | | | O | 4 | CTIMER0_MAT1 — 32-bit CTimer0 match output 1. |
| | | | | | | I | 5 | I2S_BRIDGE_WS_IN — Allows I2S bypass by re-routing this function to a pin that includes the I2S_BRIDGE_WS_OUT function. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved |
| | | | | | | I/O | 8 | SEC_PIO0_1 — Secure GPIO pin. |
| PIO0_2 | F5 | G4 | H15 | | Z | I/O | 0 | PIO0_2 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC0_RXD_SDA_MOSI_DATA — Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER0_MAT2 — 32-bit CTimer0 match output 2. |
| | | | | | | I | 5 | I2S_BRIDGE_DATA_IN — Allows I2S bypass by re-routing this function to a pin that includes the I2S_BRIDGE_DATA_OUT function. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved |
| | | | | | | I/O | 8 | SEC_PIO0_2 — Secure GPIO pin. |
| PIO0_3 | F4 | H2 | H14 | | Z | I/O | 0 | PIO0_3 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC0_CTS_SDA_SSEL0 — Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER0_MAT3 — 32-bit CTimer0 match output 3. |
| | | | | | | I/O | 5 | FC1_SSEL2 — Flexcomm 1: SPI slave select 2. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved |
| | | | | | | I/O | 8 | SEC_PIO0_3 — Secure GPIO pin. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|-------------------|----------------|----------------|--------------------------------------|-----|-----------------|------|------------|--|
| | | | | | | | | |
| PIO0_4 | G1 | J1 | K17 | [2] | Z | I/O | 0 | PIO0_4 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC0_RTS_SCL_SSEL1 — Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | I | 4 | CTIMER_INP0 — Capture input 0 to CTIMER input muxes. |
| | | | | | | I/O | 5 | FC1_SSEL3 — Flexcomm 1: SPI slave select 3. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | O | 7 | CMP0_OUT — Analog comparator 0 output. |
| | I/O | 8 | SEC_PIO0_4 — Secure GPIO pin. | | | | | |
| PIO0_5/ ADC0_0 | J3 | F4 | F16 | [3] | Z | I/O | 0 | PIO0_5/ADC0_0 — General-purpose digital input/output pin. ADC input channel 0 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | I/O | 1 | FC0_SSEL2 — Flexcomm 0: SPI slave select 2. |
| | | | | | | I | 2 | SCT0_GPI0 — Pin input 0 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT0 — SCTimer/PWM output 0. |
| | | | | | | I | 4 | CTIMER_INP1 — Capture input 1 to CTIMER input muxes. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | I/O | 8 | SEC_PIO0_5 — Secure GPIO pin. | | | | | |
| PIO0_6/ ADC0_8 | J1 | E1 | F17 | [3] | Z | I/O | 0 | PIO0_6/ADC0_8 — General-purpose digital input/output pin. ADC input channel 8 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | I/O | 1 | FC0_SSEL3 — Flexcomm 0: SPI slave select 3. |
| | | | | | | I | 2 | SCT0_GPI1 — Pin input 1 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT1 — SCTimer/PWM output 1. |
| | | | | | | O | 4 | CTIMER0_MAT0 — 32-bit CTimer0 match output 0. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | I/O | 8 | SEC_PIO0_6 — Secure GPIO pin. | | | | | |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|-----------------|----------------|--------------------------------------|----------------|-----|-----------------|------|------------|---|
| PIO0_7/ TRST | F3 | J2 | J15 | [2] | Z | I/O | 0 | PIO0_7 — General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset). |
| | | | | | | I/O | 1 | FC1_SCK — Flexcomm 1: USART, SPI, or I2S clock. |
| | | | | | | I | 2 | SCT0_GPI4 — Pin input 4 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT4 — SCTimer/PWM output 4. |
| | | | | | | O | 4 | CTIMER1_MAT0 — 32-bit CTimer1 match output 0. |
| | | | | | | O | 5 | I2S_BRIDGE_CLK_OUT — Allows I2S bypass by re-routing a pin that includes the I2S_BRIDGE_CLK_IN function to this pin. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| PIO0_8/ TCK | E4 | K4 | K16 | [2] | Z | I/O | 0 | PIO0_8 — General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock In). |
| | | | | | | I/O | 1 | FC1_TXD_SCL_MISO_WS — Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| | | | | | | I | 2 | SCT0_GPI5 — Pin input 5 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT5 — SCTimer/PWM output 5. |
| | | | | | | O | 4 | CTIMER1_MAT1 — 32-bit CTimer1 match output 1. |
| | | | | | | O | 5 | I2S_BRIDGE_WS_OUT — Allows I2S bypass by re-routing a pin that includes the I2S_BRIDGE_WS_IN function to this pin. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| PIO0_9/ TMS | E3 | L3 | K15 | [2] | Z | I/O | 0 | PIO0_9 — General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select). |
| | | | | | | I/O | 1 | FC1_RXD_SDA_MOSI_DATA — Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O. |
| | | | | | | I | 2 | SCT0_GPI6 — Pin input 6 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT6 — SCTimer/PWM output 6. |
| | | | | | | O | 4 | CTIMER1_MAT2 — 32-bit CTimer1 match output 2. |
| | | | | | | O | 5 | I2S_BRIDGE_DATA_OUT — Allows I2S bypass by re-routing a pin that includes the I2S_BRIDGE_DATA_IN function to this pin. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | 8 | SEC_PIO0_9 — Secure GPIO pin. | | | | | | |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|--------------------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO0_10/ TDI | E2 | J3 | L16 | [2] | Z | I/O | 0 | PIO0_10 — General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). |
| | | | | | | I/O | 1 | FC1_CTS_SDA_SSELO — Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| | | | | | | I | 2 | SCT0_GPI7 — Pin input 7 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT7 — SCTimer/PWM output 7. |
| | | | | | | O | 4 | CTIMER1_MAT3 — 32-bit CTimer1 match output 3. |
| | | | | | | I/O | 5 | FC0_SSEL2 — Flexcomm 0: SPI slave select 2. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_10 — Secure GPIO pin. |
| PIO0_11/ TDO | E1 | L1 | K13 | [2] | Z | I/O | 0 | PIO0_11 — General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out). |
| | | | | | | I/O | 1 | FC1_RTS_SCL_SSEL1 — Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1. |
| | | | | | | I | 2 | SCT0_GPI0 — Pin input 0 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT8 — SCTimer/PWM output 8. |
| | | | | | | I | 4 | CTIMER_INP2 — Capture input 2 to CTIMER input muxes. |
| | | | | | | I/O | 5 | FC0_SSEL3 — Flexcomm 0: SPI slave select 3. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_11 — Secure GPIO pin. |
| PIO0_12/ ADC0_1 | K1 | E3 | F15 | [3] | Z | I/O | 0 | PIO0_12/ADC0_1 — General-purpose digital input/output pin. ADC input channel 1 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | I/O | 1 | FC1_SSEL2 — Flexcomm 1: SPI slave select 2. |
| | | | | | | I | 2 | SCT0_GPI2 — Pin input 2 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT2 — SCTimer/PWM output 2. |
| | | | | | | I | 4 | CTIMER_INP3 — Capture input 3 to CTIMER input muxes. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_12 — Secure GPIO pin. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|--------------------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO0_13/ ADC0_9 | G4 | G3 | G16 | [3] | Z | I/O | 0 | PIO0_13/ADC0_9 — General-purpose digital input/output pin. ADC input channel 9 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | I/O | 1 | FC1_SSEL3 — Flexcomm 1: SPI slave select 3. |
| | | | | | | I | 2 | SCT0_GPI3 — Pin input 3 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT3 — SCTimer/PWM output 3. |
| | | | | | | O | 4 | CTIMER0_MAT1 — 32-bit CTimer0 match output 1. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_13 — Secure GPIO pin. |
| PIO0_14 | K4 | A3 | B17 | [2] | Z | I/O | 0 | PIO0_14 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC2_SCK — Flexcomm 1: USART, SPI, or I2S clock. |
| | | | | | | I | 2 | SCT0_GPI0 — Pin input 0 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT0 — SCTimer/PWM output 0. |
| | | | | | | O | 4 | CTIMER2_MAT0 — 32-bit CTimer2 match output 0. |
| | | | | | | I | 5 | I2S_BRIDGE_CLK_IN — Allows I2S bypass by re-routing this function to a pin that includes the I2S_BRIDGE_CLK_OUT function. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_14 — Secure GPIO pin. |
| PIO0_15 | J6 | A5 | A16 | [2] | Z | I/O | 0 | PIO0_15 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC2_TXD_SCL_MISO_WS — Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| | | | | | | I | 2 | SCT0_GPI1 — Pin input 1 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT1 — SCTimer/PWM output 1. |
| | | | | | | O | 4 | CTIMER2_MAT1 — 32-bit CTimer2 match output 1. |
| | | | | | | I | 5 | I2S_BRIDGE_WS_IN — Allows I2S bypass by re-routing this function to a pin that includes the I2S_BRIDGE_WS_OUT function. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_15 — Secure GPIO pin. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|--|
| PIO0_16 | K5 | D6 | B12 | [2] | Z | I/O | 0 | PIO0_16 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC2_RXD_SDA_MOSI_DATA — Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O. |
| | | | | | | I | 2 | SCT0_GPI2 — Pin input 2 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT2 — SCTimer/PWM output 2. |
| | | | | | | O | 4 | CTIMER2_MAT2 — 32-bit CTimer2 match output 2. |
| | | | | | | I | 5 | I2S_BRIDGE_DATA_IN — Allows I2S bypass by re-routing this function to a pin that includes the I2S_BRIDGE_DATA_OUT function. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_16 — Secure GPIO pin. |
| PIO0_17 | - | D7 | B14 | [2] | Z | I/O | 0 | PIO0_17 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC2_CTS_SDA_SSEL0 — Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| | | | | | | I | 2 | SCT0_GPI3 — Pin input 3 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT3 — SCTimer/PWM output 3. |
| | | | | | | O | 4 | CTIMER2_MAT3 — 32-bit CTimer2 match output 3. |
| | | | | | | I/O | 5 | FC5_SSEL2 — Flexcomm 5: SPI slave select 2. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_17 — Secure GPIO pin. |
| PIO0_18 | - | B7 | A14 | [2] | Z | I/O | 0 | PIO0_18 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC2_RTS_SCL_SSEL1 — Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1. |
| | | | | | | I | 2 | SCT0_GPI6 — Pin input 6 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT6 — SCTimer/PWM output 6. |
| | | | | | | I | 4 | CTIMER_INP4 — Capture input 4 to CTIMER input muxes. |
| | | | | | | I/O | 5 | FC5_SSEL3 — Flexcomm 5: SPI slave select 3. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_18 — Secure GPIO pin. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------------------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO0_19/ ADC0_2 | H6 | A1 | D12 | [3] | Z | I/O | 0 | PIO0_19/ADC0_2 — General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | | 1 | FC2_SSEL2 — Flexcomm 2: SPI slave select 2. |
| | | | | | | | 2 | SCT0_GPI4 — Pin input 4 to SCTimer/PWM. |
| | | | | | | | 3 | SCT0_OUT4 — SCTimer/PWM output 4. |
| | | | | | | | 4 | CTIMER_INP5 — Capture input 5 to CTIMER input muxes. |
| | | | | | | | 5 | UTICK_CAP0 — Micro-tick timer capture input 0. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | | 8 | SEC_PIO0_19 — Secure GPIO pin. |
| PIO0_20/ ADC0_10 | H5 | B2 | E13 | [3] | Z | I/O | 0 | PIO0_20/ADC0_10 — General-purpose digital input/output pin. ADC input channel 10 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | | 1 | FC2_SSEL3 — Flexcomm 2: SPI slave select 3. |
| | | | | | | | 2 | SCT0_GPI5 — Pin input 5 to SCTimer/PWM. |
| | | | | | | | 3 | SCT0_OUT5 — SCTimer/PWM output 5. |
| | | | | | | | 4 | CTIMER0_MAT2 — 32-bit CTimer0 match output 2. |
| | | | | | | | 5 | CTIMER_INP11 — Capture input 11 to CTIMER input muxes. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | | 8 | SEC_PIO0_20 — Secure GPIO pin. |
| PIO0_21 | L5 | C7 | A12 | [2] | Z | I/O | 0 | PIO0_21 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FC3_SCK — Flexcomm 3: USART, SPI, or I2S clock. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER3_MAT0 — 32-bit CTimer3 match output 0. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | TRACECLK — Trace clock. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | | 8 | SEC_PIO0_21 — Secure GPIO pin. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|---------------------------------------|-----|-----------------|------|------------|---|
| PIO0_22 | H7 | D8 | A10 | [2] | Z | I/O | 0 | PIO0_22 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC3_TXD_SCL_MISO_WS — Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER3_MAT1 — 32-bit CTimer3 match output 1. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | O | 6 | TRACEDATA[0] — Trace data bit 0. |
| | | | | | | | 7 | R — Reserved. |
| | I/O | 8 | SEC_PIO0_22 — Secure GPIO pin. | | | | | |
| PIO0_23 | K7 | C9 | A8 | [2] | Z | I/O | 0 | PIO0_23/ — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC3_RXD_SDA_MOSI_DATA — Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER3_MAT2 — 32-bit CTimer3 match output 2. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | O | 6 | TRACEDATA[1] — Trace data bit 1. |
| | | | | | | | 7 | R — Reserved. |
| | I/O | 8 | SEC_PIO0_23 — Secure GPIO pin. | | | | | |
| PIO0_24 | H8 | B9 | B8 | [2] | Z | I/O | 0 | PIO0_24 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC3_CTS_SDA_SSEL0 — Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER3_MAT3 — 32-bit CTimer3 match output 3. |
| | | | | | | I/O | 5 | FC2_SSEL2 — Flexcomm 2: SPI slave select 2. |
| | | | | | | O | 6 | TRACEDATA[2] — Trace data bit 2. |
| | | | | | | O | 7 | CLKOUT — Output of the CLKOUT function. |
| | I/O | 8 | SEC_PIO0_24 — Secure GPIO pin. | | | | | |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------------------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO0_25 | L6 | A9 | B7 | [2] | Z | I/O | 0 | PIO0_25 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC3_RTS_SCL_SSEL1 — Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | I | 3 | FREQME_GPIO_CLK — Frequency Measure pin clock input. |
| | | | | | | I | 4 | CTIMER_INP6 — Capture input 6 to CTIMER input muxes. |
| | | | | | | I/O | 5 | FC2_SSEL3 — Flexcomm 2: SPI slave select 3. |
| | | | | | | O | 6 | TRACEDATA[3] — Trace data bit 3. |
| | | | | | | I | 7 | CLKIN — Clock input. |
| | | | | | | I/O | 8 | SEC_PIO0_25 — Secure GPIO pin. |
| PIO0_26/ ADC0_3 | L3 | A2 | B16 | [3] | Z | I/O | 0 | PIO0_26/ADC0_3 — General-purpose digital input/output pin. ADC input channel 3 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | I/O | 1 | FC3_SSEL2 — Flexcomm 3: SPI slave select 2. |
| | | | | | | I | 2 | SCT0_GPI6 — Pin input 6 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT6 — SCTimer/PWM output 6. |
| | | | | | | I | 4 | CTIMER_INP7 — Capture input 7 to CTIMER input muxes. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_26 — Secure GPIO pin. |
| PIO0_27/ ADC0_11 | J4 | B3 | D13 | [3] | Z | I/O | 0 | PIO0_27/ADC0_11 — General-purpose digital input/output pin. ADC input channel 11 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | I/O | 1 | FC3_SSEL3 — Flexcomm 3: SPI slave select 3. |
| | | | | | | I | 2 | SCT0_GPI7 — Pin input 7 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT7 — SCTimer/PWM output 7. |
| | | | | | | O | 4 | CTIMER0_MAT3 — 32-bit CTimer0 match output 3. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_27 — Secure GPIO pin. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|---------------------------------------|----------------|-----|-----------------|------|------------|---|
| PIO0_28 | - | D11 | A6 | [2] | Z | I/O | 0 | PIO0_28 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC4_SCK — Flexcomm 4: USART, SPI, or I2S clock. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER4_MAT0 — 32-bit CTimer4 match output 0. |
| | | | | | | O | 5 | I2S_BRIDGE_CLK_OUT — Allows I2S bypass by re-routing a pin that includes the I2S_BRIDGE_CLK_IN function to this pin. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| I/O | 8 | SEC_PIO0_28 — Secure GPIO pin. | | | | | | |
| PIO0_29 | K8 | B10 | B6 | [2] | Z | I/O | 0 | PIO0_29 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC4_TXD_SCL_MISO_WS — Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER4_MAT1 — 32-bit CTimer4 match output 1. |
| | | | | | | O | 5 | I2S_BRIDGE_WS_OUT — Allows I2S bypass by re-routing a pin that includes the I2S_BRIDGE_WS_IN function to this pin. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| I/O | 8 | SEC_PIO0_29 — Secure GPIO pin. | | | | | | |
| PIO0_30 | L8 | C11 | C6 | [2] | Z | I/O | 0 | PIO0_30 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC4_RXD_SDA_MOSI_DATA — Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER4_MAT2 — 32-bit CTimer4 match output 2. |
| | | | | | | O | 5 | I2S_BRIDGE_DATA_OUT — Allows I2S bypass by re-routing a pin that includes the I2S_BRIDGE_DATA_IN function to this pin. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| I/O | 8 | SEC_PIO0_30 — Secure GPIO pin. | | | | | | |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|-------------------|----------------|----------------|----------------|-----|-----------------|------|------------|--|
| PIO0_31 | - | A11 | B1 | [2] | Z | I/O | 0 | PIO0_31 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC4_CTS_SDA_SSELO — Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| | | | | | | I | 2 | SCT0_GPIO0 — Pin input 0 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT6 — SCTimer/PWM output 6. |
| | | | | | | O | 4 | CTIMER4_MAT3 — 32-bit CTimer4 match output 3. |
| | | | | | | I/O | 5 | FC3_SSEL2 — Flexcomm 3: SPI slave select 2. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | | 7 | R — Reserved. |
| | | | | | | I/O | 8 | SEC_PIO0_31 — Secure GPIO pin. |
| PIO1_0 | - | E17 | H4 | [3] | Z | I/O | 0 | PIO1_0 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC4_RTS_SCL_SSEL1 — Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1. |
| | | | | | | I | 2 | SCT0_GPI1 — Pin input 1 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT7 — SCTimer/PWM output 7. |
| | | | | | | I | 4 | CTIMER_INP8 — Capture input 8 to CTIMER input muxes. |
| | | | | | | I/O | 5 | FC3_SSEL3 — Flexcomm 3: SPI slave select 3. |
| PIO1_1 | - | G15 | H5 | [2] | Z | I/O | 0 | PIO1_1 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC4_SSEL2 — Flexcomm 4: SPI slave select 2. |
| | | | | | | I | 2 | SCT0_GPIO2 — Pin input 2 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT8 — SCTimer/PWM output 8. |
| | | | | | | O | 4 | CTIMER1_MAT0 — 32-bit CTimer1 match output 0. |
| PIO1_2/ CMP0_C | K6 | A7 | B11 | [3] | Z | I/O | 0 | PIO1_2/CMP0_C — General-purpose digital input/output pin. Analog comparator input C if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | I/O | 1 | FC4_SSEL3 — Flexcomm 4: SPI slave select 3. |
| | | | | | | I | 2 | SCT0_GPI3 — Pin input 3 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT9 — SCTimer/PWM output 9. |
| | | | | | | O | 4 | CTIMER1_MAT1 — 32-bit CTimer1 match output 1. |
| PIO1_3 | F10 | G16 | J4 | [2] | Z | I/O | 0 | PIO1_3 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC5_SCK — Flexcomm 5: USART, SPI, or I2S clock. |
| PIO1_4 | F9 | G17 | H3 | [2] | Z | I/O | 0 | PIO1_4 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC5_TXD_SCL_MISO_WS — Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| PIO1_5 | E11 | J16 | J3 | [2] | Z | I/O | 0 | PIO1_5 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC5_RXD_SDA_MOSI_DATA — Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|--------------------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| | | | | | | | | |
| PIO1_6 | - | J17 | K3 | [2] | Z | I/O | 0 | PIO1_6 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC5_CTS_SDA_SSEL0 — Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| | | | | | | I | 2 | SCT0_GPI4 — Pin input 4 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT4 — SCTimer/PWM output 4. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I/O | 5 | FC4_SSEL2 — Flexcomm 4: SPI slave select 2. |
| PIO1_7 | - | J15 | E3 | [2] | Z | I/O | 0 | PIO1_7 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC5_RTS_SCL_SSEL1 — Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1. |
| | | | | | | I | 2 | SCT0_GPI5 — Pin input 5 to SCTimer/PWM. |
| | | | | | | O | 3 | SCT0_OUT5 — SCTimer/PWM output 5. |
| | | | | | | I | 4 | CTIMER_INP9 — Capture input 9 to CTIMER input muxes. |
| | | | | | | I/O | 5 | FC4_SSEL3 — Flexcomm 4: SPI slave select 3. |
| PIO1_8/ ADC0_4 | J5 | B5 | B15 | [3] | Z | I/O | 0 | PIO1_8/ADC0_4 — General-purpose digital input/output pin. ADC input channel 4 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | I/O | 1 | FC5_SSEL2 — Flexcomm 5: SPI slave select 2. |
| | | | | | | I | 2 | SCT0_GPI6 — Pin input 6 to SCTimer/PWM. |
| | | | | | | I | 3 | CTIMER_INP12 — Capture input 12 to CTIMER input muxes. |
| | | | | | | O | 4 | CTIMER1_MAT2 — 32-bit CTimer1 match output 2. |
| PIO1_9/ ADC0_12 | K3 | B1 | E14 | [3] | Z | I/O | 0 | PIO1_9ADC0_12 — General-purpose digital input/output pin. ADC input channel 12 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | I/O | 1 | FC5_SSEL3 — Flexcomm 5: SPI slave select 3. |
| | | | | | | I | 2 | SCT0_GPI7 — Pin input 7 to SCTimer/PWM. |
| | | | | | | I | 3 | UTICK_CAP1 — Micro-tick timer capture input 1. |
| | | | | | | O | 4 | CTIMER1_MAT3 — 32-bit CTimer1 match output 3. |
| PIO1_10 | E10 | K16 | F2 | [2] | Z | I/O | 0 | PIO1_10 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | MCLK — MCLK input or output for I2S and/or digital microphone. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | I | 3 | FREQME_GPIO_CLK — Frequency Measure pin clock input. |
| | | | | | | I | 4 | CTIMER_INP10 — Capture input 10 to CTIMER input muxes. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | R — Reserved. |
| | | | | | | O | 7 | CLKOUT — Output of the CLKOUT function. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|--|
| PIO1_11 | E5 | L2 | K14 | [2] | Z | I/O | 0 | PIO1_11 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | HS_SPI_SCK — Clock for high speed SPI. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER2_MAT0 — 32-bit CTimer2 match output 0. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | I/O | 6 | FLEXSPI0B_DATA0 — Data bit 0 for the FlexSPI B interface. |
| PIO1_12 | D2 | M2 | M17 | [2] | Z | I/O | 0 | PIO1_12 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | HS_SPI_MISO — Master-in/slave-out data for high speed SPI. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER2_MAT1 — 32-bit CTimer2 match output 1. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | I/O | 6 | FLEXSPI0B_DATA1 — Data bit 1 for the FlexSPI B interface. |
| PIO1_13 | D3 | N1 | M16 | [2] | Z | I/O | 0 | PIO1_13 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | HS_SPI_MOSI — Master-out/slave-in data for high speed SPI. |
| | | | | | | | 2 | R — Reserved |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER2_MAT2 — 32-bit CTimer2 match output 2. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | I/O | 6 | FLEXSPI0B_DATA2 — Data bit 2 for the FlexSPI B interface. |
| PIO1_14 | D4 | N2 | M14 | [2] | Z | I/O | 0 | PIO1_14 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | HS_SPI_SSEL0 — Slave Select 0 for high speed SPI. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER2_MAT3 — 32-bit CTimer2 match output 3. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | I/O | 6 | FLEXSPI0B_DATA3 — Data bit 3 for the FlexSPI B interface. |
| PIO1_15 | C2 | N3 | M15 | [2] | Z | I/O | 0 | PIO1_15 — General-purpose digital input/output pin. Remark: The state of this pin at Reset in conjunction with PIO1_16 and PIO1_17 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in the relevant User Manual for more details. |
| | | | | | | I/O | 1 | HS_SPI_SSEL1 — Slave Select 1 for high speed SPI. |
| | | | | | | | 2 | R — Reserved |
| | | | | | | | 3 | R — Reserved |
| | | | | | | O | 4 | CTIMER3_MAT0 — 32-bit CTimer3 match output 0. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|--|
| PIO1_16 | C3 | M4 | P17 | [2] | Z | I/O | 0 | PIO1_16 — General-purpose digital input/output pin. Remark: The state of this pin at Reset in conjunction with PIO1_15 and PIO1_17 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in the relevant User Manual for more details. |
| | | | | | | I/O | 1 | HS_SPI_SSEL2 — Slave Select 2 for high speed SPI. |
| | | | | | | O | 2 | SCT0_OUT8 — SCTimer/PWM output 8. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER3_MAT1 — 32-bit CTimer3 match output 1. |
| PIO1_17 | B2 | N4 | M13 | [2] | Z | I/O | 0 | PIO1_17 — General-purpose digital input/output pin. Remark: The state of this pin at Reset in conjunction with PIO1_15 and PIO1_16 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in the relevant User Manual for more details. |
| | | | | | | I/O | 1 | HS_SPI_SSEL3 — Slave Select 3 for high speed SPI. |
| | | | | | | O | 2 | SCT0_OUT9 — SCTimer/PWM output 9. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER3_MAT2 — 32-bit CTimer3 match output 2. |
| PIO1_18 | B7 | T9 | U4 | [2] | Z | I/O | 0 | PIO1_18 — General-purpose digital input/output pin. |
| | | | | | | O | 1 | FLEXSPI0A_SCLK — Clock output for the FlexSPI A interface. |
| | | | | | | I | 2 | SCT0_GPI0 — Pin input 0 to SCTimer/PWM. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER3_MAT3 — 32-bit CTimer3 match output 3. |
| PIO1_19 | B4 | T4 | U16 | [2] | Z | I/O | 0 | PIO1_19 — General-purpose digital input/output pin. |
| | | | | | | O | 1 | FLEXSPI0A_SS0_N — Active low slave select 0 for the FlexSPI A interface. |
| | | | | | | O | 2 | SCT0_OUT0 — SCTimer/PWM output 0. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER4_MAT0 — 32-bit CTimer4 match output 0. |
| PIO1_20 | C6 | T5 | T12 | [2] | Z | I/O | 0 | PIO1_20 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FLEXSPI0A_DATA0 — Data bit 0 for the FlexSPI A interface. |
| | | | | | | I | 2 | SCT0_GPI1 — Pin input 1 to SCTimer/PWM. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER4_MAT1 — 32-bit CTimer4 match output 1. |
| PIO1_21 | C7 | U5 | U12 | [2] | Z | I/O | 0 | PIO1_21 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FLEXSPI0A_DATA1 — Data bit 1 for the FlexSPI A interface. |
| | | | | | | O | 2 | SCT0_OUT1 — SCTimer/PWM output 1. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER4_MAT2 — 32-bit CTimer4 match output 2. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|--|
| | | | | | | | | |
| PIO1_22 | B5 | P6 | T11 | [2] | Z | I/O | 0 | PIO1_22 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FLEXSPI0A_DATA2 — Data bit 2 for the FlexSPI A interface. |
| | | | | | | | 2 | SCT0_GPI2 — Pin input 2 to SCTimer/PWM. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER4_MAT3 — 32-bit CTimer4 match output 3. |
| PIO1_23 | A5 | P7 | T10 | [2] | Z | I/O | 0 | PIO1_23 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FLEXSPI0A_DATA3 — Data bit 3 for the FlexSPI A interface. |
| | | | | | | | 2 | SCT0_OUT2 — SCTimer/PWM output 2. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER_INP8 — Capture input 8 to CTIMER input muxes. |
| PIO1_24 | - | T7 | U10 | [2] | Z | I/O | 0 | PIO1_24 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FLEXSPI0A_DATA4 — Data bit 4 for the FlexSPI A interface. |
| | | | | | | | 2 | SCT0_GPI3 — Pin input 3 to SCTimer/PWM. |
| | | | | | | | 3 | R — Reserved. |
| PIO1_25 | - | U7 | U8 | [2] | Z | I/O | 0 | PIO1_25 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FLEXSPI0A_DATA5 — Data bit 5 for the FlexSPI A interface. |
| | | | | | | | 2 | SCT0_OUT3 — SCTimer/PWM output 3. |
| | | | | | | | 3 | R — Reserved. |
| PIO1_26 | - | R7 | U6 | [2] | Z | I/O | 0 | PIO1_26 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FLEXSPI0A_DATA6 — Data bit 6 for the FlexSPI A interface. |
| | | | | | | | 2 | SCT0_GPI4 — Pin input 4 to SCTimer/PWM. |
| | | | | | | | 3 | R — Reserved. |
| PIO1_27 | - | T8 | T7 | [2] | Z | I/O | 0 | PIO1_27 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FLEXSPI0A_DATA7 — Data bit 7 for the FlexSPI A interface. |
| | | | | | | | 2 | SCT0_OUT4 — SCTimer/PWM output 4. |
| | | | | | | | 3 | R — Reserved. |
| PIO1_28 | - | U9 | T6 | [2] | Z | I/O | 0 | PIO1_28 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FLEXSPI0A_DQS — Data strobe output for the FlexSPI A interface. |
| | | | | | | | 2 | SCT0_GPI5 — Pin input 5 to SCTimer/PWM. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO1_29 | - | U3 | U14 | [2] | Z | I/O | 0 | PIO1_29 — General-purpose digital input/output pin. |
| | | | | | | O | 1 | FLEXSPI0A_SS1_N — Active low slave select 1 for the FlexSPI A interface. |
| | | | | | | I/O | 2 | SCT0_OUT5 — SCTimer/PWM output 5. |
| | | | | | | I | 3 | UTICK_CAP2 — Micro-tick timer capture input 2. |
| | | | | | | I | 4 | CTIMER_INP13 — Capture input 13 to CTIMER input muxes. |
| | | | | | | O | 5 | FLEXSPI0A_SCLK_N or FLEXSPI0B_SCLK — Inverted clock output for the FlexSPI A interface or Clock output for the FlexSPI B interface. |
| PIO1_30 | - | P10 | P5 | [2] | Z | I/O | 0 | PIO1_30 — General-purpose digital input/output pin. |
| | | | | | | O | 1 | SD0_CLK — SD/MMC0 clock. |
| | | | | | | I | 2 | SCT0_GPI0 — Pin input 0 to SCTimer/PWM. |
| PIO1_31 | - | R9 | N8 | [2] | Z | I/O | 0 | PIO1_31 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | SD0_CMD — SD/MMC0 card command I/O. |
| | | | | | | I | 2 | SCT0_GPI1 — Pin input 1 to SCTimer/PWM. |
| PIO2_0 | - | R11 | N6 | [3] | Z | I/O | 0 | PIO2_0 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | SD0_D[0] — SD/MMC0 interface data 0. |
| | | | | | | I | 2 | SCT0_GPI2 — Pin input 2 to SCTimer/PWM. |
| PIO2_1 | - | T11 | K6 | [3] | Z | I/O | 0 | PIO2_1 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | SD0_D[1] — SD/MMC0 interface data 1. |
| | | | | | | I | 2 | SCT0_GPI3 — Pin input 3 to SCTimer/PWM. |
| PIO2_2 | - | U11 | P6 | [3] | Z | I/O | 0 | PIO2_2 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | SD0_D[2] — SD/MMC0 interface data 2. |
| | | | | | | O | 2 | SCT0_OUT0 — SCTimer/PWM output 0. |
| PIO2_3 | - | T12 | M5 | [2] | Z | I/O | 0 | PIO2_3 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | SD0_D[3] — SD/MMC0 interface data 3. |
| | | | | | | O | 2 | SCT0_OUT1 — SCTimer/PWM output 1. |
| PIO2_4 | - | T13 | N5 | [2] | Z | I/O | 0 | PIO2_4 — General-purpose digital input/output pin. |
| | | | | | | I | 1 | SD0_WR_PRT — SD/MMC 0 write protect. |
| | | | | | | O | 2 | SCT0_OUT2 — SCTimer/PWM output 2. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I | 5 | SD0_DS — Read data strobe from SD/MMC0 device. |
| PIO2_5 | - | U13 | M4 | [2] | Z | I/O | 0 | PIO2_5 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | SD0_D[4] — SD/MMC0 interface data 4. |
| | | | | | | O | 2 | SCT0_OUT3 — SCTimer/PWM output 3. |
| | | | | | | | 3 | R — Reserved. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO2_6 | - | U15 | P4 | [2] | Z | I/O | 0 | PIO2_6 — General-purpose digital input/output pin. |
| | | | | | | | 1 | SD0_D[5] — SD/MMC0 interface data 5. |
| | | | | | | | 2 | SCT0_GPI4 — Pin input 4 to SCTimer/PWM. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER1_MAT0 — 32-bit CTimer1 match output 0. |
| PIO2_7 | - | U16 | N4 | [2] | Z | I/O | 0 | PIO2_7 — General-purpose digital input/output pin. |
| | | | | | | | 1 | SD0_D[6] — SD/MMC0 interface data 6. |
| | | | | | | | 2 | SCT0_GPI5 — Pin input 5 to SCTimer/PWM. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER1_MAT1 — 32-bit CTimer1 match output 1. |
| PIO2_8 | - | U17 | M1 | [2] | Z | I/O | 0 | PIO2_8 — General-purpose digital input/output pin. |
| | | | | | | | 1 | SD0_D[7] — SD/MMC0 interface data 7. |
| | | | | | | | 2 | SCT0_OUT4 — SCTimer/PWM output 4. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER1_MAT2 — 32-bit CTimer1 match output 2. |
| PIO2_9 | - | R13 | M2 | [2] | Z | I/O | 0 | PIO2_9 — General-purpose digital input/output pin. |
| | | | | | | | 1 | SD0_CARD_DET_N — SD/MMC 0 card detect (active low). |
| | | | | | | | 2 | SCT0_OUT5 — SCTimer/PWM output 5. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER1_MAT3 — 32-bit CTimer1 match output 3. |
| PIO2_10 | - | T15 | M3 | [2] | Z | I/O | 0 | PIO2_10 — General-purpose digital input/output pin. |
| | | | | | | | 1 | SD0_RESET_N — SD/MMC0 card hardware reset, active low. |
| | | | | | | | 2 | SCT0_GPI6 — Pin input 6 to SCTimer/PWM. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER2_MAT0 — 32-bit CTimer2 match output 0. |
| PIO2_11 | - | T16 | N3 | [2] | Z | I/O | 0 | PIO2_11 — General-purpose digital input/output pin. |
| | | | | | | | 1 | SD0_VOLT — SD/MMC0 card regulator voltage control. |
| | | | | | | | 2 | SCT0_GPI7 — Pin input 7 to SCTimer/PWM. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER2_MAT1 — 32-bit CTimer2 match output 1. |
| PIO2_12 | - | T3 | T14 | [2] | Z | I/O | 0 | PIO2_12 — General-purpose digital input/output pin. |
| | | | | | | | 1 | R — Reserved. |
| | | | | | | | 2 | SCT0_OUT6 — SCTimer/PWM output 6. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER2_MAT2 — 32-bit CTimer2 match output 2. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description | | | | | | | |
|--------------------|--|----------------|----------------|-----|-----------------|----------|--------------------|---|----|-----|-----|---|----------|---|---|
| PIO2_13 | - | T1 | N15 | [2] | Z | I/O | 0 | PIO2_13 — General-purpose digital input/output pin. | | | | | | | |
| | | | | | | | 1 | R — Reserved. | | | | | | | |
| | | | | | | | O 2 | SCT0_OUT7 — SCTimer/PWM output 7. | | | | | | | |
| | | | | | | | 3 | R — Reserved. | | | | | | | |
| | | | | | | | O 4 | CTIMER2_MAT3 — 32-bit CTimer2 match output 3. | | | | | | | |
| | | | | | | | 5 | R — Reserved. | | | | | | | |
| | | | | | | | 6 | R — Reserved. | | | | | | | |
| PIO2_14/ CMP0_A | G5 | C1 | F14 | [3] | Z | I/O ; AI | 0 | PIO2_14/CMP0_A — General-purpose digital input/output pin. Analog comparator input A if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. | | | | | | | |
| | | | | | | | 1 | R — Reserved. | | | | | | | |
| | | | | | | | O 2 | SCT0_OUT8 — SCTimer/PWM output 8. | | | | | | | |
| | | | | | | | 3 | R — Reserved. | | | | | | | |
| | | | | | | | I 4 | CTIMER_INP1 — Capture input 1 to CTIMER input muxes. | | | | | | | |
| | | | | | | | PIO2_15/ CMP0_D | H4 | E2 | F13 | [3] | Z | I/O ; AI | 0 | PIO2_15/CMP0_D — General-purpose digital input/output pin. Analog comparator input D if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | | | | | | | | | 1 | R — Reserved. |
| O 2 | SCT0_OUT9 — SCTimer/PWM output 9. | | | | | | | | | | | | | | |
| 3 | R — Reserved. | | | | | | | | | | | | | | |
| 4 | R — Reserved. | | | | | | | | | | | | | | |
| 5 | R — Reserved. | | | | | | | | | | | | | | |
| 6 | R — Reserved. | | | | | | | | | | | | | | |
| PIO2_16 | B3 | R1 | P16 | [2] | Z | I/O | 0 | PIO2_16 — General-purpose digital input/output pin. | | | | | | | |
| | | | | | | | O 1 | PDM_CLK01 — PDM clock output for DMIC channels 0 and 1. | | | | | | | |
| | | | | | | | 2 | R — Reserved. | | | | | | | |
| | | | | | | | 3 | R — Reserved. | | | | | | | |
| PIO2_17 | C4 | U1 | R16 | [2] | Z | I/O | 0 | PIO2_17 — General-purpose digital input/output pin. | | | | | | | |
| | | | | | | | O 1 | PDM_CLK23 — PDM clock output for DMIC channels 2 and 3. | | | | | | | |
| | | | | | | | 2 | R — Reserved. | | | | | | | |
| | | | | | | | 3 | R — Reserved. | | | | | | | |
| | | | | | | | 4 | R — Reserved. | | | | | | | |
| | | | | | | | 5 | R — Reserved. | | | | | | | |
| | | | | | | | I/O 6 | FLEXSPI0B_DATA4 — Data bit 4 for the FlexSPI B interface. | | | | | | | |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO2_18 | B1 | R2 | P15 | [2] | Z | I/O | 0 | PIO2_18 — General-purpose digital input/output pin. |
| | | | | | | | O 1 | PDM_CLK45 — PDM clock output for DMIC channels 4 and 5. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | I/O 6 | FLEXSPI0B_DATA5 — Data bit 5 for the FlexSPI B interface. |
| PIO2_19 | A2 | T2 | N14 | [2] | Z | I/O | 0 | PIO2_19 — General-purpose digital input/output pin. |
| | | | | | | | O 1 | PDM_CLK67 — PDM clock output for DMIC channels 6 and 7. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | O 6 | FLEXSPI0B_SS0_N — Active low slave select 0 for the FlexSPI B interface. |
| PIO2_20 | C5 | U2 | N13 | [2] | Z | I/O | 0 | PIO2_20 — General-purpose digital input/output pin. |
| | | | | | | | I 1 | PDM_DATA01 — PDM data input for DMIC channels 0 and 1. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| PIO2_21 | A3 | R3 | P13 | [2] | Z | I/O | 0 | PIO2_21 — General-purpose digital input/output pin. |
| | | | | | | | I 1 | PDM_DATA23 — PDM data input for DMIC channels 2 and 3. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | I 4 | CTIMER_INP14 — Capture input 14 to CTIMER input muxes. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | O 6 | FLEXSPI0B_SS1_N — Active low slave select 1 for the FlexSPI B interface. |
| PIO2_22 | - | P3 | P14 | [2] | Z | I/O | 0 | PIO2_22 — General-purpose digital input/output pin. |
| | | | | | | | I 1 | PDM_DATA45 — PDM data input for DMIC channels 4 and 5. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | I/O 6 | FLEXSPI0B_DATA6 — Data bit 6 for the FlexSPI B interface. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description | |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|--|--|
| | | | | | | | | | |
| PIO2_23 | - | P5 | R14 | [2] | Z | I/O | 0 | PIO2_23 — General-purpose digital input/output pin. | |
| | | | | | | | I | 1 | PDM_DATA67 — PDM data input for DMIC channels 6 and 7. |
| | | | | | | | | 2 | R — Reserved. |
| | | | | | | | | 3 | R — Reserved. |
| | | | | | | | | 4 | R — Reserved. |
| | | | | | | | | 5 | R — Reserved. |
| | | | | | | | I/O | 6 | FLEXSPI0B_DATA7 — Data bit 7 for the FlexSPI B interface. |
| PIO2_24 | - | L16 | G2 | [2] | Z | I/O | 0 | PIO2_24 — General-purpose digital input/output pin. | |
| | | | | | | | O | 1 | SWO — Serial Wire Debug trace output. |
| | | | | | | | | 2 | R — Reserved. |
| | | | | | | | | 3 | R — Reserved. |
| | | | | | | | | 4 | R — Reserved. |
| | | | | | | | | 5 | R — Reserved. |
| | | | | | | | O | 6 | GPIO_INT_BMAT — Output of the pin interrupt pattern match engine. |
| PIO2_25 | D8 | L17 | F1 | [2] | Z | I/O | 0 | PIO2_25 — General-purpose digital input/output pin. | |
| | | | | | | | O | 1 | SWCLK — Serial Wire Debug clock. This is the default function after booting. |
| PIO2_26 | D10 | L15 | H2 | [2] | Z | I/O | 0 | PIO2_26 — General-purpose digital input/output pin. | |
| | | | | | | | I/O | 1 | SWDIO — Serial Wire Debug I/O. This is the default function after booting. |
| PIO2_27 | D9 | M14 | H1 | [2] | Z | I/O | 0 | PIO2_27 — General-purpose digital input/output pin. | |
| | | | | | | | I | 1 | USB1_OVERCURRENTN — USB1 bus overcurrent indicator (active low). USB host only function. Port power fault signal indicating over-current condition. This signal monitors over-current on the USB bus (external circuitry required to detect over-current condition, active LOW) |
| PIO2_28 | C8 | N15 | K2 | [2] | Z | I/O | 0 | PIO2_28 — General-purpose digital input/output pin. | |
| | | | | | | | O | 1 | USB1_PORTPWRN — USB1 VBUS drive enable (Indicates VBUS must supplied in host mode). |
| PIO2_29 | C11 | N17 | L2 | [2] | Z | I/O | 0 | PIO2_29 — General-purpose digital input/output pin. | |
| | | | | | | | I/O | 1 | I3C0_SCL — Clock for I3C master or slave. |
| | | | | | | | O | 2 | SCT0_OUT0 — SCTimer/PWM output 0. |
| | | | | | | | | 3 | R — Reserved. |
| | | | | | | | | 4 | R — Reserved. |
| | | | | | | | O | 5 | CLKOUT — Output of the CLKOUT function. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|--------------------|----------------|----------------|---|-----|-----------------|-------------|------------|--|
| PIO2_30 | C9 | P16 | K1 | [2] | Z | I/O | 0 | PIO2_30 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | I3C0_SDA — Data for I3C master or slave. |
| | | | | | | O | 2 | SCT0_OUT3 — SCTimer/PWM output 3. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I | 5 | CLKIN — Clock input. |
| | | | | | | | 6 | R — Reserved. |
| | O | 7 | CMP0_OUT — Analog comparator 0 output. | | | | | |
| PIO2_31/ CMP0_B | J7 | B6 | C12 | [3] | Z | I/O ; AI | 0 | PIO2_31/CMP0_B — General-purpose digital input/output pin. Analog comparator input B if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | O | 1 | I3C0_PUR — Pullup resistor control for I3C master. The I3C0_PUR function controls the SDA pull-up. It is intended to be connected to one end of an external low-value pull-up resistor (e.g. 1KOhm), with the other end connected to the SDA line. If there is no external high weak bus keeper on SDA, then add an additional external weak (e.g. 100KR or even 500KR) always-on pull-up on this line. |
| | | | | | | O | 2 | SCT0_OUT7 — SCTimer/PWM output 7. |
| | | | | | | I | 3 | UTICK_CAP3 — Micro-tick timer capture input 3. |
| | | | | | | I | 4 | CTIMER_INP15 — Capture input 15 to CTIMER input muxes. |
| | O | 5 | SWO — Serial Wire Debug trace output. | | | | | |
| PIO3_0 | - | - | D14 | [2] | Z | I/O | 0 | PIO3_0 — General-purpose digital input/output pin. |
| | | | | | | O | 1 | PDM_CLK01 — PDM clock output for DMIC channels 0 and 1. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | 5 | FC0_SCK — Flexcomm 0: USART, SPI, or I2S clock. | | | | | |
| PIO3_1 | - | - | D15 | [2] | Z | I/O | 0 | PIO3_1 — General-purpose digital input/output pin. |
| | | | | | | O | 1 | PDM_CLK23 — PDM clock output for DMIC channels 2 and 3. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | I/O | 5 | FC0_TXD_SCL_MISO_WS — Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. | | | | | |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description | |
|--------|----------------|----------------|----------------|-----|-----------------|------|------------|---|---|
| | | | | | | | | | |
| PIO3_2 | - | - | D16 | [2] | Z | I/O | 0 | PIO3_2 — General-purpose digital input/output pin. | |
| | | | | | | | O | 1 | PDM_CLK45 — PDM clock output for DMIC channels 4 and 5. |
| | | | | | | | | 2 | R — Reserved. |
| | | | | | | | | 3 | R — Reserved. |
| | | | | | | | | 4 | R — Reserved. |
| | | | | | | | I/O | 5 | FC0_RXD_SDA_MOSI_DATA — Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O |
| PIO3_3 | - | - | D17 | [2] | Z | I/O | 0 | PIO3_3 — General-purpose digital input/output pin. | |
| | | | | | | | O | 1 | PDM_CLK67 — PDM clock output for DMIC channels 6 and 7. |
| | | | | | | | | 2 | R — Reserved. |
| | | | | | | | | 3 | R — Reserved. |
| | | | | | | | | 4 | R — Reserved. |
| | | | | | | | I/O | 5 | FC0_CTS_SDA_SSEL0 — Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| | | | | | | | O | 7 | CMP0_OUT — Analog comparator 0 output. |
| PIO3_4 | - | - | C16 | [2] | Z | I/O | 0 | PIO3_4 — General-purpose digital input/output pin. | |
| | | | | | | | I | 1 | PDM_DATA01 — PDM data input for DMIC channels 0 and 1. |
| | | | | | | | | 2 | R — Reserved. |
| | | | | | | | | 3 | R — Reserved. |
| | | | | | | | | 4 | R — Reserved. |
| | | | | | | | I/O | 5 | FC0_RTS_SCL_SSEL1 — Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1. |
| PIO3_5 | - | - | C14 | [2] | Z | I/O | 0 | PIO3_5 — General-purpose digital input/output pin. | |
| | | | | | | | I | 1 | PDM_DATA23 — PDM data input for DMIC channels 2 and 3. |
| | | | | | | | | 2 | R — Reserved. |
| | | | | | | | | 3 | R — Reserved. |
| | | | | | | | | 4 | R — Reserved. |
| | | | | | | | I/O | 5 | FC0_SSEL2 — Flexcomm 0: SPI slave select 2. |
| PIO3_6 | - | - | C13 | [2] | Z | I/O | 0 | PIO3_6 — General-purpose digital input/output pin. | |
| | | | | | | | I | 1 | PDM_DATA45 — PDM data input for DMIC channels 4 and 5. |
| | | | | | | | | 2 | R — Reserved. |
| | | | | | | | | 3 | R — Reserved. |
| | | | | | | | | 4 | R — Reserved. |
| | | | | | | | I/O | 5 | FC0_SSEL3 — Flexcomm 0: SPI slave select 3. |
| PIO3_7 | - | - | E10 | [2] | Z | I/O | 0 | PIO3_7 — General-purpose digital input/output pin. | |
| | | | | | | | I | 1 | PDM_DATA67 — PDM data input for DMIC channels 6 and 7. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| | | | | | | | | |
| PIO3_8 | - | - | C10 | [2] | Z | I/O | 0 | PIO3_8 — General-purpose digital input/output pin. |
| | | | | | | | O 1 | SD1_CLK — SD/MMC1 clock. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | O 4 | CTIMER0_MAT0 — 32-bit CTimer0 match output 0. |
| PIO3_9 | - | - | B10 | [2] | Z | I/O | 0 | PIO3_9 — General-purpose digital input/output pin. |
| | | | | | | | I/O 1 | SD1_CMD — SD/MMC1 card command I/O. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | O 4 | CTIMER0_MAT1 — 32-bit CTimer0 match output 1. |
| PIO3_10 | - | - | C9 | [2] | Z | I/O | 0 | PIO3_10 — General-purpose digital input/output pin. |
| | | | | | | | I/O 1 | SD1_D[0] — SD/MMC1 interface data 0. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | O 4 | CTIMER0_MAT2 — 32-bit CTimer0 match output 2. |
| PIO3_11 | - | - | D9 | [2] | Z | I/O | 0 | PIO3_11 — General-purpose digital input/output pin. |
| | | | | | | | I/O 1 | SD1_D[1] — SD/MMC1 interface data 1. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | O 4 | CTIMER0_MAT3 — 32-bit CTimer0 match output 3. |
| PIO3_12 | - | - | C8 | [2] | Z | I/O | 0 | PIO3_12 — General-purpose digital input/output pin. |
| | | | | | | | I/O 1 | SD1_D[2] — SD/MMC1 interface data 2. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | I 4 | CTIMER_INP0 — Capture input 0 to CTIMER input muxes. |
| PIO3_13 | - | - | D5 | [2] | Z | I/O | 0 | PIO3_13 — General-purpose digital input/output pin. |
| | | | | | | | I/O 1 | SD1_D[3] — SD/MMC1 interface data 3. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | I 4 | CTIMER_INP1 — Capture input 1 to CTIMER input muxes. |
| PIO3_14 | - | - | D10 | [2] | Z | I/O | 0 | PIO3_14 — General-purpose digital input/output pin. |
| | | | | | | | I 1 | SD1_WR_PRT — SD/MMC 1 write protect. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | O 4 | CTIMER3_MAT0 — 32-bit CTimer3 match output 0. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO3_15 | - | - | E9 | [2] | Z | I/O | 0 | PIO3_15 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | SD1_D[4] — SD/MMC1 interface data 4. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER3_MAT1 — 32-bit CTimer3 match output 1. |
| | | | | | | I/O | 5 | FC5_SCK — Flexcomm 5: USART, SPI, or I2S clock. |
| PIO3_16 | - | - | E6 | [2] | Z | I/O | 0 | PIO3_16 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | SD1_D[5] — SD/MMC1 interface data 5. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER3_MAT2 — 32-bit CTimer3 match output 2. |
| | | | | | | I/O | 5 | FC5_TXD_SCL_MISO_WS — Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| PIO3_17 | - | - | E5 | [2] | Z | I/O | 0 | PIO3_17 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | SD1_D[6] — SD/MMC1 interface data 6. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER3_MAT3 — 32-bit CTimer3 match output 3. |
| | | | | | | I/O | 5 | FC5_RXD_SDA_MOSI_DATA — Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O |
| PIO3_18 | - | - | D1 | [2] | Z | I/O | 0 | PIO3_18 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | SD1_D[7] — SD/MMC1 interface data 7. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER4_MAT0 — 32-bit CTimer4 match output 0. |
| | | | | | | I/O | 5 | FC5_CTS_SDA_SSEL0 — Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| PIO3_19 | - | - | D2 | [2] | Z | I/O | 0 | PIO3_19 — General-purpose digital input/output pin. |
| | | | | | | I | 1 | SD1_CARD_DET_N — SD/MMC 1 card detect (active low). |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | O | 4 | CTIMER4_MAT1 — 32-bit CTimer4 match output 1. |
| | | | | | | I/O | 5 | MCLK — MCLK input or output for I2S and/or digital microphone. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------------------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO3_20 | - | - | C2 | [2] | Z | I/O | 0 | PIO3_20 — General-purpose digital input/output pin. |
| | | | | | | | 1 | SD1_RESET_N — SD/MMC1 card hardware reset, active low. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER4_MAT2 — 32-bit CTimer4 match output 2. |
| PIO3_21 | - | - | D8 | [2] | Z | I/O | 0 | PIO3_21 — General-purpose digital input/output pin. |
| | | | | | | | 1 | SD1_VOLT — SD/MMC1 card regulator voltage control. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | CTIMER4_MAT3 — 32-bit CTimer4 match output 3. |
| | | | | | | | 6 | GPIO_INT_BMAT — Output of the pin interrupt pattern match engine. |
| PIO3_22 | - | - | D6 | [2] | Z | I/O | 0 | PIO3_22 — General-purpose digital input/output pin. |
| | | | | | | | 1 | R — Reserved. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I/O | 5 | FC5_RTS_SCL_SSEL1 — Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1. |
| PIO3_23/ ADC0_5 | - | - | H12 | [3] | Z | I/O | 0 | PIO3_23/ADC0_5 — General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | | 1 | R — Reserved. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I/O | 5 | FC5_SSEL2 — Flexcomm 5: SPI slave select 2. |
| PIO3_24/ ADC0_13 | - | - | E15 | [3] | Z | I/O | 0 | PIO3_24/ADC0_13 — General-purpose digital input/output pin. ADC input channel 13 if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin. |
| | | | | | | | 1 | R — Reserved. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I/O | 5 | FC5_SSEL3 — Flexcomm 5: SPI slave select 3. |
| PIO3_25 | - | - | R9 | [2] | Z | I/O | 0 | PIO3_25 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FC6_SCK — Flexcomm 6: USART, SPI, or I2S clock. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO3_26 | A8 | - | P9 | [2] | Z | I/O | 0 | PIO3_26 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC6_TXD_SCL_MISO_WS — Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| PIO3_27 | A7 | - | T8 | [2] | Z | I/O | 0 | PIO3_27 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC6_RXD_SDA_MOSI_DATA — Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O |
| PIO3_28 | - | - | R8 | [2] | Z | I/O | 0 | PIO3_28 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC6_CTS_SDA_SSEL0 — Flexcomm 6: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| PIO3_29 | - | - | P8 | [2] | Z | I/O | 0 | PIO3_29 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC6_RTS_SCL_SSEL1 — Flexcomm 6: USART request-to-send, I2C clock, SPI slave select 1. |
| PIO3_30 | - | - | N9 | [2] | Z | I/O | 0 | PIO3_30 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC6_SSEL2 — Flexcomm 6: SPI slave select 2. |
| PIO3_31 | - | - | P7 | [2] | Z | I/O | 0 | PIO3_31 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC6_SSEL3 — Flexcomm 6: SPI slave select 3. |
| PIO4_0 | - | - | R13 | [2] | Z | I/O | 0 | PIO4_0 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC7_SCK — Flexcomm 7: USART, SPI, or I2S clock. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | I | 4 | FREQME_GPIO_CLK — Frequency Measure pin clock input. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | R — Reserved. |
| PIO4_1 | - | - | T17 | [2] | Z | I/O | 0 | PIO4_1 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC7_TXD_SCL_MISO_WS — Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | I | 7 | CLKIN — Clock input. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|--|-----|-----------------|------|------------|--|
| PIO4_2 | - | - | T16 | [2] | Z | I/O | 0 | PIO4_2 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC7_RXD_SDA_MOSI_DATA — Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O. |
| PIO4_3 | - | - | T3 | [2] | Z | I/O | 0 | PIO4_3 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC7_CTS_SDA_SSEL0 — Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| PIO4_4 | - | - | R2 | [2] | Z | I/O | 0 | PIO4_4 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC7_RTS_SCL_SSEL1 — Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1. |
| PIO4_5 | - | - | P1 | [2] | Z | I/O | 0 | PIO4_5 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC7_SSEL2 — Flexcomm 7: SPI slave select 2. |
| PIO4_6 | - | - | P2 | [2] | Z | I/O | 0 | PIO4_6 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC7_SSEL3 — Flexcomm 7: SPI slave select 3. |
| PIO4_7 | - | - | P3 | [2] | Z | I/O | 0 | PIO4_7 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | MCLK — MCLK input or output for I2S and/or digital microphone. |
| PIO4_8 | - | - | R4 | [2] | Z | I/O | 0 | PIO4_8 — General-purpose digital input/output pin. |
| | | | | | | | 1 | R — Reserved. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I/O | 5 | FC2_CTS_SDA_SSEL0 — Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| | | | | | | | 6 | R — Reserved. |
| | O | 7 | CMP0_OUT — Analog comparator 0 output. | | | | | |
| PIO4_9 | - | - | R5 | [2] | Z | I/O | 0 | PIO4_9 — General-purpose digital input/output pin. |
| | | | | | | | 1 | R — Reserved. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | | 5 | R — Reserved. |
| | O | 6 | GPIO_INT_BMAT — Output of the pin interrupt pattern match engine. | | | | | |
| PIO4_10 | - | - | R6 | [2] | Z | I/O | 0 | PIO4_10 — General-purpose digital input/output pin. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|---------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO7_24 | - | - | T15 | [2] | Z | I/O | 0 | PIO7_24 — General-purpose digital input/output pin. |
| | | | | | | | 1 | R — Reserved. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | | 5 | FC2_SCK — Flexcomm 2: USART, SPI, or I2S clock. |
| | | | | | | | 6 | ESPI_ALERTN — Alert used by eSPI slave to request service from eSPI master, active LOW. |
| PIO7_25 | - | - | P12 | [2] | Z | I/O | 0 | PIO7_25 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FC1_SCK — Flexcomm 1: USART, SPI, or I2S clock. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | ESPI_RST — Active LOW reset for the eSPI interface. |
| PIO7_26 | - | - | N12 | [2] | Z | I/O | 0 | PIO7_26 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FC1_TXD_SCL_MISO_WS — Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | ESPI_CSN — Active LOW chip select input. |
| PIO7_27 | - | - | R12 | [2] | Z | I/O | 0 | PIO7_27 — General-purpose digital input/output pin. |
| | | | | | | | 1 | FC1_RXD_SDA_MOSI_DATA — Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | | 5 | R — Reserved. |
| | | | | | | | 6 | ESPI_IO[0] — Bi-directional input/output pin used to transfer data between master and slaves. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|--------------|----------------|----------------|----------------|-----|-----------------|------|------------|---|
| PIO7_28 | - | - | N10 | [2] | Z | I/O | 0 | PIO7_28 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC1_CTS_SDA_SSEL0 — Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I/O | 5 | R — Reserved. |
| | | | | | | I/O | 6 | ESPI_IO[1] — Bi-directional input/output pin used to transfer data between master and slaves. |
| PIO7_29 | - | - | R10 | [2] | Z | I/O | 0 | PIO7_29 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC1_RTS_SCL_SSEL1 — Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I/O | 5 | R — Reserved. |
| | | | | | | I/O | 6 | ESPI_CLK — Provides the reference timing for all the serial input and output operations. |
| PIO7_30 | - | - | P10 | [2] | Z | I/O | 0 | PIO7_30 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC1_SSEL2 — Flexcomm 1: SPI slave select 2. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I/O | 5 | FC2_TXD_SCL_MISO_WS — Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word select/frame. |
| | | | | | | I/O | 6 | ESPI_IO[2] — Bi-directional input/output pin used to transfer data between master and slaves. |
| PIO7_31 | - | - | T4 | [2] | Z | I/O | 0 | PIO7_31 — General-purpose digital input/output pin. |
| | | | | | | I/O | 1 | FC1_SSEL3 — Flexcomm 1: SPI slave select 3. |
| | | | | | | | 2 | R — Reserved. |
| | | | | | | | 3 | R — Reserved. |
| | | | | | | | 4 | R — Reserved. |
| | | | | | | I/O | 5 | FC2_RXD_SDA_MOSI_DATA — Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O. |
| | | | | | | I/O | 6 | ESPI_IO[3] — Bi-directional input/output pin used to transfer data between master and slaves. |
| PMIC_I2C_SCL | - | E16 | F4 | [4] | Z | O | - | I2C clock. Used for communication with an off-chip PMIC, if present. It is not an open drain pin. |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [4] | Type | Function # | Description |
|---------------|---------------------------------------|--|--|-----|-----------------|------|------------|---|
| PMIC_I2C_SDA | - | F16 | F3 | [4] | Z | I/O | - | I2C data. Used for communication with an off-chip PMIC, if present. It is not an open drain pin. |
| PMIC_IRQ_N | - | A15 | F5 | [4] | Z | I | - | Interrupt input, active low logic. Used with an off-chip PMIC, if present. |
| PMIC_MODE0 | - | C15 | D3 | [4] | O | O | - | Power mode control output to an off-chip PMIC, if present. Value is controlled by the PDRUNCFG and PDSLEEPCFG registers. Reset state is 0. |
| PMIC_MODE1 | - | B16 | E4 | [4] | O | O | - | Power mode control output to an off-chip PMIC, if present. Value is controlled by the PDRUNCFG and PDSLEEPCFG registers. Reset state is 0. |
| RESETN | K10 | B15 | C4 | | - | I | - | External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and the boot code to execute. Wakes up the part from deep power-down mode. |
| RTCXIN | - | B17 | A2 | | - | - | - | RTC oscillator input. |
| RTCXOUT | - | A17 | B3 | | - | - | - | RTC oscillator output. |
| USB1_DM | B9 | T17 | T1 | | - | I/O | - | USB1 bidirectional D- line. |
| USB1_DP | B10 | R17 | U2 | | - | I/O | - | USB1 bidirectional D+ line. |
| USB1_VBUS [6] | - | R16 | T2 | | - | I | - | VBUS pin (power on USB cable). 5 V tolerant pin when supplies are present or when not present. |
| USB1_VDD3V3 | C10 | N16 | K5 | [5] | - | - | - | USB1 analog 3.3 V supply. |
| LDO_ENABLE | H9 | A16 | C5 | | - | - | - | When 1, enables the on-chip regulator to power core logic through the VDDCORE pins. Tie low if an off-chip power management IC (PMIC) is used to supply power to core logic. This pin can not be left floating. 100K external pull-up or 10K external pull-down is recommended. LDO_Enable is a fail-safe pin. It can driven high before VDD_AO1V8 supply comes up or at the same time. |
| VDD_AO1V8 | L11 | C13; D13 | B2; D4 | [5] | - | - | - | Supply 1.8 V supply for "always on" features. This includes the RTC, RESETN, LDO_ENABLE, PMIC_IRQ_N, PMIC_MODE0, and PMIC_MODE1. See Table 5 |
| VDDIO_0 | B8; D7; E7; F2; G3; J2 | F5; H5; K5; M5; N6; N8; N10 | J12; J13; K12; M10; M12; M9 | [5] | - | - | - | Single 1.8 V to 3.3 V power supply for GPIOs defined as belonging to the VDDIO_0 group. VDDIO_0, VDDIO_1, and VDDIO_2 may be supplied at different voltage levels as needed by the application. VDDIO_0 supplies the following port pins: PIO0_0 to PIO0_13; PIO1_11 to PIO1_29; and PIO2_12 to PIO2_23. See Table 5 |
| VDDIO_1 | E9; J8; L2 | E6; E8; E10; H13; H14; K13; L14 | F10; F11; F6; F7; F9; J5; J6 | [5] | - | - | - | Single 1.8 V to 3.3 V power supply for GPIOs defined as belonging to the VDDIO_1 group. VDDIO_0, VDDIO_1, and VDDIO_2 may be supplied at different voltage levels as needed by the application. VDDIO_1 supplies the following port pins: PIO0_14 to PIO0_31; PIO1_0 to PIO1_10; PIO2_24 to PIO2_31; PMIC_I2C_SCL and PMIC_I2C_SDA. See Table 5 |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | | Reset state [1] | Type | Function # | Description |
|-------------|--|--|--|-----|-----------------|------|------------|---|
| VDDIO_2 | - | N12; P11; P12 | M7; M8 | [5] | - | - | - | Single 1.8 V to 3.3 V power supply for GPIOs defined as belonging to the VDDIO_2 group. VDDIO_0, VDDIO_1, and VDDIO_2 may be supplied at different voltage levels as needed by the application. VDDIO_2 supplies the following port pins: PIO1_30 to PIO1_31 and PIO2_0 to PIO2_11. See Table 5 |
| VDD1V8 | A9; K2; L10; D5; G8; H10; H11; J10 | B11; C16; C17; E15; F13; G14; L4; R15 | E8; J14; H6; G6; H7; J7; M6 | [5] | - | - | - | 1.8 V supply voltage for on-chip analog functions other than the ADC and comparator. |
| VDDA_ADC1V8 | - | E4 | H13 | [5] | - | - | - | 1.8 V analog supply voltage for ADC and comparator. |
| VDDA_BIAS | - | C4 | E12 | [5] | - | - | - | Bias for ADC and comparator. VDD_BIAS must be equal to max ADC input voltage or max comparator input voltage |
| VDDCORE | A10; C1; E8; F1; F6; F7; G2; G7; G10; G11 | C5; D9; F14; J4; J14; P9; R5; R14 | G9; H10; H8; H9; J10; J11; J8; J9; K10; K8; K9; L9 | [5] | - | - | - | Power supply for core logic. May be supplied from the internal LDO or externally by an off-chip power management IC (PMIC). An external filter capacitor is always required on these pins, see Section 13.2 “Power Sequencing” |
| VREFN | - | C2 | G12 | | - | - | - | ADC negative reference voltage. |
| VREFP | - | D2 | F12 | [5] | - | - | - | ADC positive reference voltage. |
| VDD1V8_1 | G9 | A13 | F8 | [5] | - | - | - | 1.8 V supply voltage for on-chip digital logic during active mode. In deep-sleep mode, this pin can be powered off to conserve additional current (~ 65 uA). |

Table 4. Pin description ...continued

| Symbol | 114-pin, WLCSP | 176-pin, VFBGA | 249-pin, FOWLP | Reset state [1] | Type | Function # | Description |
|---------|---|---|--|-----------------|------|------------|-------------------------|
| VSS | A1; A6; A11; B6; D6; E6; F8; F11; G6; J9; J11; L1; L7 | D5; D15; E12; E14; F7; F11; G6; H8; H9; H10; J8; J10; K8; K9; K10; L6; L12; M7; M11; M13; N14; P13 | A1; A17; C11; C15; C3; C7; E11; E7; G10; G11; G13; G14; G15; G3; G4; G5; G7; G8; H11; K11; K4; K7; L10; L11; L12; L13; L14; L15; L3; L4; L5; L6; L7; L8; M11; N11; N7; P11; R11; R15; R3; R7; U1; U17 | - | - | - | Ground. |
| VSSA | | C3, D12 | D7; D11 | - | - | - | Analog ground. |
| XTALIN | K9 | B14 | B4 | - | - | - | Main oscillator input. |
| XTALOUT | L9 | B13 | A4 | - | - | - | Main oscillator output. |

- [1] Z = high impedance; pull-up or pull-down disabled. AI = analog input. I = input. O = output. I/O = input/output. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes.
- [2] Pad with programmable glitch filter; provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See [Figure 21](#).
- [3] Pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. See [Figure 21](#).
- [4] These pins are intended for connection to an off-chip power management IC (PMIC) if such a device is used to supply power to core logic to this device. These pins may be used for other purposes if the on-chip regulator is used to supply power to core logic.

- [5] See [Section 13.1 “General operating conditions”](#) for specification of actual allowable voltage ranges.
- [6] On WLCSP114 package, USB ISP mode is not supported. VBUS pin is not available on the WLCSP114 package. To detect VBUS connection, user can connect a GPIO pin to the USB connector's VBUS. When a rising edge occurs on the GPIO pin, software should set bit 10 (FORCE_VBUS) and bit 16 (DCON) in the DEVCMDSTAT register.
- [7] On the WLCSP package, VDDA_ADC1V8 is internally connected to VDD1V8 pin; VDDA_BIAS is internally connected to VDDIO_0; VREFP is internally connected to VDD1V8; VREFN is internally connected to VSS; VSSA is internally connected to VSS.

8. Power Supply for pins

[Table 6](#) shows the GPIOs belonging to the specific VDDIO groups and VDD_AO1V8 domain. Each VDDIO supply pin may be supplied at different voltage levels as needed by the application and can be powered between 1.71 V to 3.6 V.

Table 5. Power Supply for pins

| Pin | GPIO pins |
|-----------|--|
| VDDIO_0 | PIO0_0 to PIO0_13 PIO1_11 to PIO1_29 PIO2_12 to PIO2_23 PIO3_25 to PIO3_31 PIO4_0 to PIO4_10 PIO7_24 to PIO7_31 |
| VDDIO_1 | PIO0_14 to PIO0_31 PIO1_0 to PIO1_10 PIO2_24 to PIO2_31 PIO3_0 to PIO3_24 PMIC_I2C_SCL PMIC_I2C_SDA |
| VDDIO_2 | PIO1_30 to PIO1_31 PIO2_0 to PIO2_11 |
| VDD_AO1V8 | RESETN LDO_ENABLE PMIC_IRQ_N PMIC_MODE0 and PMIC_MODE1 |

9. Termination of unused pins

Table 6 shows how to terminate pins that are **not** used in the application. In many cases, unused pins can be left unconnected since pins are default high Z state or can be configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 6. Termination of unused pins

| Pin | Default state ^[1] | Recommended termination of unused pins |
|------------------|------------------------------|--|
| All PION pins | I; Z | Leave unconnected. |
| PMIC_I2C_SCL/SDA | Z | Leave unconnected. |
| PMIC_IRQ_N | I; Z | Tie high if not used in the system. |
| PMIC_MODEn | O | Leave unconnected. |
| RESETN | I | Tie high if not used in the system. |
| RTCXIN | I | Tie to ground. |
| RTCXOUT | - | Leave unconnected. |
| USB1_DM/DP | - | Leave unconnected. |
| USB1_VBUS | - | Leave unconnected. |
| USB1_VDD3V3 | - | Leave unconnected. |
| VDD_AO1V8 | - | Tie to 1.8V power. |
| VDD_1V8 | - | Tie to 1.8V power. |
| VDD_1V8_1 | - | Tie to 1.8V power during active. Can be powered off during deep sleep mode to reduce current consumption by approximately 65 uA. |
| VDDA_ADC1V8 | - | Tie to 1.8V power. |
| VDDA_BIAS | - | Tie to 1.8 V power. |
| VREFN | - | Tie to VSS. |
| VREFP | - | Tie to VDDA_ADC1V8 |
| VSSA | - | Tie to VSS. |
| XTALIN | I | Tie to ground. |
| XTALOUT | - | Leave unconnected. |

[1] Z = Input, pull-up, and pull-down disabled; I = Input; O = Output

9.0.1 Pin states in different power modes

Table 7. Pin states in different power modes

| Pin | Active | Sleep | Deep-sleep | Deep power-down |
|---------------|--|-------|------------|-----------------|
| All PION pins | As configured in IOCON ^[1] . Default is Z (input, pull-up, and pull-down disable) | | | |
| PMIC_MODE0/1 | 00 | 00 | | |

[1] Default and programmed pin states are retained in sleep and deep-sleep.

10. Functional description

10.1 Architectural overview

The ARM Cortex-M33 includes two AHB-Lite buses, the system bus and the C-code bus. The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

A multi-layer AHB matrix connects the CPU buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals on different slave ports of the matrix to be accessed simultaneously by different bus masters. More information on the multilayer matrix can be found in [Section 10.12.1](#). Connections in the multilayer matrix are shown in [Figure 3](#). Note that while the AHB bus itself supports word, halfword, and byte accesses, not all AHB peripherals need or provide that support.

10.2 Arm Cortex-M33 processor

The Cortex-M33 is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The Cortex-M33 offers an instruction set based on Thumb@-2, low interrupt latency, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller, multiple core buses capable of simultaneous accesses, and a floating point unit.

The RT600 includes the Armv8-M Security Extension that adds security through code and data protection features.

Information about Cortex-M33 configuration options can be found in the user manual.

10.3 Arm Cortex-M33 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

10.4 Xtensa HiFi 4 advanced Audio Digital Signal Processor

The HiFi 4 Audio Engine is present on selected RT600 devices. The HiFi 4 is a highly optimized audio processor geared for efficient execution of audio and voice codecs and pre- and post-processing modules. It includes support for four 32x32-bit MACs, some support for 72-bit accumulators, limited ability to support eight 32x16-bit MACs, and the ability to issue two 64-bit loads per cycle. There is an floating point unit included, providing up to four single-precision IEEE floating point MACs per cycle. The HiFi 4 Audio Engine is a configuration option of the Xtensa LX6 processor. All HiFi 4 Audio Engine operations can be used as intrinsics in standard C/C++ applications.

Information about HiFi 4 DSP configuration options can be found in the user manual.

10.5 Memory Protection Unit (MPU)

The Cortex-M33 processor has a memory protection unit (MPU) that provides fine grain memory control, enabling applications to implement security privilege levels, separating code, data and stack on a task-by-task basis. Such requirements are critical in many embedded applications.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

10.6 Nested Vectored Interrupt Controller (NVIC) for Cortex-M33

The NVIC is an integral part of the Cortex-M33. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

10.6.1 Features

- Controls system exceptions and peripheral interrupts.
- Supports up to 58 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

10.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

10.7 System Tick timer (SysTick)

The Arm Cortex-M33 includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the FRO or the Cortex-M33 core clock.

10.8 PowerQuad Hardware Accelerator

The RT600 has a PowerQuad hardware accelerator for CMSIS DSP functions (fixed and floating point unit) with support of SDK software API faster execution of ARM CMSIS instruction set. The PowerQuad is a hardware accelerator targeting common calculations in DSP applications. With the assistance of the PowerQuad, the Cortex-M33 can be freed to perform other tasks. While the PowerQuad is executing the assigned computation task, the CM33 can prepare the next PowerQuad task, resulting in a pipeline of PowerQuad tasks.

10.9 On-chip static RAM

The RT600 supports 5 MB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

10.10 On-chip ROM

The 128 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-Application Programming (IAP) and In-System Programming (ISP).
- ROM-based USB drivers (HID, CDC, MSC, and DFU). Supports flash updates via USB. USB ISP mode is not supported in WLCSP114 package.
- Supports booting from valid USART, SPI, I2C, Octal/Quad SPI, HS USB, SD/eMMC.
- Legacy, Single, and Dual image boot.
- OTP API for programming OTP memory.
- Random Number Generator (RNG) API.

10.11 OTP

The RT600 contains up to 16 kB byte of on-time-programmable memory used for part configuration, key storage (as an alternative to PUF) and various other uses. The OTP contains pre-programmed factory configuration data such as on-chip oscillator calibration values, among other things. It may also be used by customer applications to configure some details of device operation, code signature values, aspects of device security, debug options, and boot options

10.12 Memory mapping

The RT600 incorporates several distinct memory regions. The APB peripheral area is 512 kB in size and is divided to allow for up to 64 peripherals. Each peripheral is allocated 4 kB of space simplifying the address decoding. The registers incorporated into the CPU, such as NVIC, SysTick, and sleep mode control, are located on the private peripheral bus.

The Arm Cortex-M33 processor has a single 4 GB address space.

10.12.1 AHB multilayer matrix

The RT600 uses a multi-layer AHB matrix to connect the CPU buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters. [Figure 4](#) shows details of the available matrix connections.

Remark: Attempted accesses by the CM33 to unused spaces between assigned memory and peripheral spaces generally cause an exception. For the HiFi4 this is not the case.

10.12.2 Memory Protection Unit (MPU)

The Cortex-M33 processor has a memory protection unit (MPU) that provides fine grain memory control, enabling applications to implement security privilege levels, separating code, data and stack on a task-by-task basis. Such requirements are critical in many embedded applications.

The MPU register interface is located on the private peripheral bus and is described in detail in Cortex-M33 DGUG — ARM Cortex-M33 Devices Generic User Guide

10.12.3 TrustZone and Cortex-M33 busing on this device

The implementation of ARM TrustZone on this device involves using address bit 28 to divide the address space into potential secure and non-secure regions. Address bit 28 is not decoded in memory access hardware, so each physical location appears in two places on whatever bus they are located on. Other hardware determines which kinds of accesses (including non-secure callable) are actually allowed for any particular address.

In addition, the shared RAM is generally expected to be used for both code and data, in different balance for different applications. Some applications may require a great deal of code and little data, others may require most of the shared RAM to be used for data. For this reason, the entire shared RAM appears on both the code bus and the data bus of the Cortex-M33. Code can be located at addresses that are on the code bus, data can be located at addresses that are on the data bus. As long as code and data are contained in shared RAM that is connected on different AHB matrix slave ports, each can be accessed simultaneously on the appropriate bus.

[Table 8](#) shows the overall mapping of the code and data buses for secure and non-secure accesses to various device resources. The block diagrams in [Figure 3 “Block diagram overview”](#) may also be useful in understanding the memory map.

In addition to the fixed mapping of secure and non-secure spaces, “checker” hardware present on all AHB matrix ports confirms the types of access allowed for each peripheral or memory range (with a granularity of 32 memory ranges for each port). This is described in more detail in RT6xx User Manual (please see RT6xx Trusted execution environment chapter)

Remark: In the peripheral description chapters of this manual, only the native (non-secure) base address is noted, secure base addresses can be found in this chapter or created algorithmically where needed.

Table 8. TrustZone and Cortex-M33 general mapping

| Start address | End address | TrustZone | CM-33 bus | CM-33 usage |
|---------------|-------------|------------|-----------|--|
| 0x0000 0000 | 0x0FFF FFFF | Non-secure | Code | Shared RAM, Boot ROM, OSPI memory mapped region. |
| 0x1000 0000 | 0x1FFF FFFF | Secure | Code | Same as above |
| 0x2000 0000 | 0x2FFF FFFF | Non-secure | Data | Shared RAM, CM33 access to HiFi 4 TCMs via inbound PIF. Non-cacheable FlexSPI memory mapped region for DSP only. |
| 0x3000 0000 | 0x3FFF FFFF | Secure | Data | Same as above |
| 0x4000 0000 | 0x4FFF FFFF | Non-secure | Data | AHB and APB peripherals. |
| 0x5000 0000 | 0x5FFF FFFF | Secure | Data | Same as above |

- [1] The HiFi 4 accesses shared RAM via a separate connection, not using the AHB matrix.
- [2] The size shown for peripherals spaces indicates the space allocated in the memory map, not the actual space used by the peripheral.
- [3] Some AHB and APB peripherals are not accessible to the HiFi 4.
- [4] Selected areas of secure regions may be marked as non-secure callable.

10.12.4 Links to specific memory map descriptions and tables:

- [Section 10.12.5 “Device overview”](#)

- [Section 10.12.6 “Cortex-M33 Memory overview”](#)
- [Section 10.12.7 “Shared RAM detail”](#)
- [Section 10.12.8 “APB peripherals”](#)
- [Section 10.12.9 “AHB peripherals”](#)
- [Section 10.12.10 “HiFi 4 memory map”](#)

10.12.5 Device overview

The RT600 incorporates several distinct memory regions. [Table 9](#) gives a simplified view of the overall map of the entire address space from the user program viewpoint following reset. The figure indicates the main address regions and how (or whether) they related to both the Cortex-M33 and the HiFi 4.

Table 9. Device overview memory map

| Start addr | End addr | Size | Cortex-M33 function | HiFi 4 function |
|-------------|-------------|----------------------------|---|--|
| 0x0000 0000 | 0x0047 FFFF | 4.5 MB | Shared RAM via the CM33 code bus (non-secure access). See Section 10.12.7 . | Shared RAM - cacheable access. See Section 10.12.10 . [1] |
| 0x0300 0000 | 0x0303 FFFF | 256 KB | Boot ROM (non-secure access). See Section 10.12.6 | - |
| 0x0800 0000 | 0x0FFF FFFF | 128 MB | FlexSPI memory mapped space with cache and on-the-fly AES decryption (non-secure access). See Section 10.12.6 . [2] | FlexSPI memory mapped space, cacheable. See Section 10.12.10 . [2] |
| 0x1000 0000 | 0x1047 FFFF | 4.5 MB | Shared RAM via the CM33 code bus (secure access). See Section 10.12.7 . [3] | - |
| 0x1300 0000 | 0x1303 FFFF | 256 KB | Boot ROM (secure access). See Section 10.12.6 | - |
| 0x1800 0000 | 0x1FFF FFFF | 128 MB | FlexSPI memory mapped space with cache and on-the-fly AES decryption (secure access). See Section 10.12.6 . | - |
| 0x2000 0000 | 0x2047 FFFF | 4.5 MB | Shared RAM via the CM33 data bus (non-secure access). See Section 10.12.7 . | Shared RAM - non-cacheable access. See Section 10.12.10 . [1] |
| 0x2400 0000 | 0x2400 FFFF | 64 KB | Cortex-M33 access to HiFi 4 data TCM via inbound PIF (non-secure access). See Section 10.12.6 . | HiFi 4 data TCM - 4 interleaved banks. See Section 10.12.10 . |
| 0x2402 0000 | 0x2402 FFFF | 64 KB | Cortex-M33 access to HiFi 4 instruction TCM via inbound PIF (non-secure access). See Section 10.12.6 . | HiFi 4 instruction TCM. See Section 10.12.10 . |
| 0x2800 0000 | 0x2FFF FFFF | 128 MB | - | FlexSPI memory mapped space, non-cacheable. See Section 10.12.10 . [2] |
| 0x3000 0000 | 0x3047 FFFF | 4.5 MB | Shared RAM via the CM33 data bus (secure access). See Section 10.12.7 . [3] | - |
| 0x3400 0000 | 0x3400 FFFF | 64 KB | Cortex-M33 access to HiFi 4 data TCM via inbound PIF (secure access). See Section 10.12.6 . | - |
| 0x3402 0000 | 0x3402 FFFF | 64 KB | Cortex-M33 access to HiFi 4 instruction TCM via inbound PIF (secure access). See Section 10.12.6 . | HiFi 4 instruction TCM. See Section 10.12.10 . |
| 0x4000 0000 | 0x4003 FFFF | 256 KB [4] | APB peripherals (non-secure access). See Section 10.12.8 . | APB peripherals. See Section 10.12.10 . [5] |
| 0x4010 0000 | 0x4015 FFFF | 400 KB [4] | AHB peripherals (non-secure access). See Section 10.12.9 . | AHB peripherals. See Section 10.12.10 . [5] |
| 0x5000 0000 | 0x5003 FFFF | 256 KB [4] | APB peripherals (secure access). See Section 10.12.8 . | - |
| 0x5010 0000 | 0x5015 FFFF | 400 KB [4] | AHB peripherals (secure access). See Section 10.12.9 . | - |

[1] The HiFi 4 accesses shared RAM via a separate connection, not using the AHB matrix.

[2] Access to the FlexSPI memory space can be enabled or disabled for the CM33 and the HiFi 4.

- [3] Selected areas of secure regions may be marked as non-secure callable.
- [4] The size shown for peripheral spaces indicates the space allocated in the memory map, not the actual space used by the peripheral.
- [5] Some AHB and APB peripherals are not accessible to the HiFi 4.

10.12.6 Cortex-M33 Memory overview

[Table 10](#) gives a more detailed memory map as seen by the Cortex-M33. The purpose of the four address spaces for the shared RAMs is outlined at the beginning of this chapter. The details of which shared RAM regions are on which AHB matrix slave ports can be seen here. Further details given in [Section 10.12.6](#).

Table 10. Cortex-M33 overview memory map

| AHB port | Non-secure start address | Non-secure end address | Secure start address | Secure end address | Function [1] |
|----------|--------------------------|------------------------|----------------------|--------------------|--|
| 2 | 0x0000 0000 | 0x0000 FFFF | 0x1000 0000 | 0x1000 FFFF | Shared RAM on CM33 code bus, partitions 0 to 1. |
| 3 | 0x0001 0000 | 0x0001 FFFF | 0x1001 0000 | 0x1001 FFFF | Shared RAM on CM33 code bus, partitions 2 to 3. |
| 4 | 0x0002 0000 | 0x0003 FFFF | 0x1002 0000 | 0x1003 FFFF | Shared RAM on CM33 code bus, partitions 4 to 7. |
| 5 | 0x0004 0000 | 0x0007 FFFF | 0x1004 0000 | 0x1007 FFFF | Shared RAM on CM33 code bus, partitions 8 to 11. |
| 6 | 0x0008 0000 | 0x000F FFFF | 0x1008 0000 | 0x100F FFFF | Shared RAM on CM33 code bus, partitions 12 to 15. |
| 7 | 0x0010 0000 | 0x001F FFFF | 0x1010 0000 | 0x101F FFFF | Shared RAM on CM33 code bus, partitions 16 to 19. |
| 8 | 0x0020 0000 | 0x002F FFFF | 0x1020 0000 | 0x102F FFFF | Shared RAM on CM33 code bus, partitions 20 to 23. |
| 9 | 0x0030 0000 | 0x003F FFFF | 0x1030 0000 | 0x103F FFFF | Shared RAM on CM33 code bus, partitions 24 to 27. |
| 10 | 0x0040 0000 | 0x0047 FFFF | 0x1040 0000 | 0x1047 FFFF | Shared RAM on CM33 code bus, partitions 28 to 29. |
| 0 | 0x0300 0000 | 0x0303 FFFF | 0x1300 0000 | 0x1303 FFFF | Boot ROM |
| 1 | 0x0800 0000 | 0x0FFF FFFF | 0x1800 0000 | 0x1FFF FFFF | FlexSPI memory mapped space with cache and on-the-fly AES decryption. |
| 2 | 0x2000 0000 | 0x2000 FFFF | 0x3000 0000 | 0x3000 FFFF | Shared RAM on CM33 data bus, partitions 0 to 1. |
| 3 | 0x2001 0000 | 0x2001 FFFF | 0x3001 0000 | 0x3001 FFFF | Shared RAM on CM33 data bus, partitions 2 to 3. |
| 4 | 0x2002 0000 | 0x2003 FFFF | 0x3002 0000 | 0x3003 FFFF | Shared RAM on CM33 data bus, partitions 4 to 7. |
| 5 | 0x2004 0000 | 0x2007 FFFF | 0x3004 0000 | 0x3007 FFFF | Shared RAM on CM33 data bus, partitions 8 to 11. |
| 6 | 0x2008 0000 | 0x200F FFFF | 0x3008 0000 | 0x300F FFFF | Shared RAM on CM33 data bus, partitions 12 to 15. |
| 7 | 0x2010 0000 | 0x201F FFFF | 0x3010 0000 | 0x301F FFFF | Shared RAM on CM33 data bus, partitions 16 to 19. |
| 8 | 0x2020 0000 | 0x202F FFFF | 0x3020 0000 | 0x302F FFFF | Shared RAM on CM33 data bus, partitions 20 to 23. |
| 9 | 0x2030 0000 | 0x203F FFFF | 0x3030 0000 | 0x303F FFFF | Shared RAM on CM33 data bus, partitions 24 to 27. |
| 10 | 0x2040 0000 | 0x2047 FFFF | 0x3040 0000 | 0x3047 FFFF | Shared RAM on CM33 data bus, partitions 28 to 29. |
| 11 | 0x2400 0000 | 0x240F FFFF | 0x3400 0000 | 0x340F FFFF | HiFi 4 inbound PIF. Allows AHB access to HiFi 4 Instruction and Data TCMS. |
| 12 | 0x4000 0000 | 0x4001 FFFF | 0x5000 0000 | 0x5001 FFFF | AHB to APB bridge 0 [2] |
| | 0x4002 0000 | 0x4003 FFFF | 0x5002 0000 | 0x5003 FFFF | AHB to APB bridge 1 [2] |
| 13 | 0x4010 0000 | 0x4011 FFFF | 0x5010 0000 | 0x5011 FFFF | AHB peripherals [3] |
| 14 | 0x4012 0000 | 0x4012 FFFF | 0x5012 0000 | 0x5012 FFFF | AHB peripherals [3] |
| 15 | 0x4013 0000 | 0x4013 FFFF | 0x5013 0000 | 0x5013 FFFF | AHB peripherals [3] |
| 16 | 0x4014 0000 | 0x4014 FFFF | 0x5014 0000 | 0x5014 FFFF | AHB peripherals [3] |
| 17 | 0x4015 0000 | 0x4015 FFFF | 0x5015 0000 | 0x5015 FFFF | AHB peripherals [3] |

[1] Gaps between AHB matrix slave ports are not shown.

[2] Details of this space may be found in [Section 10.12.8 "APB peripherals"](#).

[3] Details of this space may be found in [Section 10.12.9 "AHB peripherals"](#).

10.12.7 Shared RAM detail

[Table 11](#) reflects both the Cortex-M33 and DSP views of the RAM partitions and address. The AHB matrix port is only relevant to the Cortex-M33 because the DSP accesses these RAMs via a separate bus.

The partitions shown in [Table 11](#) are mirrored in all four shared RAM address regions for the Cortex-M33. The purpose of those regions is outlined in [Section 10.12.3](#), while [Table 12](#) gives the base addresses for the four regions.

A variety of shared RAM partition sizes are provided to allow more flexibility in assigning the uses of those spaces. For each application, shared RAM usage should be planned to minimize collision of accesses by the two buses of the Cortex-M33, as well as other bus masters, including DMA controllers and the HiFi 4.

A best case would be if each shared RAM partition is accessed by only one master at any particular time, “ownership” being passed to another master (for instance) when a buffer is filled from a peripheral, a block of data is processed by an algorithm, etc.

To summarize, access collisions can occur under the following conditions.

- On the AHB matrix: when two AHB masters access a resource on the same slave port at the same time. AHB masters include the HiFi 4 when it is using the AHB matrix, not when it is accessing shared RAM.
- HiFi 4 accessing shared RAM: when the HiFi 4 and an AHB master access the same shared RAM partition at the same time. Note that in this case, the access collision happens at the partition, not at the slave port. Since there are multiple partitions for each slave port, this allows even more opportunity to avoid collisions.

Table 11. Shared RAM memory map: offsets for all types of shared memory accesses

| AHB port | Partition | Start offset | End offset | Size |
|----------|-----------|--------------|------------|--------|
| 2 | 0 | 0x00 0000 | 0x00 7FFF | 32 KB |
| | 1 | 0x00 8000 | 0x00 FFFF | 32 KB |
| 3 | 2 | 0x01 0000 | 0x01 7FFF | 32 KB |
| | 3 | 0x01 8000 | 0x01 FFFF | 32 KB |
| 4 | 4 | 0x02 0000 | 0x02 7FFF | 32 KB |
| | 5 | 0x02 8000 | 0x02 FFFF | 32 KB |
| | 6 | 0x03 0000 | 0x03 7FFF | 32 KB |
| | 7 | 0x03 8000 | 0x03 FFFF | 32 KB |
| 5 | 8 | 0x04 0000 | 0x04 FFFF | 64 KB |
| | 9 | 0x05 0000 | 0x05 FFFF | 64 KB |
| | 10 | 0x06 0000 | 0x06 FFFF | 64 KB |
| | 11 | 0x07 0000 | 0x07 FFFF | 64 KB |
| 6 | 12 | 0x08 0000 | 0x09 FFFF | 128 KB |
| | 13 | 0x0A 0000 | 0x0B FFFF | 128 KB |
| | 14 | 0x0C 0000 | 0x0D FFFF | 128 KB |
| | 15 | 0x0E 0000 | 0x0F FFFF | 128 KB |

Table 11. Shared RAM memory map: offsets for all types of shared memory accesses

| AHB port | Partition | Start offset | End offset | Size |
|----------|-----------|--------------|------------|--------|
| 7 | 16 | 0x10 0000 | 0x13 FFFF | 256 KB |
| | 17 | 0x14 0000 | 0x17 FFFF | 256 KB |
| | 18 | 0x18 0000 | 0x1B FFFF | 256 KB |
| | 19 | 0x1C 0000 | 0x1F FFFF | 256 KB |
| 8 | 20 | 0x20 0000 | 0x23 FFFF | 256 KB |
| | 21 | 0x24 0000 | 0x27 FFFF | 256 KB |
| | 22 | 0x28 0000 | 0x2B FFFF | 256 KB |
| | 23 | 0x2C 0000 | 0x2F FFFF | 256 KB |
| 9 | 24 | 0x30 0000 | 0x33 FFFF | 256 KB |
| | 25 | 0x34 0000 | 0x37 FFFF | 256 KB |
| | 26 | 0x38 0000 | 0x3B FFFF | 256 KB |
| | 27 | 0x3C 0000 | 0x3F FFFF | 256 KB |
| 10 | 28 | 0x40 0000 | 0x43 FFFF | 256 KB |
| | 29 | 0x44 0000 | 0x47 FFFF | 256 KB |

Table 12. Base addresses for different types of shared memory accesses

| Base address | Cortex-M33 | HiFi 4 |
|--------------|-----------------------|---|
| 0x0000 0000 | Code bus - non-secure | Cacheable (see Section 10.12.10.1) |
| 0x1000 0000 | Code bus - secure | - |
| 0x2000 0000 | Data bus - non-secure | Non-cacheable (see Section 10.12.10.1) |
| 0x3000 0000 | Data bus - secure | - |

10.12.8 APB peripherals

[Table 13](#) provides details of the addresses for APB peripherals. APB peripherals have both secure and non-secure access possibilities, and are accessible by the HiFi 4 unless secured.

Table 13. APB peripherals memory map

| AHB port | APB bridge | Non-secure base address | Secure base address | Peripheral |
|----------|------------|-------------------------|---------------------|---|
| 12 | 0 | 0x4000 0000 | 0x5000 0000 | RSTCTL0. Reset control group 0. [1] |
| | | 0x4000 1000 | 0x5000 1000 | CLKCTL0. Clock control group 0. [1] |
| | | 0x4000 2000 | 0x5000 2000 | SYSCTL0. System control group 0. [1] |
| | | 0x4000 4000 | 0x5000 4000 | IOCON. Pin function selection and pin control setup. |
| | | 0x4000 6000 | 0x5000 6000 | PUF. Physical unclonable function cryptographic key generation. |
| | | 0x4000 E000 | 0x5000 E000 | WWDT0 (Windowed watchdog timer 0). |
| | | 0x4000 F000 | 0x5000 F000 | Utick (Micro-tick timer). |
| 1 | 0 | 0x4002 0000 | 0x5002 0000 | RSTCTL1. Reset control group 1. [1] |
| | | 0x4002 1000 | 0x5002 1000 | CLKCTL1. Clock control group 1. [1] |
| | | 0x4002 2000 | 0x5002 2000 | SYSCTL1. System control group 1. [1] |
| | | 0x4002 5000 | 0x5002 5000 | GPIO pin interrupts (PINT). |
| | | 0x4002 6000 | 0x5002 6000 | Input multiplexing controls. |
| | | 0x4002 8000 | 0x5002 8000 | CT32B0 (standard counter/timer 0). |
| | | 0x4002 9000 | 0x5002 9000 | CT32B1 (standard counter/timer 1). |
| | | 0x4002 A000 | 0x5002 A000 | CT32B2 (standard counter/timer 2). |
| | | 0x4002 B000 | 0x5002 B000 | CT32B3 (standard counter/timer 3). |
| | | 0x4002 C000 | 0x5002 C000 | CT32B4 (standard counter/timer 4). |
| | | 0x4002 D000 | 0x5002 D000 | MRT (Multi-Rate Timer). |
| | | 0x4002 E000 | 0x5002 E000 | WWDT1 (Windowed watchdog timer 1). |
| | | 0x4002 F000 | 0x5002 F000 | Frequency measure unit. |
| | | 0x4003 0000 | 0x5003 0000 | RTC & Wake-up timer. |
| | | 0x4003 6000 | 0x5003 6000 | I3C interface. |
| | | 0x4003 7000 | 0x5003 7000 | eSPI interface. |

[1] Reset, clock, and system control functions are separated into 2 groups to allow the possibility of securing group 0 while leaving group 1 unsecured.

10.12.9 AHB peripherals

[Table 14](#) provides details of the addresses for AHB peripherals. AHB peripherals have both secure and non-secure access possibilities. Some AHB matrix ports are accessible by the HiFi 4 (for peripherals that are not secure), some are accessible only by the Cortex-M33.

Table 14. AHB peripheral memory map

| AHB port | Non-secure base address | Secure base address | Accessible by HiFi 4? | Peripheral |
|----------|-------------------------|---------------------|-----------------------|---|
| 13 | 0x4010 0000 | 0x5010 0000 | Yes | High Speed GPIO (general purpose I/O for port pins that are not selected for some other function by IOCON). |
| | 0x4010 4000 | 0x5010 4000 | | DMA0 registers. |
| | 0x4010 5000 | 0x5010 5000 | | DMA1 registers. |
| | 0x4010 6000 | 0x5010 6000 | | Flexcomm Interface 0. |
| | 0x4010 7000 | 0x5010 7000 | | Flexcomm Interface 1. |
| | 0x4010 8000 | 0x5010 8000 | | Flexcomm Interface 2. |
| | 0x4010 9000 | 0x5010 9000 | | Flexcomm Interface 3. |
| | 0x4010 F000 | 0x5010 F000 | | Debug mailbox. |
| | 0x4011 0000 | 0x5011 0000 | | Message Unit A (Cortex-M33 port). |
| | 0x4011 1000 | 0x5011 1000 | | Message Unit B (HiFi 4 port). |
| | 0x4011 2000 | 0x5011 2000 | | Semaphore. |
| | 0x4011 3000 | 0x5011 3000 | | OS Event Timer 0 (for access by Cortex-M33). |
| | 0x4011 4000 | 0x5011 4000 | | OS Event Timer 1 (for access by HiFi 4). |
| 14 | 0x4012 0000 | 0x5012 0000 | Yes | CRC Engine. |
| | 0x4012 1000 | 0x5012 1000 | | D-MIC (8 channel PDM digital microphone interface) |
| | 0x4012 2000 | 0x5012 2000 | | Flexcomm Interface 4. |
| | 0x4012 3000 | 0x5012 3000 | | Flexcomm Interface 5. |
| | 0x4012 4000 | 0x5012 4000 | | Flexcomm Interface 6. |
| | 0x4012 6000 | 0x5012 6000 | | Flexcomm Interface 14 (High Speed SPI). |
| | 0x4012 7000 | 0x5012 7000 | | Flexcomm Interface 15 (PMIC I2C). |
| 15 | 0x4013 0000 | 0x5013 0000 | Yes | OTP Controller (One Time Programmable factory and user settings). |
| | 0x4013 4000 | 0x5013 4000 | | FlexSPI and OTFAD registers. |
| | 0x4013 5000 | 0x5013 5000 | | PMC (PMU control). |
| | 0x4013 6000 | 0x5013 6000 | | SDIO0 registers. |
| | 0x4013 8000 | 0x5013 8000 | | Random Number Generator. |
| | 0x4013 9000 | 0x5013 9000 | | ACMP0 (comparator). |
| | 0x4013 A000 | 0x5013 A000 | | ADC0. |
| | 0x4013 B000 | 0x5013 B000 | | HS USB PHY registers. |
| 16 | 0x4014 0000 | 0x5014 0000 | No | HS USB RAM interface. |
| | 0x4014 4000 | 0x5014 4000 | | HS USB device registers. |
| | 0x4014 5000 | 0x5014 5000 | | HS USB host registers. |
| | 0x4014 6000 | 0x5014 6000 | | SCTimer/PWM. |
| | 0x4014 8000 | 0x5014 8000 | | Security Control registers (AHB_SECURE_CTRL). |

Table 14. AHB peripheral memory map ...continued

| AHB port | Non-secure base address | Secure base address | Accessible by HiFi 4? | Peripheral |
|----------|-------------------------|---------------------|-----------------------|--|
| 17 | 0x4015 0000 | 0x5015 0000 | No | PowerQuad coprocessor. |
| | 0x4015 1000 | 0x5015 1000 | | Casper coprocessor. |
| | 0x4015 2000 | 0x5015 2000 | | Casper RAM interface. |
| | 0x4015 4000 | 0x5015 4000 | | Secure HS GPIO (alternate 32-bit GPIO facility that can be secured separately from the main GPIO). |
| | 0x4015 8000 | 0x5015 8000 | | Hash-AES registers. |

10.12.10 HiFi 4 memory map

[Table 15](#) provides a detailed memory map from the viewpoint of the HiFi 4.

Table 15. HiFi 4 overview memory map

| Cacheable start address [1] | Cacheable end address [1] | Non-cacheable start address [1] | Non-cacheable end address [1] | Function | Size | AHB port |
|---|---|---|---|---|--------|------------------------|
| 0x0000 0000 | 0x0000 7FFF | 0x2000 0000 | 0x2000 7FFF | Shared RAM partition 0. | 32 KB | 2 [2] |
| 0x0000 8000 | 0x0000 FFFF | 0x2000 8000 | 0x2000 FFFF | Shared RAM partition 1. | 32 KB | |
| 0x0001 0000 | 0x0001 7FFF | 0x2001 0000 | 0x2001 7FFF | Shared RAM partition 2. | 32 KB | 3 [2] |
| 0x0001 8000 | 0x0001 FFFF | 0x2001 8000 | 0x2001 FFFF | Shared RAM partition 3. | 32 KB | |
| 0x0002 0000 | 0x0002 7FFF | 0x2002 0000 | 0x2002 7FFF | Shared RAM partition 4. | 32 KB | 4 [2] |
| 0x0002 8000 | 0x0002 FFFF | 0x2002 8000 | 0x2002 FFFF | Shared RAM partition 5. | 32 KB | |
| 0x0003 0000 | 0x0003 7FFF | 0x2003 0000 | 0x2003 7FFF | Shared RAM partition 6. | 32 KB | |
| 0x0003 8000 | 0x0003 FFFF | 0x2003 8000 | 0x2003 FFFF | Shared RAM partition 7. | 32 KB | |
| 0x0004 0000 | 0x0004 FFFF | 0x2004 0000 | 0x2004 FFFF | Shared RAM partition 8. | 64 KB | 5 [2] |
| 0x0005 0000 | 0x0005 FFFF | 0x2005 0000 | 0x2005 FFFF | Shared RAM partition 9. | 64 KB | |
| 0x0006 0000 | 0x0006 FFFF | 0x2006 0000 | 0x2006 FFFF | Shared RAM partition 10. | 64 KB | |
| 0x0007 0000 | 0x0007 FFFF | 0x2007 0000 | 0x2007 FFFF | Shared RAM partition 11. | 64 KB | |
| 0x0008 0000 | 0x0009 FFFF | 0x2008 0000 | 0x2009 FFFF | Shared RAM partition 12. | 128 KB | 6 [2] |
| 0x000A 0000 | 0x000B FFFF | 0x200A 0000 | 0x200B FFFF | Shared RAM partition 13. | 128 KB | |
| 0x000C 0000 | 0x000D FFFF | 0x200C 0000 | 0x200D FFFF | Shared RAM partition 14. | 128 KB | |
| 0x000E 0000 | 0x000F FFFF | 0x200E 0000 | 0x200F FFFF | Shared RAM partition 15. | 128 KB | |
| 0x0010 0000 | 0x0013 FFFF | 0x2010 0000 | 0x2013 FFFF | Shared RAM partition 16. | 256 KB | 7 [2] |
| 0x0014 0000 | 0x0017 FFFF | 0x2014 0000 | 0x2017 FFFF | Shared RAM partition 17. | 256 KB | |
| 0x0018 0000 | 0x001B FFFF | 0x2018 0000 | 0x201B FFFF | Shared RAM partition 18. | 256 KB | |
| 0x001C 0000 | 0x001F FFFF | 0x201C 0000 | 0x201F FFFF | Shared RAM partition 19. | 256 KB | |
| 0x0020 0000 | 0x0023 FFFF | 0x2020 0000 | 0x2023 FFFF | Shared RAM partition 20. | 256 KB | 8 [2] |
| 0x0024 0000 | 0x0027 FFFF | 0x2024 0000 | 0x2027 FFFF | Shared RAM partition 21. | 256 KB | |
| 0x0028 0000 | 0x002B FFFF | 0x2028 0000 | 0x202B FFFF | Shared RAM partition 22. | 256 KB | |
| 0x002C 0000 | 0x002F FFFF | 0x202C 0000 | 0x202F FFFF | Shared RAM partition 23. | 256 KB | |
| 0x0030 0000 | 0x0033 FFFF | 0x2030 0000 | 0x2033 FFFF | Shared RAM partition 24. | 256 KB | 9 [2] |
| 0x0034 0000 | 0x0037 FFFF | 0x2034 0000 | 0x2037 FFFF | Shared RAM partition 25. | 256 KB | |
| 0x0038 0000 | 0x003B FFFF | 0x2038 0000 | 0x203B FFFF | Shared RAM partition 26. | 256 KB | |
| 0x003C 0000 | 0x003F FFFF | 0x203C 0000 | 0x203F FFFF | Shared RAM partition 27. | 256 KB | |
| 0x0040 0000 | 0x0043 FFFF | 0x2040 0000 | 0x2043 FFFF | Shared RAM partition 28. | 256 KB | 10 [2] |
| 0x0044 0000 | 0x0047 FFFF | 0x2044 0000 | 0x2047 FFFF | Shared RAM partition 29. | 256 KB | |
| 0x2400 0000 | 0x2400 FFFF | - | - | Data TCM - in 4 interleaved banks. | 64 KB | 11 [2] |
| 0x2402 0000 | 0x2402 FFFF | - | - | Instruction TCM (includes the default vector table) | 64 KB | |
| - | - | 0x4000 0000 | 0x4001 FFFF | AHB to APB bridge 0 | 128 KB | 12 |
| - | - | 0x4002 0000 | 0x4003 FFFF | AHB to APB bridge 1 | 128 KB | |
| - | - | 0x4010 0000 | 0x4011 FFFF | AHB peripherals [3] | 128 KB | 13 |
| - | - | 0x4012 0000 | 0x4012 FFFF | AHB peripherals [3] | 64 KB | 14 |
| - | - | 0x4013 0000 | 0x4013 FFFF | AHB peripherals | 64 KB | 15 |

- [1] This is a suggested configuration of cacheable and non-cacheable regions, See [Section 10.12.10.1](#) below.
- [2] The HiFi 4 does not use AHB to access this space.
- [3] AHB peripherals on other AHB matrix ports are not accessible to the HiFi 4. See [Section 10.12.9 "AHB peripherals"](#).

10.12.10.1 Using cacheable and non-cacheable memory regions

The cacheable and non-cacheable regions indicated in the table above and elsewhere in this chapter are recommended (not forced by hardware) in order to insure that the TCMs are not in cacheable space. If this is not done, TCM accesses will use additional power while providing no performance improvement. Cacheable and non-cacheable regions may be user configured via software tools (e.g. the linker used to create HiFi 4 code), and at run time via API calls.

The recommended configuration allows the user to control cache usage for the large shared memory via the two logical address ranges that access the same physical memories. By selecting the address for specific memory usage (as shown in [Table 15](#)), the cache will, or will not, be used for that access.

For example, HiFi4 code may always be placed at cacheable addresses. Data that is accessed as a long sequential stream (and therefore not useful to cache) may be placed in non-cacheable addresses. Avoiding the cache when it is not needed will save power and leave more cache space for operations that can take advantage of it.

In addition, cacheing certain areas, such as data that is altered through a different path such as DMA, or peripheral registers, can cause improper operation.

10.13 System control

10.13.1 Clock sources

The RT600 supports three external and three internal clock sources:

- 12 Mhz Free Running Oscillator
- 48/60 MHz Free Running Oscillator (FRO).
- 1 MHz Low-Power Internal Oscillator.
- Crystal oscillator.
- 32 kHz Crystal Oscillator
- External Clock Input pin (50 MHz maximum)

10.13.1.1 12 MHz Free Running Oscillator (FRO)

The FRO 12 MHz oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage. This FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes

10.13.1.2 48/60 MHz Free Running Oscillator (FRO)

Selectable 48 MHz or 60 MHz FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.

10.13.1.3 1 MHz Low-Power oscillator

The 1 MHz oscillator provides an ultra low-power, low-frequency clock source that can be used to clock a variety of functions including the Watchdog Timer (WWDT) and the OSTimer. It can also be used as the main system clock for low-power operation.

The 1 MHz Low Power oscillator is accurate to +/-10% over temperature.

10.13.1.4 Crystal oscillator

The main crystal oscillator on the RT600 can be used with crystal frequencies from 4 MHz to 25 MHz. The crystal oscillator may be used to drive a PLL to achieve higher clock rates.

One aspect of the oscillator high gain mode is that a larger voltage swing is used at the crystal pin. This gives a higher noise immunity within the oscillator and less edge to edge jitter of the internal clock. When high gain mode is not required, power used by the crystal oscillator can be reduced by using low power mode.

Remark: High gain mode requires a 1 megohm resistor to be inserted in series. See [Section 16.4](#). For this reason, high gain mode and low power mode cannot both be used in the same application. The board design must reflect the mode that will be used.

10.13.1.5 32 kHz oscillator

The 32KHz oscillator resides in the “always-on” domain and is used to drive the Real Time Clock. It is also available for use for a variety of other purposes including low-power UART operation or as the main system clock for very low frequency operation.

10.13.2 System PLL (PLL0)

The system PLL accepts an input clock frequency in the range of 32.768 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

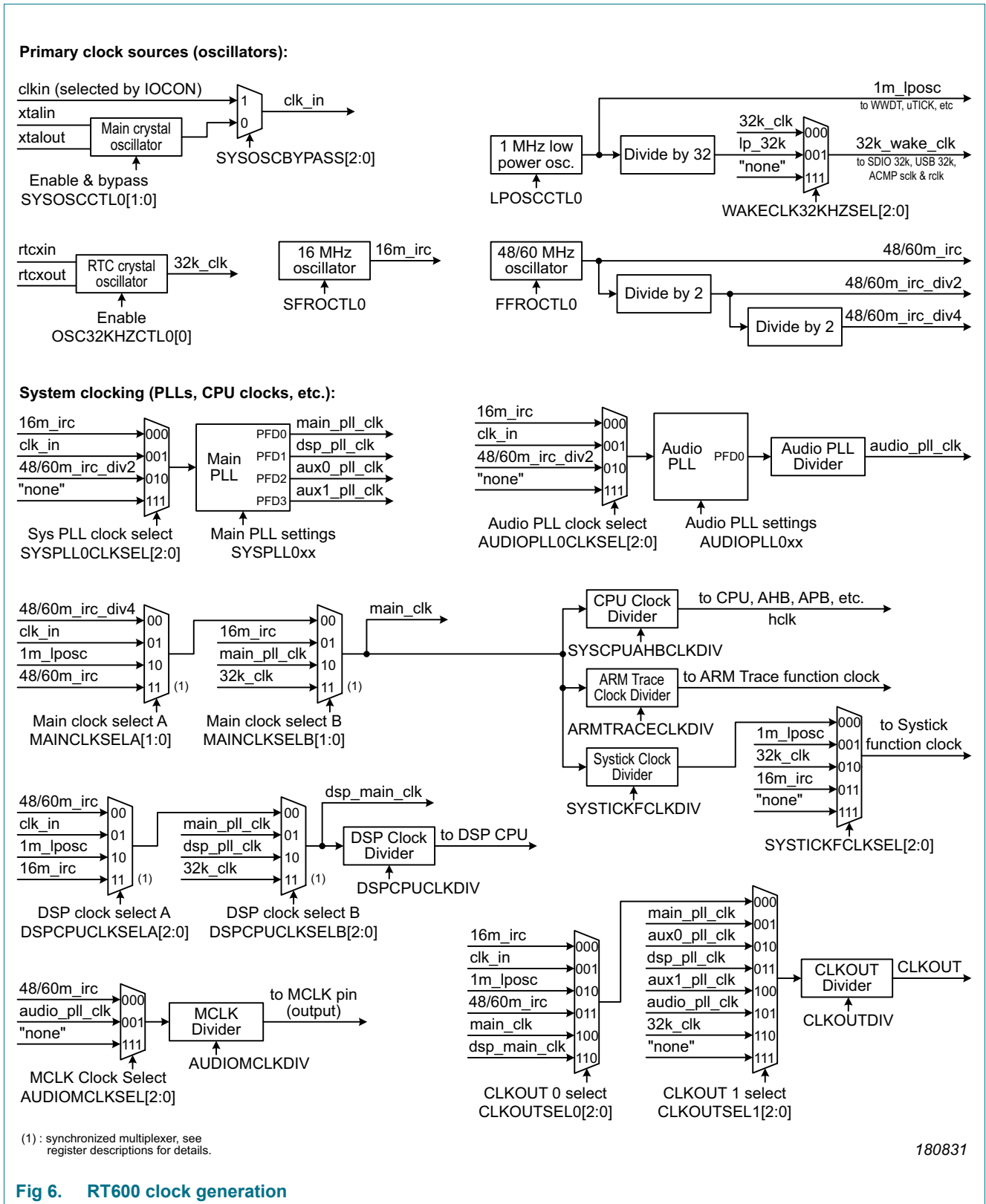
The PLL can be enabled or disabled by software.

10.13.3 Audio PLL (PLL2)

The audio PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

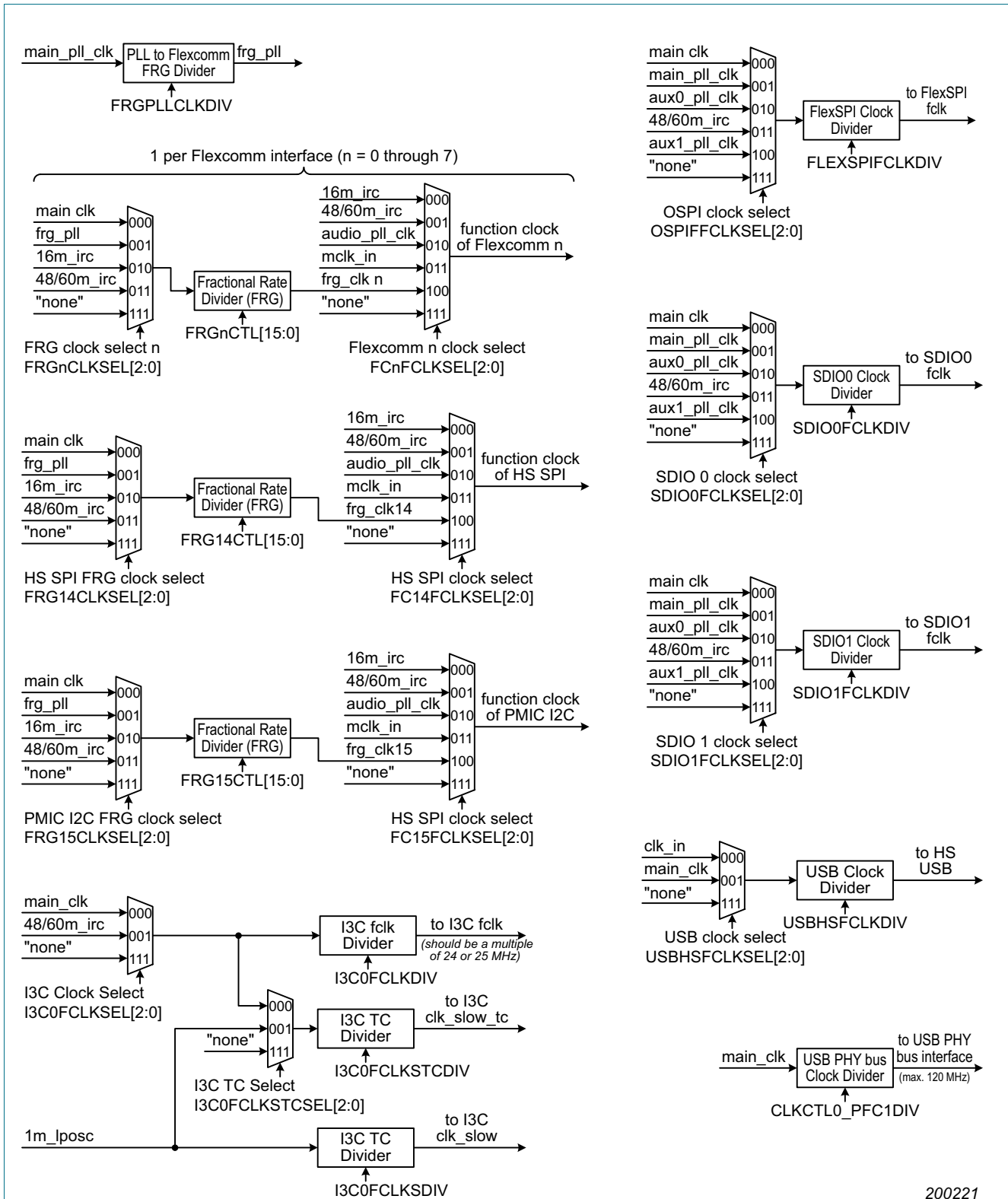
The PLL can be enabled or disabled by software.

10.13.4 Clock Generation



180831

Fig 6. RT600 clock generation



200221

Fig 7. RT600 clock generation (continued)

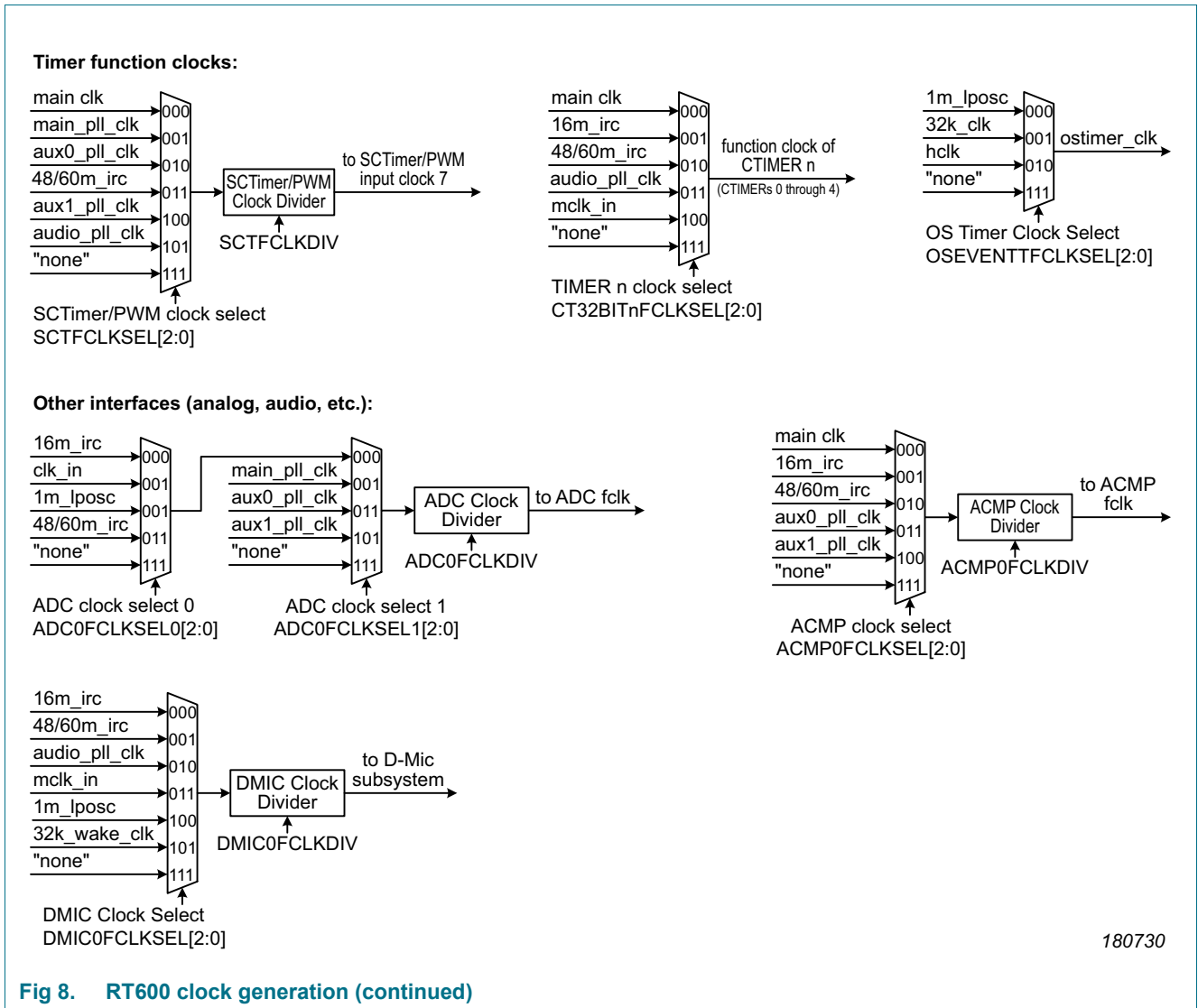


Fig 8. RT600 clock generation (continued)

10.13.5 Safety

The RT600 includes a Windowed WatchDog Timer (WWDT), which can be enabled by software after reset. Once enabled, the WWDT remains locked and cannot be modified in any way until a reset occurs.

10.14 Power control

The RT600 supports a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be adjusted for power consumption. In addition, there are individual power-down controls for many (particularly analog) peripherals. Finally, any set of individual shared Ram partitions may be placed in retain/standby mode or powered-off entirely. This selection can be made on a partition-by-partition basis.

In addition, there are three special modes of processor power reduction with different peripherals running: sleep mode, deep-sleep mode, and deep power-down mode that can be activated using the power API library from the SDK software package.

10.14.1 Sleep mode

There are independent sleep modes for each of the two CPUs. In sleep mode, the system clock to that CPU is stopped and execution of instructions is suspended until either a reset or an interrupt occurs. Peripheral functions, if selected to be clocked can continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

10.14.2 Deep-sleep mode

In deep-sleep mode, the system clock to the processor is disabled as in sleep mode. All analog blocks are powered down by default but can be selected to keep running through the power API if needed as wake-up sources. The main clock and all peripheral clocks are disabled. The FRO is disabled.

Deep-sleep mode eliminates all power used by analog peripherals and all dynamic power used by the processor itself, memory systems and related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

GPIO Pin Interrupts, GPIO Group Interrupts, and selected peripherals such as USB0, USB1, DMIC, SPI, I2C, USART, WWDT, RTC, Micro-tick Timer, and BOD can be left running in deep sleep mode. The FRO, RTC oscillator, and the watchdog oscillator can be left running. In some cases, DMA can operate in deep-sleep mode. For more details, see RT600 user manual.

10.14.3 Deep power-down mode and Full Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the RTC power domain, the RESET pin, and the PMIC_IRQ_N pin. The RT600 can wake up from deep power-down mode via the RESET pin, the RTC alarm, and the PMIC_IRQ_N pin. The ALARM1HZ flag in RTC control register generates an RTC wake-up interrupt request, which can wake up the part. During deep power-down mode, the contents of the SRAM and registers are not retained. All functional pins are tri-stated in deep power-down mode.

In deep power-down mode, all rails can remained powered and supply to the VDDCORE supply can be powered down. In full deep power-down mode, all rails can be powered off and the VDD_AO18 supply can remain powered.

10.14.4 Peripheral configuration in reduced power modes

[Table 16](#) shows the peripheral configuration in reduced power modes.

Table 16. Peripheral configuration in reduced power modes

| Peripheral/Clock | Reduced power mode | | |
|------------------------|---------------------|---------------------|--------------------------------|
| | Sleep | Deep-sleep | Deep power-down ^[2] |
| 1m_lposc | Software configured | Software configured | Off |
| 16m_irc | Software configured | Software configured | Off |
| 48/60m_irc | Software configured | Software configured | Off |
| Crystal oscillator | Software configured | Software configured | Off |
| RTC and RTC oscillator | Software configured | Software configured | Software configured |

Table 16. Peripheral configuration in reduced power modes

| Peripheral/Clock | Reduced power mode | | |
|---------------------------|---------------------|------------------------------------|--------------------------------|
| | Sleep | Deep-sleep | Deep power-down ^[2] |
| System PLL | Software configured | Software configured | Off |
| Audio PLL | Software configured | Software configured | Off |
| SRAM memory arrays | Software configured | Software configured | Off |
| SRAM periphery | Software configured | Software configured | Off |
| Boot ROM | On | Off | Off |
| Other digital peripherals | Software configured | Software configured | Off |
| A to D converter | Software configured | Software configured | Off |
| Analog Comparator | Software configured | Software configured ^[1] | Off |

[1] The comparator may be on in deep-sleep mode, but cannot generate a wake-up interrupt.

[2] Applies to both deep power-down and full deep power-down modes.

Table 17 shows typical wake-up sources for reduced power modes.

Table 17. Wake-up sources for reduced power modes

| Power mode | Wake-up source | Comment |
|----------------------|---|--|
| Sleep | Any peripheral that can cause an interrupt in sleep mode | [1][2] |
| | HWWAKE | Flexcomm Interfaces and DMIC subsystem activity. [4] |
| Deep-sleep | Pin interrupts | [1][2][3] |
| | Watchdog interrupt | Only WDT0 can generate a wake-up from deep-sleep mode. [1][2][3] |
| | Watchdog reset | Only WDT0 can generate a chip reset. [1] |
| | Reset pin | No configuration needed. |
| | RTC 1 Hz alarm timer | [1][2][3] |
| | RTC_ALARM, RTC_WAKE | [1][2][3] |
| | Micro-tick timer | Note: the Micro-tick timer is specifically targeted for ultra-low power wake-up from deep-sleep mode [1][2][3] |
| | OS Event Timer | [1][2][3] |
| | Flexcomm USART | Interrupt from USART in slave or 32 kHz mode. [1][2][3] |
| | Flexcomm SPI | Interrupt from SPI in slave mode. [1][2][3] |
| | Flexcomm I2C | Interrupt from I2C in slave mode. [1][2][3] |
| | Flexcomm I2S | Interrupt from I2S in slave mode. [1][2][3] |
| | I3C | Interrupt from I3C in slave mode. [1][2][3] |
| | USB need clock | Interrupt from USB when activity is detected that requires a clock. [1][2][3][4] |
| | DMA | See DMA controller chapter in UM for details of DMA-related interrupts. [1][2][3] |
| | DMA controllers | [1][2][3] |
| | DMIC | [1][2][3] |
| | HWWAKE | Certain Flexcomm Interface and DMIC subsystem activity. [4] |
| | Quad/octal SPI | [1][2][3] |
| | SDIO | [1][2][3] |
| | HASH-AES | [1][2][3] |
| | CASPER | [1][2][3] |
| | PowerQuad | [1][2][3] |
| | A to D converter | [1][2][3] |
| HiFi4 DSP | [2][3][5] | |
| Deep power-down | RTC_ALARM, RTC_WAKE | [1][2][3] |
| | Reset pin | No configuration needed. |
| Full deep power-down | Same as deep power-down except that external power must be restored prior to wake-up. | |

- [1] See specific peripheral chapter for basic configuration.
- [2] The related interrupt must be enabled in the NVIC.
- [3] Enable related function in the and STARTEN0 or STARTEN1 register.
- [4] See Hardware Wake-up control register in UM
- [5] Typically via the Message Unit interrupt. See Inter-CPU communications in UM chapter.

10.15 General Purpose I/O (GPIO)

The RT600 provides GPIO ports with a total of up to 147 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

10.15.1 Features

- Accelerated GPIO functions:
 - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
 - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
 - All GPIO registers are byte and half-word addressable.
 - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- One GPIO group interrupt can be triggered by a combination of any pin or pins.

10.16 Pin interrupt/pattern engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the I/O+ bus for fast single-cycle access.

10.16.1 Features

- Pin interrupts:
 - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
 - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
 - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
 - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
 - Pin interrupts can wake up the device from sleep mode and deep-sleep mode.
- Pattern match engine:
 - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
 - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
 - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
 - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
 - Pattern match engine facilitates wake-up only from active and sleep modes.

10.17 Communications peripherals

10.17.1 High-speed USB Host/Device interface (USB1)

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

10.17.1.1 USB1 device controller

The device controller enables 480 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

Features

- Fully compliant with *USB 2.0 Specification* (high speed).
- Supports 12 physical (6 logical) endpoints with up to 8 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.

- While USB is in the Suspend mode, the RT600 can enter one of the reduced power modes and wake up on USB activity.
- Double buffer implementation for Bulk and Isochronous endpoints.

10.17.1.2 USB1 host controller

The host controller enables high speed data exchange with USB devices attached to the bus. It consists of register interface and serial interface engine. The register interface complies with the Enhanced Host Controller Interface (EHCI) specification.

Features

- EHCI compliant.
- Two downstream ports.
- Supports per-port power switching.

10.17.2 FlexSPI Flash Interface

The Flexible Serial Peripheral Interface (FlexSPI) host controller supports up to two SPI channels and up to 4 external devices. Each channel supports Single/Dual/Quad/Octal mode data transfer (1/2/4/8 bidirectional data lines).

FlexSPI flash interface with 32 KB cache and dynamic decryption for execute-in-place and supports DMA.

10.17.2.1 Features

- Flexible sequence engine (LUT table) to support various vendor devices.
 - Serial NOR Flash or other device with similar SPI protocol as Serial NOR Flash
 - Serial NAND Flash
 - HyperBus device (HyperFlash/HyperRAM)
 - FPGA device
- Flash access mode
 - Single/Dual/Quad/Octal mode
 - SDR/DDR mode
 - Individual/Parallel mode
- Support sampling clock mode:
 - Internal dummy read strobe looped back internally
 - Internal dummy read strobe looped back from pad
 - Flash provided read strobe
- Automatic Data Learning to select correct sample clock phase
- Memory mapped read/write access by AHB Bus
 - AHB RX Buffer implemented to reduce read latency. Total AHB RX Buffer size: 256 * 64 Bits
 - 16 AHB masters supported with priority for read access
 - 8 flexible and configurable buffers in AHB RX Buffer

- AHB TX Buffer implemented to buffer all write data from one AHB burst. AHB TX Buffer size: 8 * 64 Bits
- All AHB masters share this AHB TX Buffer. No AHB master number limitation for Write Access.
- Software triggered Flash read/write access by IP Bus
 - IP RX FIFO implemented to buffer all read data from External device. FIFO size: 64 * 64 Bits
 - IP TX FIFO implemented to buffer all Write data to External device. FIFO size: 128 * 64 Bits
 - DMA support to fill IP TX FIFO
 - DMA support to read IP RX FIFO
 - SCLK stopped when reading flash data and IP RX FIFO is full
 - SCLK stopped when writing flash data and IP TX FIFO is empty

10.17.3 SD/eMMC Interfaces

SD/eMMC memory card interface is available with dedicated DMA controller. Supports the eMMC 5.0 standard including HS400 DDR mode. HS-400 is supported on SD port 0 only.

10.17.4 Flexcomm Interface serial communication

10.17.4.1 Features

- USART with asynchronous operation or synchronous master or slave operation.
- SPI master or slave, with up to 4 slave selects.
- I²C, including separate master, slave, and monitor functions.
- Two I2S functions using Flexcomm Interface 6 and Flexcomm Interface 7.
- Data for USART, SPI, and I2S traffic uses the Flexcomm Interface FIFO. The I²C function does not use the FIFO.

10.17.4.2 SPI serial I/O controller (Flexcomm Interfaces 0 - 7)

Features

- Excluding delays introduced by external device and PCB, The maximum supported bit rate for SPI master mode (transmit/receive) is 25 Mbit/s and the maximum supported bit rate for SPI slave mode (transmit/receive) is 25 Mbit/s.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software or DMA set-up.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- Four Slave Select input/outputs with selectable polarity and flexible usage.
- Activity on the SPI in slave mode allows wake-up from deep-sleep mode on any enabled interrupt.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

10.17.4.3 I²C-bus interface

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

Features

- All I2Cs support standard, Fast-mode, and Fast-mode Plus with data rates of up to 1 Mbit/s.
- All I2Cs support high-speed slave mode with data rates of up to 3.4 Mbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I²C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I²C-bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Activity on the I2C in slave mode allows wake-up from deep-sleep mode on any enabled interrupt.

10.17.4.4 USART

Features

- Excluding delays introduced by external device and PCB, the maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 20 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 20.0 Mbit/s.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.

- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

10.17.4.5 I²S-bus interface

The I²S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I²S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the RT600, the I²S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of the Flexcomm Interface implements four I²S channel pairs.

The I²S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I²S signals, and are configured together for either transmit or receive operation, using the same mode, same data configuration and frame configuration. All such channel pairs can participate in a time division multiplexing (TDM) arrangement. For cases requiring an MCLK input and/or output, this is handled outside of the I²S block in the system level clocking scheme.

Features

- A Flexcomm Interface may implement one or more I²S channel pairs, the first of which could be a master or a slave, and the rest of which would be slaves. All channel pairs are configured together for either transmit or receive and other shared attributes. The number of channel pairs is defined for each Flexcomm Interface, and may be from 0 to 4.
- Configurable data size for all channels within one Flexcomm Interface, from 4 bits to 32 bits. Each channel pair can also be configured independently to act as a single channel (mono as opposed to stereo operation).
- All channel pairs within one Flexcomm Interface share a single bit clock (SCK) and word select/frame trigger (WS), and data line (SDA).
- Data for all I²S traffic within one Flexcomm Interface uses the Flexcomm Interface FIFO. The FIFO depth is 8 entries.
- Left justified and right justified data modes.

- DMA support using FIFO level triggering.
- TDM (Time Division Multiplexing) with a several stereo slots and/or mono slots is supported. Each channel pair can act as any data slot. Multiple channel pairs can participate as different slots on one TDM data line.
- The bit clock and WS can be selectively inverted.
- Sampling frequencies supported depends on the specific device configuration and applications constraints (for example, system clock frequency and PLL availability.) but generally supports standard audio data rates. See the data rates section in I²S chapter in the RT6xx user manual to calculate clock and sample rates.

10.17.5 High-Speed SPI interface (Flexcomm Interface 14)

An additional, stand-alone SPI module is provided. This will be a high-speed SPI able to provide 50 MHz transfer rates. Functionally, it is identical to the SPI Flexcomm interfaces 0 to 7. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode (transmit/receive) is 50 Mbit/s. The maximum supported bit rate for SPI slave mode (receive) is 50Mbit/s and for SPI slave mode (transmit) is 35 Mbit/s.

10.17.6 I3C interface

The MIPI Alliance Improved Inter-Integrated Circuit (MIPI I3C) brings major improvements in use and power over I2C, and provides an alternative to SPI for mid-speed applications. The I3C bus is designed to support future sensor interface architectures, widely expected in Internet-of-Things applications.

The I3C bus is intended to be used by microcontrollers (MCU) and application processors (AP) to connect to sensors, actuators, and other MCUs (as slaves). Connecting an MCU to other MCUs and connecting an AP to an MCU are considered to be the major use cases.

10.17.6.1 Features

- In-band interrupts: interrupts can go from Slave to Master without extra wires, such that the Master knows which Slave sent the interrupt.
- In-band command codes (Common Command Codes (CCC))
- Dynamic addressing
- Multi-master / multi-drop
- Hot-Join
- I2C compatibility. Note that I2C compatibility has limitations. Please refer to user manual for further details.

10.18 Counter/timer peripherals

10.18.1 General-purpose 32-bit timers/external event counter

The RT600 includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

10.18.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to four 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins may vary by device.
- Four 32-bit match registers that allow:
 - Continuous operation with optional interrupt generation on match.
 - Stop timer on match with optional interrupt generation.
 - Reset timer on match with optional interrupt generation.
 - Shadow registers are added for glitch-free PWM output.
- For each timer, up to four external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins may vary by device):
 - Set LOW on match.
 - Set HIGH on match.
 - Toggle on match.
 - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to four match registers can be configured for PWM operation, allowing up to three single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins may vary by device.)

10.18.2 SCTimer/PWM

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable.
- Limit, halt, stop, and start conditions.
- Values of Match/Capture registers, plus reload or capture control values.

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

10.18.2.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs, interrupts, and the SCTimer/PWM states.
 - Match register 0 can be used as an automatic limit.
 - In bi-directional mode, events can be enabled based on the count direction.
 - Match events can be held until another qualifying event occurs.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:
 - 8 inputs
 - 10 outputs
 - 16 match/capture registers
 - 16 events
 - 32 states
- PWM capabilities including dead time and emergency abort functions

10.18.3 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

A separate Watchdog Timer is provided for each of the two CPUs.

10.18.3.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.

- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from $(T_{cy(WDCLK)} \times 256 \times 4)$ to $(T_{cy(WDCLK)} \times 2^{24} \times 4)$ in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the WDOSC as the clock source.

10.18.4 Real Time Clock (RTC) timer

The RTC timer is a 32-bit timer which counts down from a preset value to zero. At zero, the preset value is reloaded and the counter continues. The RTC timer uses the 32.768 kHz clock input to create a 1 Hz or 1 kHz clock. Selectable on-chip crystal load capacitors are available for the RTC Oscillator.

10.18.5 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

10.18.5.1 Features

- 24-bit interrupt timer.
- Four channels independently counting down from individually set values.
- Repeat and one-shot interrupt modes.

10.18.6 OS/Event Timer

An OS/EVENT Timer module will provide a common time-base between the two CPUs for event synchronization and time-stamping.

The OS/EVENT Timer is comprised of a shared, free-running counter readable by each CPU and individual match and capture registers for each CPU.

The shared and local counters in this module will be implemented using Gray code. This will enable them to be read asynchronously by the processing domains.

The main counter in the OS/EVENT Timer module begins counting immediately following power-up and continues counting through any subsequent system resets (except those caused by a new POR).

10.18.6.1 Features

- 64-bit Gray code counter. Using Gray code means that the timer can run at a frequency unrelated to either CPU clock and can still be read by either CPU without a synchronization delay. Gray code is a reflected binary code that changes in a single bit position for each increment.
- Separate functions for each CPU:
- A capture register can copy the main counter value when triggered by a CPU request.
- A match register can be compared to the main counter and can optionally generate an interrupt or wake-up event

10.18.7 Micro-Tick Timer

A 32-bit MicroTick timer that runs from the 1 MHz low-power oscillator. This timer can wake up the device from reduced power modes up to deep-sleep, with extremely low power consumption. The MicroTick timer has an added timestamp feature in the form of 4 capture registers.

10.18.7.1 Features

- Ultra simple, ultra-low power timer that can run and wake up the device in reduced power modes other than deep power-down.
- Write once to start.
- Interrupt or software polling.
- Four capture registers that can be triggered by external pin transitions.

10.19 Other digital peripherals

10.19.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

Two identical DMA controllers are provided on the RT600. The user may elect to dedicate one of these to the Cortex M-33 CPU and the other for use by the DSP CPU and/or one may be used as a secure DMA the other non-secure.

10.19.1.1 Features

- One channel per on-chip peripheral direction: typically one for input and one for output for most peripherals.
- DMA operations can optionally be triggered by on- or off-chip events.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

10.19.2 DMIC subsystem

10.19.2.1 Features

- Pulse-Density Modulation (PDM) data input for left and/or right channels on 1 or 2 buses.
- Flexible decimation.
- 16 entry FIFO for each channel.
- DC blocking or unaltered DC bias can be selected.

- Data can be transferred using DMA from deep-sleep mode without waking up the CPU, then automatically returning to deep-sleep mode.
- Data can be streamed directly to I²S on Flexcomm Interface 7.

10.19.3 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

10.19.3.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
 - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
 - CRC-16: $x^{16} + x^{15} + x^2 + 1$
 - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1's complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
 - 8-bit write: 1-cycle operation.
 - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
 - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

10.20 Analog peripherals

10.20.1 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 5 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the Arm TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCTimer/PWM inputs for tight timing control between the ADC and the SCTimer/PWM.

10.20.1.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing among up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).

- 12-bit conversion rate of 5.0 Msamples/s. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

10.20.2 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

10.20.3 Analog Comparator

The comparator (CMP) module provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage, known as rail-to-rail operation.

10.21 Security features

The security system on RT600 has a set of hardware blocks and ROM code to implement the security features of the device. The hardware consists of an AES engine, a SHA engine (Hash-AES block), a random number generator, and a key storage block that keys from an SRAM based PUF (Physically Unclonable Function). All components of the system can be accessed by the processor or the DMA engine to encrypt or decrypt data and for hashing. The ROM is responsible for secure boot in addition to providing support for various security functions.

10.21.1 Features

- Trust Zone M
- AES256 Decryption Engine.
- SHA-1, SHA-2 HASH Engine.
- Physical Unclonable Function (PUF) Key Generation.
- CASPER security Cortex-M33 co-processor.
- Random number generator (RNG).
- On-the-Fly Decryption on Octal/Quad0 SPI interface.
- Universally Unique Identifier (UUID)
- Device Identifier Composition Engine (DICE)

10.21.2 AES256

RT600 devices provide an on-chip hardware AES encryption and decryption engine to protect the image content and to accelerate processing for data encryption or decryption, data integrity, and proof of origin. Data can be encrypted or decrypted by the AES engine using a key from the PUF or a software supplied key.

10.21.3 SHA-1 and SHA-2

The Hash peripheral is used to perform SHA-1 and SHA-2 (256) based hashing. A hash takes an arbitrarily large message or image and forms a relatively small fixed size “unique” number called a digest. The data is fed by words from the processor, DMA, or hosted access; the words are converted from little-endian (Arm standard) to big-endian (SHA standard) by the block.

10.21.3.1 Features

- Used with an HMAC to support a challenge/response or to validate a message.
- Can be used to verify external memory that has not been compromised.

10.21.4 PUF

The PUF controller provides a secure key storage without injecting or provisioning device unique PUF root key.

10.21.4.1 Features

- Key strength of 256 bits. The PUF constructs 256-bit strength device unique PUF root key using the digital fingerprint of a device derived from SRAM and error correction data called Activation Code (AC). The AC is generated during enrollment process and must be stored on external non-volatile memory device in the system.
- Generation, storage, and reconstruction of keys.
- Key sizes from 64 bits to 4096 bits. PUF controller allows storage of keys, generated externally or on chip, of sizes 64 bits to 4096 bits
- PUF controller allows to assign a 4-bit index value for each key while generating key codes. Keys that are assigned index value zero are output through HW bus, accessible to AES engine and OTFAD block only. Keys with non-zero index are available through APB register interface

10.21.5 CASPER co-processor

The Cryptographic Accelerator (CASPER) engine provides acceleration of asymmetric cryptographic algorithms. When the Cryptographic Accelerator (CASPER) is used in conjunction with hardware blocks for hashing and symmetric cryptography, significant performance can be achieved. Supported crypto functions are implemented in the SDK (Software Development Kit) and the mbed TLS examples utilize the CASPER peripheral for computations.

10.21.6 Random Number Generator (RNG)

Random Number Generators (RNG) are used for cryptographic, modeling, and simulation applications, which employ keys that must be generated in a random fashion.

10.21.7 On-the-Fly Decryption on Octal/Quad SPI interface (OTFAD)

The OTFAD function provides AES-128 Counter Mode On-the-Fly Decryption of external data located on the Quad/octal SPI flash interface (QuadSPI) interface.

10.21.8 Universally Unique Identifier (UUID)

The RT600 stores a 128-bit IETF RFC4122 compliant non-sequential Universally Unique Identifier (UUID). It can be read from registers SYSCTL0_UUID0 through SYSCTL0_UUID3

10.21.9 Device Identifier Composition Engine (DICE)

The RT600 supports Device Identifier Composition Engine (DICE) to provide Composite Device Identifier (CDI). CDI value would be available in registers SYSCTL0DICEHWREG0 through SYSCTL0DICEHWREG7 for consumption after boot completion. It is recommended to overwrite these registers once ephemeral key-pairs are generated using this value.

10.22 Emulation and debugging

Debug and trace functions are integrated into the Arm Cortex-M33. Serial wire debug and trace functions are supported. The Arm Cortex-M33 is configured to support up to eight breakpoints and four watch points.

The Arm SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

11. Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|--------------------|---|---|-----|------|-------|------|
| VDD_AO1V8 | Supply 1.8 V supply for "always on" features. | | [2] | -0.3 | 1.98 | V |
| VDD1V8 | 1.8 V supply voltage for on-chip analog functions other than the ADC and comparator. | | [2] | -0.3 | 1.98 | V |
| VDD1V8_1 | 1.8 V supply voltage for on-chip digital logic | | [2] | -0.3 | 1.98 | V |
| VDDCORE | Power supply for core logic | On-chip regulator not used. Power supplied by an off-chip power management IC (PMIC). | [2] | -0.3 | 1.155 | V |
| VDDIO_0/1/2 | Supply voltage for GPIO pins | | [2] | -0.3 | 3.96 | V |
| VDDA_ADC1V8 | 1.8 V analog supply voltage for ADC and comparator. | | [2] | -0.3 | 1.98 | V |
| VDDA_BIAS | Bias for ADC and comparator for 0 V to 1.8 V input range. Must equal to max input voltage | | [2] | -0.3 | 3.96 | V |
| VREFP | ADC positive reference voltage | | [2] | -0.3 | 1.98 | V |
| USB1_VDD3V3 | USB1 analog 3.3 V supply | | [2] | -0.3 | 3.96 | V |
| I _{DD} | supply current (VFBGA176) | per VDDIO pin, 1.71 V ≤ V _{DDIO} < 2.7 V | [3] | - | 100 | mA |
| | supply current (VFBGA176) | per VDDIO pin, 2.7 V ≤ V _{DDIO} < 3.6 V | [3] | - | 100 | mA |
| | supply current (WLCSP114) | per VDDIO pin, 1.71 V ≤ V _{DDIO} < 2.7 V | [3] | - | 100 | mA |
| | supply current (WLCSP114) | per VDDIO pin, 2.7 V ≤ V _{DDIO} < 3.6 V | [3] | - | 100 | mA |
| | supply current (FOWLP249) | per VDDIO pin, 1.71 V ≤ V _{DDIO} < 2.7 V | [3] | - | 100 | mA |
| | supply current (FOWLP249) | per VDDIO pin, 2.7 V ≤ V _{DDIO} < 3.6 V | [3] | - | 100 | mA |
| I _{SS} | ground current (VFBGA176) | 1.71 V ≤ V _{DDIO} < 2.7 V | [3] | - | 100 | mA |
| | ground current (VFBGA176) | 2.7 V ≤ V _{DDIO} < 3.6 V | [3] | - | 100 | mA |
| | ground current (WLCSP114) | 1.71 V ≤ V _{DDIO} < 2.7 V | [3] | - | 100 | mA |
| | ground current (WLCSP114) | 2.7 V ≤ V _{DDIO} < 3.6 V | [3] | - | 100 | mA |
| | ground current (FOWLP249) | 1.71 V ≤ V _{DDIO} < 2.7 V | [3] | - | 100 | mA |
| | ground current (FOWLP249) | 2.7 V ≤ V _{DDIO} < 3.6 V | [3] | - | 100 | mA |
| I _{latch} | I/O latch-up current | -(0.5V _{DD}) < V _I < (1.5V _{DD}); T _j < 125 °C | | - | 100 | mA |
| T _{stg} | storage temperature | | | -55 | 150 | °C |

Table 18. Limiting values ...continuedIn accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------------|---------------------------------------|--|-----|-----|------|------|
| $T_{j(max)}$ | maximum junction temperature | | | - | 105 | °C |
| $P_{tot(pack)}$ | total power dissipation (per package) | VFBGA176, based on package heat transfer, not device power consumption | [5] | - | 1 | W |
| $P_{tot(pack)}$ | total power dissipation (per package) | WLSCP114, based on package heat transfer, not device power consumption | [5] | - | 1 | W |
| V_{ESD} | electrostatic discharge voltage | human body model; all pins | [4] | - | 2000 | V |

[1] The following applies to the limiting values:

- a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
 - b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
 - c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in [Table 30](#).
- [2] Maximum/minimum voltage above the maximum operating voltage (see [Table 30](#)) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.
- [3] The peak current should not exceed the total supply current.
- [4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 k Ω series resistor.
- [5] Determined in accordance to JEDEC JESD51-2A natural convection environment (still air).

12. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD} . The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications. Determined in accordance to JEDEC JESD51-2A natural convection environment (still air). Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

Table 19. Thermal resistance [\[1\]](#)

| Symbol | Parameter | Conditions | Max/Min | Unit |
|-------------------------|---|---------------------------|---------|------|
| VFBGA176 Package | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | JESD51-9, 2s2p, still air | 32.8 | °C/W |

- [1] Determined in accordance to JEDEC JESD51-2A natural convection environment (still air). Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

13. Static characteristics

13.1 General operating conditions

Table 20. General operating conditions

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-------------------------|--|---|------|--------------------|-------|------|
| f_{clk} | CPU (Cortex-M33) clock frequency | | - | - | 300 | MHz |
| | CPU (Cortex-M33) clock frequency | For USB high-speed device and host operations | 90 | - | 300 | MHz |
| | CPU (Cortex-M33) clock frequency | For USB full-speed device and host operations | 12 | - | 300 | MHz |
| f_{clk} | DSP clock frequency | | - | - | 600 | MHz |
| VDD_AO1V8 | Supply 1.8 V supply for "always on" features. | | 1.71 | - | 1.89 | V |
| VDD1V8 | 1.8 V supply voltage for on-chip analog functions other than the ADC and comparator. | | 1.71 | - | 1.89 | V |
| VDD1V8_1 ^[4] | 1.8 V supply voltage for on-chip digital logic | | 1.71 | - | 1.89 | V |
| VDDCORE ^[3] | Power supply for core logic. On-chip regulator not used. Power supplied by an off-chip power management IC (PMIC). | Retention Mode | 0.7 | - | 1.155 | V |
| | | Active Mode (M33 Max Freq = 75 MHz, FBB) | 0.7 | - | - | V |
| | | Active Mode (M33 Max Freq = 155 MHz, FBB) | 0.8 | - | - | V |
| | | Active Mode (M33 Max Freq = 220 MHz, FBB) | 0.9 | - | - | V |
| | | Active Mode (M33 Max Freq = 275 MHz, FBB) | 1.0 | - | - | V |
| | | Active Mode (M33 Max Freq = 300 MHz, FBB) | 1.13 | - | - | V |
| VDDCORE ^[3] | Power supply for core logic. On-chip regulator not used. Power supplied by an off-chip power management IC (PMIC). | Active Mode (DSP Max Freq = 100 MHz, FBB) | 0.7 | - | - | V |
| | | Active Mode (DSP Max Freq = 240 MHz, FBB) | 0.8 | - | - | V |
| | | Active Mode (DSP Max Freq = 370 MHz, FBB) | 0.9 | - | - | V |
| | | Active Mode (DSP Max Freq = 480 MHz, FBB) | 1.0 | - | - | V |
| | | Active Mode (DSP Max Freq = 600 MHz, FBB) | 1.13 | - | - | V |
| VDDIO_0/1/2 | supply voltage for GPIO rail | | 1.71 | - | 3.6 | V |
| VDDA_1V8 | 1.8 V analog supply voltage for ADC and comparator. | | 1.71 | - | 1.89 | V |

Table 20. General operating conditions ...continued

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--------------------------|--------------------------------|------------|------|--------------------|------|------|
| VDDA_BIAS ^[2] | Bias for ADC and comparator | | 1.71 | - | 3.6 | V |
| VREFP | ADC positive reference voltage | | 1.71 | - | 1.89 | V |
| USB1_VDD3V3 | USB1 analog 3.3 V supply | | 3.0 | - | 3.6 | V |

- [1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.
- [2] VDD_BIAS must be connected to the highest VDDIO rail voltage used for the ADC input channel or comparator inputs.
- [3] The maximum frequency for the specified VDDCORE voltage is the frequency of the main clock. This is before the CPU CLOCK Divider. Please see [Figure 6](#). The VDDCORE voltage has to be set according to the chosen main clock frequency.
- [4] 1.8 V supply voltage for on-chip digital logic during active mode. In deep-sleep mode, this pin can be powered off to conserve additional current (~ 65 uA).

Table 21. General operating conditions

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-------------------------|--|---|------|--------------------|-------|------|
| f _{clk} | CPU (Cortex-M33) clock frequency | | - | - | 300 | MHz |
| | CPU (Cortex-M33) clock frequency | For USB high-speed device and host operations | 90 | - | 300 | MHz |
| | CPU (Cortex-M33) clock frequency | For USB full-speed device and host operations | 12 | - | 300 | MHz |
| f _{clk} | DSP clock frequency | | - | - | 580 | MHz |
| VDD_AO1V8 | Supply 1.8 V supply for “always on” features. | | 1.71 | - | 1.89 | V |
| VDD1V8 | 1.8 V supply voltage for on-chip analog functions other than the ADC and comparator. | | 1.71 | - | 1.89 | V |
| VDD1V8_1 ^[4] | 1.8 V supply voltage for on-chip digital logic | | 1.71 | - | 1.89 | V |
| VDDCORE ^[3] | Power supply for core logic. On-chip regulator not used. Power supplied by an off-chip power management IC (PMIC). | Retention Mode | 0.7 | - | 1.155 | V |
| | | Active Mode (M33 Max Freq = 65 MHz, FBB) | 0.7 | - | - | V |
| | | Active Mode (M33 Max Freq = 140 MHz, FBB) | 0.8 | - | - | V |
| | | Active Mode (M33 Max Freq = 210 MHz, FBB) | 0.9 | - | - | V |
| | | Active Mode (M33 Max Freq = 270 MHz, FBB) | 1.0 | - | - | V |
| | | Active Mode (M33 Max Freq = 300 MHz, FBB) | 1.13 | - | - | V |

Table 21. General operating conditions ...continued*T_{amb} = -20 °C to +70 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--------------------------|--|---|------|--------------------|------|------|
| VDDCORE ^[3] | Power supply for core logic. On-chip regulator not used. Power supplied by an off-chip power management IC (PMIC). | Active Mode (DSP Max Freq = 65 MHz, FBB) | 0.7 | - | - | V |
| | | Active Mode (DSP Max Freq = 220 MHz, FBB) | 0.8 | - | - | V |
| | | Active Mode (DSP Max Freq = 350 MHz, FBB) | 0.9 | - | - | V |
| | | Active Mode (DSP Max Freq = 455 MHz, FBB) | 1.0 | - | - | V |
| | | Active Mode (DSP Max Freq = 580 MHz, FBB) | 1.13 | - | - | V |
| VDDIO_0/1/2 | supply voltage for GPIO rail | | 1.71 | - | 3.6 | V |
| VDDA_1V8 | 1.8 V analog supply voltage for ADC and comparator. | | 1.71 | - | 1.89 | V |
| VDDA_BIAS ^[2] | Bias for ADC and comparator | | 1.71 | - | 3.6 | V |
| VREFP | ADC positive reference voltage | | 1.71 | - | 1.89 | V |
| USB1_VDD3V3 | USB1 analog 3.3 V supply | | 3.0 | - | 3.6 | V |

- [1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.
- [2] VDD_BIAS must be connected to the highest VDDIO rail voltage used for the ADC input channel or comparator inputs.
- [3] The maximum frequency for the specified VDDCORE voltage is the frequency of the main clock. This is before the CPU CLOCK Divider. Please see [Figure 6](#). The VDDCORE voltage has to be set according to the chosen main clock frequency.
- [4] 1.8 V supply voltage for on-chip digital logic during active mode. In deep-sleep mode, this pin can be powered off to conserve additional current (~ 65 uA).

13.2 Power Sequencing

Following power-on sequence should be followed when using the internal LDO in the RT600:

1. VDD_AO1V8, VDD1V8, and VDD1V8_1 pins should be powered first. There is no power sequence requirement between powering the VDD_AO1V8 and VDD1V8 pins.
2. VDDA_ADC1V8 and VREFP can be powered concurrently with VDD_AO1V8 and VDD1V8 or later.
3. VDDIO_x and VDDA_BIAS pins can be powered concurrently with VDD_AO1V8 and VDD1V8 if these pins are 1.8 V range or later if these pins are 3.3 V range.

The VDDCORE pin will be supplied from the internal LDO and the LDO is powered from the VDD1V8. An external capacitor (4.7 uF) must be connected on the VDDCORE pin.

USB1_VDD3V3 can be powered at any time, independent of the other supplies.

Following power-on sequence should be followed when using an external PMIC or external IC to drive the VDDCORE pin (internal LDO is disabled, see timing diagram below):

1. VDD_AO1V8, VDD1V8, and VDD1V8_1 pins should be powered first. There is no power sequence requirement between powering the VDD_AO1V8 and VDD1V8 pins.
2. VDDA_ADC1V8 and VREFP can be powered concurrently with VDD_AO1V8 and VDD1V8 or later.
3. VDDIO_x and VDDA_BIAS pins can be powered concurrently with VDD1V8 if these pins are 1.8 V range or later if these pins are 3.3 V range.
4. Power up the VDDCORE. The external RESETN should be held low until VDDCORE is valid in the timing diagram. VDDCORE should not be ramped up until after all the other supplies have completed ramp up.

USB1_VDD3V3 can be powered at any time, independent of the other supplies.

Sequence of operations is handled internally so there is no specific timing requirement between the supplies. The time delays caused by any of the bypass capacitors will have no effect on the operation of the part. The internal POR detectors on VDD_AO1V8, VDD1V8 pins, and the Low Voltage Detector on VDDCORE pin, require a fall time of at least 10us (preliminary) to trigger. There is no restriction on the rise time, except for the sequencing defined above.

Table 22. Power-on characteristics

$T_{amb} = -20\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}.$

| Symbol | Timing Parameter | Description | Min | Max | Unit |
|--------|---|--|-----|-----|------|
| A | VDDIO_x valid to VDDCORE valid | The delay from when the IO pad voltages become valid to core voltage valid. | 10 | - | μs |
| B | VDDCORE valid to De-assertion of RESETN | The delay from when the VDD core is valid to when the RESETN can be released. | 20 | - | μs |
| AA | Mode pin valid | When the mode pins becomes valid. On power-on, the mode pins are reset to 00 and are controlled via a POR circuit in the always-on domain. The timing is from when the VDD_AO1V8 is valid to when the mode pins are reset to 00. | - | 2 | μs |

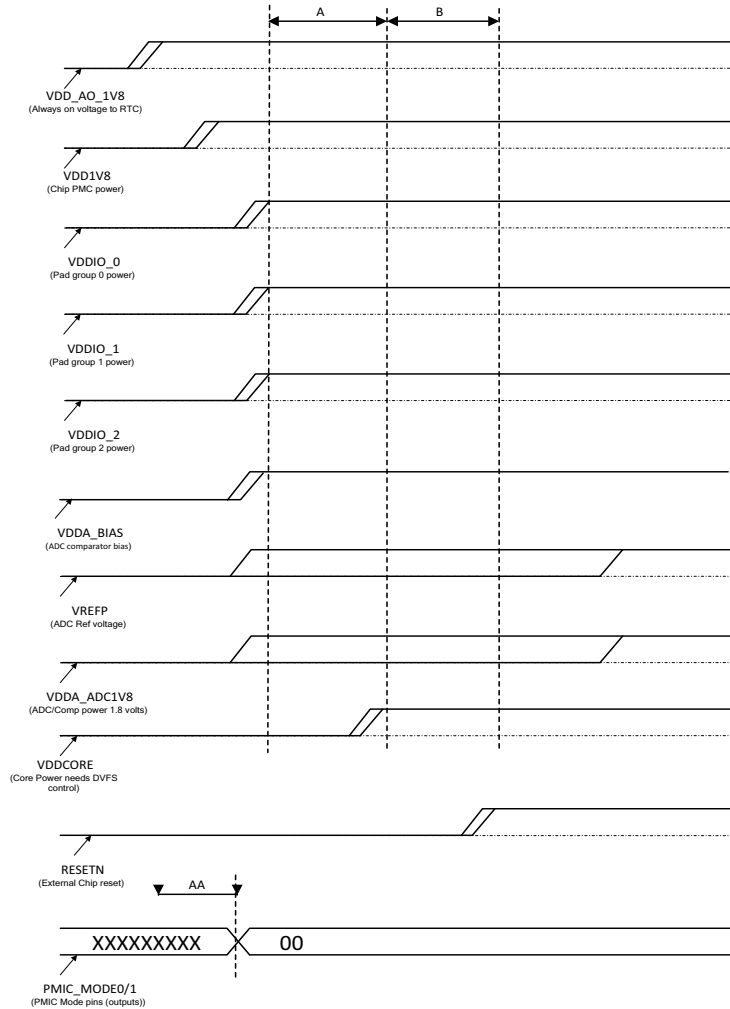


Fig 9. Power-up ramp

13.3 CoreMark data

Table 23. CoreMark score

$T_{amb} = 25\text{ }^{\circ}\text{C}$

| Parameter | Conditions | | Typ [3][4][5] | Unit |
|--|---|---------------------------|-------------------------------|----------------------|
| ARM Cortex-M33 in active mode, DSP no clock | | | | |
| CoreMark score | CoreMark code executed from SRAM; CCLK = 12 MHz, VDDCORE = 0.7 V | [1][6][7] | 3.87 | (Iterations/s) / MHz |
| | CCLK = 48 MHz, VDDCORE = 0.7 V | [1][6][7] | 3.87 | (Iterations/s) / MHz |
| | CCLK = 60 MHz, VDDCORE = 0.7 V | [1][6][7] | 3.87 | (Iterations/s) / MHz |
| | CCLK = 80 MHz, VDDCORE = 0.8 V | [2][6][7] | 3.87 | (Iterations/s) / MHz |
| | CCLK = 110 MHz, VDDCORE = 0.8 V | [2][6][7] | 3.87 | (Iterations/s) / MHz |
| | CCLK = 144 MHz, VDDCORE = 0.9 V | [2][6][7] | 3.87 | (Iterations/s) / MHz |
| | CCLK = 180 MHz, VDDCORE = 0.9 V | [2][6][7] | 3.87 | (Iterations/s) / MHz |
| | CCLK = 204 MHz, VDDCORE = 0.9 V | [2][6][7] | 3.87 | (Iterations/s) / MHz |
| | CCLK = 240 MHz, VDDCORE = 1.0 V | [2][6][7] | 3.87 | (Iterations/s) / MHz |
| | CCLK = 270 MHz, VDDCORE = 1.0 V | [2][6][7] | 3.87 | (Iterations/s) / MHz |
| | CCLK = 300 MHz, VDDCORE = 1.13 V | [2][6][7] | 3.87 | (Iterations/s) / MHz |

- [1] Clock source IRC. PLL disabled.
- [2] Clock source external clock to XTALIN (bypass mode). PLL enabled.
- [3] Characterized through bench measurements using typical samples.
- [4] Compiler settings: IAR C/C++ Compiler for Arm ver 8.32.3, High, Speed, No Size Constraints.
- [5] VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2 = VDDA_ADC1V8 = 1.8 V. VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3 V.
- [6] The frequency for the specified VDDCORE voltage is the frequency of the main clock. This is before the CPU CLOCK Divider. Please see [Figure 6](#). The VDDCORE voltage has to be set according to the chosen main clock frequency.
- [7] 4.5 MB SRAM enabled. All peripheral clocks disabled (set to NONE). All Array Power enabled (PDRUNCFG 1/2 registers). Only SRAM partition 12 access enabled (SYSCTL0_AHB_SRAM_ACCESS_DISABLE register). SYSCPUAHBCLKDIV = 0x0.

13.4 Power consumption

Table 24. Static characteristics: Power consumption in active mode

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ [2][4][5] | Max | Unit |
|--|------------------------|--|---------------------------|-------------------------------|-----|------|
| Cortex-M33 in Active mode, DSP no clock [1] | | | | | | |
| I _{DDVDDCORE} | VDDCORE supply current | enhanced while (1) code executed from SRAM; Internal LDO disabled CCLK = 12 MHz, VDDCORE = 0.7 V | [3][6][7] | - | 3.0 | - mA |
| | | CCLK = 48 MHz VDDCORE = 0.7 V | [3][6][7] | - | 6.0 | - mA |
| | | CCLK = 60 MHz VDDCORE = 0.7 V | [3][6][7] | - | 7.0 | - mA |
| | | CCLK = 80 MHz VDDCORE = 0.8 V | [6][7][8] | - | 10 | - mA |
| | | CCLK = 110 MHz VDDCORE = 0.8 V | [6][7][8] | - | 13 | - mA |

Table 24. Static characteristics: Power consumption in active mode ...continued

$T_{amb} = -20\text{ °C to }+70\text{ °C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^{[2][4][5]} | Max | Unit |
|--------|-----------|------------------------------------|-----------|--------------------------|-----|------|
| | | CCLK = 144 MHz VDDCORE = 0.9 V | [6][7][8] | - | 19 | - mA |
| | | CCLK = 180 MHz VDDCORE = 0.9 V | [6][7][8] | - | 23 | - mA |
| | | CCLK = 204 MHz VDDCORE = 0.9 V | [6][7][8] | - | 26 | - mA |
| | | CCLK = 240 MHz VDDCORE = 1.0 V | [6][7][8] | - | 34 | - mA |
| | | CCLK = 270 MHz VDDCORE = 1.0 V | [6][7][8] | - | 38 | - mA |
| | | CCLK = 300 MHz VDDCORE = 1.13 V | [6][7][8] | - | 50 | - mA |

- [1] Based on the power API library from the SDK software package available on nxp.com.
- [2] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2 = VDDA_ADC1V8 = 1.8 V. VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3 V
- [3] Clock source IRC. PLL disabled.
- [4] Characterized through bench measurements using typical samples.
- [5] Compiler settings: Keil Compiler for Arm ver 5.28, optimization level 3
- [6] The frequency for the specified VDDCORE voltage is the frequency of the main clock. This is before the CPU CLOCK Divider. Please see [Figure 6](#). The VDDCORE voltage has to be set according to the chosen main clock frequency.
- [7] 4.5 MB SRAM enabled. All peripheral clocks disabled (set to NONE). All Array Power enabled (PDRUNCFG 1/2 registers). Only SRAM partition 12 access enabled (SYSCTL0_AHB_SRAM_ACCESS_DISABLE register). SYSCPUAHBCLKDIV = 0x0.
- [8] Clock source external clock to XTALIN (bypass mode). PLL enabled.

Table 25. Static characteristics: Power consumption in active mode

$T_{amb} = -20\text{ °C to }+70\text{ °C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^{[2][4][5]} | Max | Unit |
|--|------------------------|--|-----------|--------------------------|-----|------|
| Cortex-M33 in Active mode, DSP no clock^[1] | | | | | | |
| I _{DDVDDCORE} | VDDCORE supply current | Coremark code executed from SRAM; Internal LDO disabled CCLK = 12 MHz, VDDCORE = 0.7 V | [3][6][7] | - | 3 | - mA |
| | | CCLK = 48 MHz VDDCORE = 0.7 V | [3][6][7] | - | 6 | - mA |
| | | CCLK = 60 MHz VDDCORE = 0.7 V | [3][6][7] | - | 7 | - mA |
| | | CCLK = 80 MHz VDDCORE = 0.8 V | [6][7][8] | - | 11 | - mA |
| | | CCLK = 110 MHz VDDCORE = 0.8 V | [6][7][8] | - | 14 | - mA |
| | | CCLK = 144 MHz VDDCORE = 0.9 V | [6][7][8] | - | 20 | - mA |

Table 25. Static characteristics: Power consumption in active mode ...continued

$T_{amb} = -20\text{ °C to }+70\text{ °C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^{[2][4][5]} | Max | Unit |
|--------|-----------|------------------------------------|-----------|--------------------------|-----|------|
| | | CCLK = 180 MHz VDDCORE = 0.9 V | [6][7][8] | - | 25 | - mA |
| | | CCLK = 204 MHz VDDCORE = 0.9 V | [6][7][8] | - | 28 | - mA |
| | | CCLK = 240 MHz VDDCORE = 1.0 V | [6][7][8] | - | 36 | - mA |
| | | CCLK = 270 MHz VDDCORE = 1.0 V | [6][7][8] | - | 40 | - mA |
| | | CCLK = 300 MHz VDDCORE = 1.13 V | [6][7][8] | - | 51 | - mA |

- [1] Based on the power API library from the SDK software package available on nxp.com.
- [2] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2 = VDDA_ADC1V8 = 1.8 V. VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3 V
- [3] Clock source IRC. PLL disabled.
- [4] Characterized through bench measurements using typical samples.
- [5] Compiler settings: IAR C/C++ Compiler for Arm ver 8.32.3, High, Speed, No Size Constraints
- [6] The frequency for the specified VDDCORE voltage is the frequency of the main clock. This is before the CPU CLOCK Divider. Please see [Figure 6](#). The VDDCORE voltage has to be set according to the chosen main clock frequency.
- [7] 4.5 MB SRAM enabled. All peripheral clocks disabled (set to NONE). All Array Power enabled (PDRUNCFG 1/2 registers). Only SRAM partition 12 access enabled (SYSCTL0_AHB_SRAM_ACCESS_DISABLE register). SYSCPUAHBCLKDIV = 0x0.
- [8] Clock source external clock to XTALIN (bypass mode). PLL enabled.

Table 26. Static characteristics: Power consumption in active mode

$T_{amb} = -20\text{ °C to }+70\text{ °C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^{[2][4][5]} | Max | Unit |
|--|------------------------|--|-----------|--------------------------|-----|------|
| DSP in Active mode, M33 in WF^[1] | | | | | | |
| I _{DDVDDCORE} | VDDCORE supply current | FFT code executed from SRAM partition 12; Internal LDO disabled CCLK = 12 MHz, VDDCORE = 0.7 V | [3][6][7] | - | 4.6 | - mA |
| | | CCLK = 48 MHz VDDCORE = 0.7 V | [3][6][7] | - | 11 | - mA |
| | | CCLK = 60 MHz VDDCORE = 0.7 V | [3][6][7] | - | 14 | - mA |
| | | CCLK = 80 MHz VDDCORE = 0.8 V | [6][7][8] | - | 20 | - mA |
| | | CCLK = 110 MHz VDDCORE = 0.8 V | [6][7][8] | - | 27 | - mA |
| | | CCLK = 144 MHz VDDCORE = 0.8 V | [6][7][8] | - | 34 | - mA |
| | | CCLK = 180 MHz VDDCORE = 0.8 V | [6][7][8] | - | 42 | - mA |

Table 26. Static characteristics: Power consumption in active mode ...continued

$T_{amb} = -20\text{ °C to }+70\text{ °C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^{[2][4][5]} | Max | Unit |
|--------|-----------|------------------------------------|-----------|--------------------------|-----|------|
| | | CCLK = 204 MHz VDDCORE = 0.8 V | [6][7][8] | - | 47 | - mA |
| | | CCLK = 240 MHz VDDCORE = 0.9 V | [6][7][8] | - | 63 | - mA |
| | | CCLK = 270 MHz VDDCORE = 0.9 V | [6][7][8] | - | 71 | - mA |
| | | CCLK = 300 MHz VDDCORE = 0.9 V | [6][7][8] | - | 78 | - mA |
| | | CCLK = 400 MHz VDDCORE = 1.0 V | [6][7][8] | - | 117 | - mA |
| | | CCLK = 600 MHz VDDCORE = 1.13 V | [6][7][8] | - | 207 | - mA |

- [1] Based on the power API library from the SDK software package available on nxp.com.
- [2] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2 = VDDA_ADC1V8 = 1.8 V. VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3 V
- [3] Clock source IRC. PLL disabled.
- [4] Characterized through bench measurements using typical samples.
- [5] Compiler settings: Keil Compiler for Arm ver 5.28, optimization level 3
- [6] The frequency for the specified VDDCORE voltage is the frequency of the main clock. This is before the CPU CLOCK Divider. Please see [Figure 6](#). The VDDCORE voltage has to be set according to the chosen main clock frequency.
- [7] 4.5 MB SRAM enabled. All peripheral clocks disabled (set to NONE). All Array Power enabled (PDRUNCFG 1/2 registers). Only SRAM partition 12 access enabled (SYSCTL0_AHB_SRAM_ACCESS_DISABLE register). SYSCPUAHBCLKDIV = 0x0.
- [8] Clock source external clock to XTALIN (bypass mode). PLL enabled.

Table 27. Static characteristics: Power consumption in sleep mode

$T_{amb} = -20\text{ °C to }+70\text{ °C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[2] | Max | Unit |
|---|----------------|----------------|--------------|--------------------|-----|------|
| Cortex-M33 in Sleep mode, DSP no clock | | | | | | |
| I _{DD} | supply current | CCLK = 12 MHz | [3][4][5][7] | - | 4 | - mA |
| | | CCLK = 48 MHz | [3][4][5][7] | - | 6 | - mA |
| | | CCLK = 250 MHz | [4][5][8] | - | 15 | - mA |

- [1] Based on the power API library from the SDK software package available on nxp.com.
- [2] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2 = VDDA_ADC1V8 = 1.8 V. VDDA_ADC3V3 = VREFP = USB1_VDD3V3 = 3.3 V
- [3] Clock source IRC. PLL disabled.
- [4] Characterized through bench measurements using typical samples.
- [5] Compiler settings: IAR C/C++ Compiler for Arm ver 8.32.3, optimization level 0, optimized for time off.
- [6] All peripheral clocks disabled.
- [7] Clock source IRC. PLL enabled.

Table 28. Static characteristics: Power consumption in deep-sleep mode $T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, unless otherwise specified,

| Symbol | Parameter | Conditions | Min | Typ ^{[1][2]} | Max ^[3] | Unit |
|--------------------------|----------------|--|-----|-----------------------|--------------------|------|
| I _{VDD1V8} | supply current | Deep-sleep mode; SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off | - | 174 | - | μA |
| I _{VDDCORE} | supply current | Deep-sleep mode; SRAM (32 KB) powered, Internal LDO disabled. Array On, Periphery Off $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 75 | - | μA |
| I _{VDDCORE} | supply current | Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 77 | - | μA |
| I _{VDDCORE} | supply current | Deep-sleep mode; SRAM (4.5 MB) powered, Internal LDO disabled. Array On, Periphery Off $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 190 | - | μA |
| I _{VDD_AO1V8} | supply current | Deep-sleep mode; SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off | - | 0.6 | - | μA |
| I _{VDDIO_0} | supply current | Deep-sleep mode; SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off | - | 7.0 | - | μA |
| I _{VDDIO_1} | supply current | Deep-sleep mode; SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off | - | 0.9 | - | μA |
| I _{VDDIO_2} | supply current | Deep-sleep mode; SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off | - | 6.4 | - | μA |
| I _{VDDA_1V8} | supply current | Deep-sleep mode; SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off | - | 0.1 | - | μA |
| I _{VDDA_BIAS} | supply current | Deep-sleep mode; SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off | - | 0.1 | - | μA |
| I _{VREFP} | supply current | Deep-sleep mode; SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off | - | 0.1 | - | μA |
| I _{USB1_VDD3V3} | supply current | Deep-sleep mode; SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off | - | 0.1 | - | μA |

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), All power supplies to = 1.8 V except USB1_VDD3V3 = 3.3 v

[2] Characterized through bench measurements using typical samples.

[3] Guaranteed by characterization, not tested in production.

Table 29. Static characteristics: Power consumption in deep power-down mode and full deep power-down modes $T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, unless otherwise specified,

| Symbol | Parameter | Conditions | Min | Typ ^{[1][2]} | Max ^[3] | Unit |
|------------------------|----------------|---|-----|-----------------------|--------------------|------|
| I _{VDD1V8} | supply current | Deep power-down mode; Internal LDO disabled. RTC Off | - | 16 | - | μA |
| I _{VDD_AO1V8} | supply current | Full Deep power-down mode; Internal LDO disabled. RTC Off $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 0.6 | - | μA |
| I _{VDDIO_0} | supply current | Deep power-down mode; Internal LDO disabled. RTC Off | - | 47 | - | μA |
| I _{VDDIO_1} | supply current | Deep power-down mode; Internal LDO disabled. RTC Off | - | 0.9 | - | μA |

Table 29. Static characteristics: Power consumption in deep power-down mode and full deep power-down modes
 $T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, unless otherwise specified,

| Symbol | Parameter | Conditions | Min | Typ ^{[1][2]} | Max ^[3] | Unit |
|--------------------------|----------------|---|-----|-----------------------|--------------------|------|
| I _{VDDIO_2} | supply current | Deep power-down mode; Internal LDO disabled. RTC Off | - | 47 | - | μA |
| I _{VDDA_1V8} | supply current | Deep power-down mode; Internal LDO disabled. RTC Off | - | 0.1 | - | μA |
| I _{VDDA_BIAS} | supply current | Deep power-down mode; Internal LDO disabled. RTC Off | - | 0.1 | - | μA |
| I _{VREFP} | supply current | Deep power-down mode; Internal LDO disabled. RTC Off | - | 0.1 | - | μA |
| I _{USB1_VDD3V3} | supply current | Deep power-down mode; Internal LDO disabled. RTC Off | - | 0.1 | - | μA |

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), All power supplies to = 1.8 V except USB1_VDD3V3 = 3.3 v

[2] Characterized through bench measurements using typical samples.

[3] Guaranteed by characterization, not tested in production.

13.5 Pin characteristics

Table 30. Static characteristics: pin characteristics

 $T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, unless otherwise specified. Values tested in production unless otherwise specified.

| Sym bol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--|--|--|-------------------------|--------------------|-------------------------|------|
| RESET pin, LDO_ENABLE pin, PMIC_IRQ_N pin, PMIC_MODE pins | | | | | | |
| V _{IH} | HIGH-level input voltage | | 0.7 x VDD_AO1V8 | - | VDD_AO1V8 | V |
| V _{IL} | LOW-level input voltage | | -0.3 | - | 0.3 x VDD_AO1V8 | V |
| V _{OH} | HIGH-level output voltage | I _{OH} = -2.9 mA; 1.71 V ≤ VDD_AO1V8 < 1.89 V | 0.8 x VDD_AO1V8 | - | - | V |
| V _{OL} | HIGH-level output voltage | I _{OL} = 2.9 mA; 1.71 V ≤ VDD_AO1V8 < 1.89 V | - | - | 0.2 x VDD_AO1V8 | V |
| V _{hys} | hysteresis voltage | | [4] - | 0.06 x VDD_AO1V8 | - | V |
| Standard I/O pins and PMIC I2C pins | | | | | | |
| Input characteristics | | | | | | |
| I _{IL} | LOW-level input current | V _I = 0 V; on-chip pull-up resistor disabled. 1.71 V ≤ V _{DDIO} < 1.98 V | -1.0 | | 1.0 | μA |
| | | V _I = 0 V; on-chip pull-up resistor disabled. 3.0 V ≤ V _{DDIO} < 3.6 V | -1.0 | | 1.0 | μA |
| I _{IH} | HIGH-level input current | V _I = V _{DDIO} ; on-chip pull-down resistor disabled. 1.71 V ≤ V _{DDIO} < 1.98 V | -1.0 | 0.5 | 1.0 | μA |
| | | V _I = V _{DDIO} ; on-chip pull-down resistor disabled. 3.0 V ≤ V _{DDIO} < 3.6 V | -1.0 | 0.5 | 1.0 | μA |
| V _I | input voltage | pin configured to provide a digital function except following pins V _{DDIO} = 0 V | [3] 0 | - | 3.6 | V |
| V _{IH} | HIGH-level input voltage | 1.71 V ≤ V _{DDIO} < 1.98 V | 0.7 × V _{DDIO} | - | V _{DDIO} | V |
| | | 3.0 V ≤ V _{DDIO} ≤ 3.6 V | 0.7 × V _{DDIO} | - | V _{DDIO} | V |
| V _{IL} | LOW-level input voltage | 1.71 V ≤ V _{DDIO} < 1.98 V | -0.3 | - | 0.3 × V _{DDIO} | V |
| | | 3.0 V ≤ V _{DDIO} ≤ 3.6 V | -0.3 | - | +0.7 | V |
| V _{hys} | hysteresis voltage | 1.71 V ≤ V _{DDIO} < 1.98 V | [4] 0.15 | - | - | V |
| | | 3.0 V ≤ V _{DDIO} ≤ 3.6 V | [4] 0.15 | - | - | V |
| Output characteristics | | | | | | |
| V _{OH} | HIGH-level output voltage (Normal Drive) | I _{OH} = -2.9 mA; 1.71 V ≤ V _{DDIO} < 1.98 V | 0.8 × V _{DDIO} | - | - | V |
| | | I _{OH} = -4 mA; 2.7 V ≤ V _{DDIO} ≤ 3.6 V | 0.8 × V _{DDIO} | - | - | V |
| V _{OH} | HIGH-level output voltage (Full Drive) | I _{OH} = -5.8 mA; 1.71 V ≤ V _{DDIO} < 1.98 V | 0.8 × V _{DDIO} | - | - | V |
| | | I _{OH} = -8 mA; 3.0 V ≤ V _{DDIO} ≤ 3.6 V | 0.8 × V _{DDIO} | - | - | V |

Table 30. Static characteristics: pin characteristics ...continued $T_{amb} = -20\text{ °C to }+70\text{ °C}$, unless otherwise specified. Values tested in production unless otherwise specified.

| Sym bol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--|---|--|-------------------|--------------------|-------------------------|------|
| V _{OL} | LOW-level output voltage (Normal Drive) | I _{OL} = 2.9 mA; 1.71 V ≤ V _{DDIO} < 1.98 V | - | - | 0.2 × V _{DDIO} | V |
| | | I _{OL} = 4 mA; 3.0 V ≤ V _{DDIO} ≤ 3.6 V | - | - | 0.2 × V _{DDIO} | V |
| V _{OL} | LOW-level output voltage (Full Drive) | I _{OL} = 5.8 mA; 1.71 V ≤ V _{DDIO} < 1.98 V | - | - | 0.2 × V _{DDIO} | V |
| | | I _{OL} = 8 mA; 3.0 V ≤ V _{DDIO} ≤ 3.6 V | - | - | 0.2 × V _{DDIO} | V |
| Weak input pull-up/pull-down characteristics | | | | | | |
| I _{pd} | pull-down current | V _I = V _{DDIO} | 34 | - | 180 | μA |
| | | V _I = 3.6 V | ^[2] 72 | - | 180 | μA |
| I _{pu} | pull-up current | V _I = 0 V | -34 | - | -180 | μA |
| R _{pd} | pull-down resistance | | 20 | - | 50 | kΩ |
| R _{pu} | pull-up resistance | | 20 | - | 50 | kΩ |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.

[2] Based on characterization. Not tested in production.

[3] All GPIO pins are fail safe up to 3.6 V when V_{DDIO} supply = 0 V except following pins (PIO1_19 to PIO1_31, PIO2_0 to PIO2_8, PIO0_21, PIO0_22, PIO_23 pins).

[4] Guaranteed by design, not tested in production.

14. Dynamic characteristics

14.1 Wake-up process

Table 31. Dynamic characteristic: Typical wake-up times from low power modes
 $T_{amb} = 25\text{ }^{\circ}\text{C}$; using IRC as the system clock.

| Symbol | Parameter | Conditions | | Min | Typ ^[1] | Max | Unit |
|------------|--------------|--|--------|-----|--------------------|-----|---------------|
| t_{wake} | wake-up time | from sleep mode, 250 MHz | [2][3] | - | 1.5 | - | μs |
| | | from sleep mode, 12 MHz | [2][3] | - | 6.2 | - | μs |
| t_{wake} | wake-up time | from deep-sleep mode | [2][3] | - | 637 | - | μs |
| t_{wake} | wake-up time | from deep power-down mode using RESETN. | [4] | - | 5.6 | - | ms |
| | | from deep power-down mode using PMIC_IRQ_N. | [4] | - | 7 | - | ms |
| t_{wake} | wake-up time | from full deep power-down mode using RESETN. | [4] | - | 5.6 | - | ms |
| | | from full deep power-down mode using PMIC_IRQ_N. | [4] | - | 7.6 | - | ms |

- [1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
- [2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.
- [3] IRC disabled, all peripherals off. PLL disabled.
- [4] Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the Wake-Up pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

14.2 IRC (48 MHz/60 MHz and 16 MHz)

The 48 MHz/60 MHz IRC is trimmed to $\pm 1\%$ accuracy over the entire voltage and temperature range. The 16 MHz IRC is trimmed to $\pm 3\%$ accuracy over the entire voltage and temperature range.

Table 32. Dynamic characteristic: IRC
 $T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$; 1.71 V to 3.6 V.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---------------|---------------------|------------|-------|--------------------|-------|------|
| $f_{osc(RC)}$ | IRC clock frequency | - | 15.52 | 16 | 16.48 | MHz |
| $f_{osc(RC)}$ | IRC clock frequency | - | 47.52 | 48 | 48.48 | MHz |
| $f_{osc(RC)}$ | IRC clock frequency | - | 59.4 | 60 | 60.6 | MHz |

- [1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Table 33. Dynamic characteristic: IRC $T_{amb} = -20\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}; 1.71\text{ V to }3.6\text{ V.}$

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|----------------------|---------------------|------------|-------|--------------------|-------|------|
| f _{osc(RC)} | IRC clock frequency | - | 15.52 | 16 | 16.48 | MHz |
| f _{osc(RC)} | IRC clock frequency | - | 47.52 | 48 | 48.72 | MHz |
| f _{osc(RC)} | IRC clock frequency | - | 59.4 | 60 | 60.90 | MHz |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

14.3 Internal Low Power Oscillator (1 MHz)

The IRC is trimmed to $\pm 10\%$ accuracy over the entire voltage and temperature range.

Table 34. Dynamic characteristic: LPCOSC $T_{amb} = -20\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}; 1.71\text{ V to }3.6\text{ V.}$

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|----------------------|-----------------------|------------|-----|--------------------|-----|------|
| f _{osc(RC)} | LPOSC clock frequency | - | 0.9 | 1 | 1.1 | MHz |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

14.4 Crystal oscillator

Table 35. Dynamic characteristic: oscillator $T_{amb} = -20\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}; 1.71\text{ V to }3.6\text{ V. [1][3]}$

| Symbol | Parameter | Conditions | Min | Typ ^[2] | Max | Unit |
|--------------------|---|------------|-----|--------------------|-----|------|
| f _{range} | oscillator frequency range | | 4 | - | 32 | MHz |
| R _F | feedback resistor - high gain mode only | | - | 1 | - | MΩ |
| ESR | Equivalent series resistance | - | - | - | 80 | Ω |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] See [Section 16.4](#)

[4] Select Low power mode = 1 in the CLKCTL0_SYSOSCCTL0 register.

[5] Select High Gain Mode = 0 in the CLKCTL0_SYSOSCCTL0 register.

14.5 RTC oscillator

Table 36. Dynamic characteristic: RTC oscillator $T_{amb} = -20\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}; 1.71\text{ V to }3.6\text{ V [1][2]}$

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|----------------|------------------------------|------------|-----|--------------------|-----|------|
| f _i | input frequency | - | - | 32.768 | - | kHz |
| ESR | Equivalent series resistance | - | - | 50 | 100 | kΩ |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] See [Section 16.3](#)

14.6 External Clock Input (CLKIN pin)

See [Section 16.3](#) for connecting the RTC oscillator to an external clock source.

Table 37. Dynamic characteristic: RTC oscillator

$T_{amb} = -20\text{ °C to }+70\text{ °C}; 1.71\text{ V to }3.6\text{ V}$. [\[1\]](#)

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--------|-----------------|------------|-----|--------------------|-----|------|
| f_i | input frequency | - | - | - | 50 | MHz |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

14.7 I²C-bus

Table 38. Dynamic characteristic: I²C-bus pins^[1]

$T_{amb} = 0\text{ °C to }+70\text{ °C}; 1.71\text{ V to }3.6\text{ V.}^{[2]}$

| Symbol | Parameter | | Conditions | Min | Max | Unit |
|---------------------|------------------------------|--------------|---|------|-----|------|
| f _{SCL} | SCL clock frequency | | Standard-mode | 0 | 100 | kHz |
| | | | Fast-mode | 0 | 400 | kHz |
| | | | Fast-mode Plus | 0 | 1 | MHz |
| t _f | fall time | [4][5][6][7] | Both SDA and SCL signals Standard-mode, 15 pF load | - | 6 | ns |
| | | | Fast-mode, 15 pF load | - | 6 | ns |
| | | | Fast-mode Plus, 15 pF load | - | 6 | ns |
| t _{LOW} | LOW period of the SCL clock | [11] | Standard-mode | 4.7 | - | μs |
| | | | Fast-mode | 1.3 | - | μs |
| | | | Fast-mode Plus | 0.5 | - | μs |
| t _{HIGH} | HIGH period of the SCL clock | [11] | Standard-mode | 4.0 | - | μs |
| | | | Fast-mode | 0.6 | - | μs |
| | | | Fast-mode Plus | 0.26 | - | μs |
| t _{HD;DAT} | data hold time | [3][4][8] | Standard-mode | 0 | - | μs |
| | | | Fast-mode | 0 | - | μs |
| | | | Fast-mode Plus | 0 | - | μs |
| t _{SU;DAT} | data set-up time | [9][10] | Standard-mode | 250 | - | ns |
| | | | Fast-mode | 100 | - | ns |
| | | | Fast-mode Plus | 50 | - | ns |

- [1] Guaranteed by design. Not tested in production.
- [2] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.
- [3] t_{HD;DAT} is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.
- [4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH(min)} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- [5] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.
- [6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
- [7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- [8] The maximum t_{HD;DAT} could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of t_{VD;DAT} or t_{VD;ACK} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
- [9] t_{SU;DAT} is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.
- [10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement t_{SU;DAT} = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
- [11] The MSTTIME register allows programming of certain times for the clock (SCL) high and low times. Please see RT600 user manual UM11147 for further details.

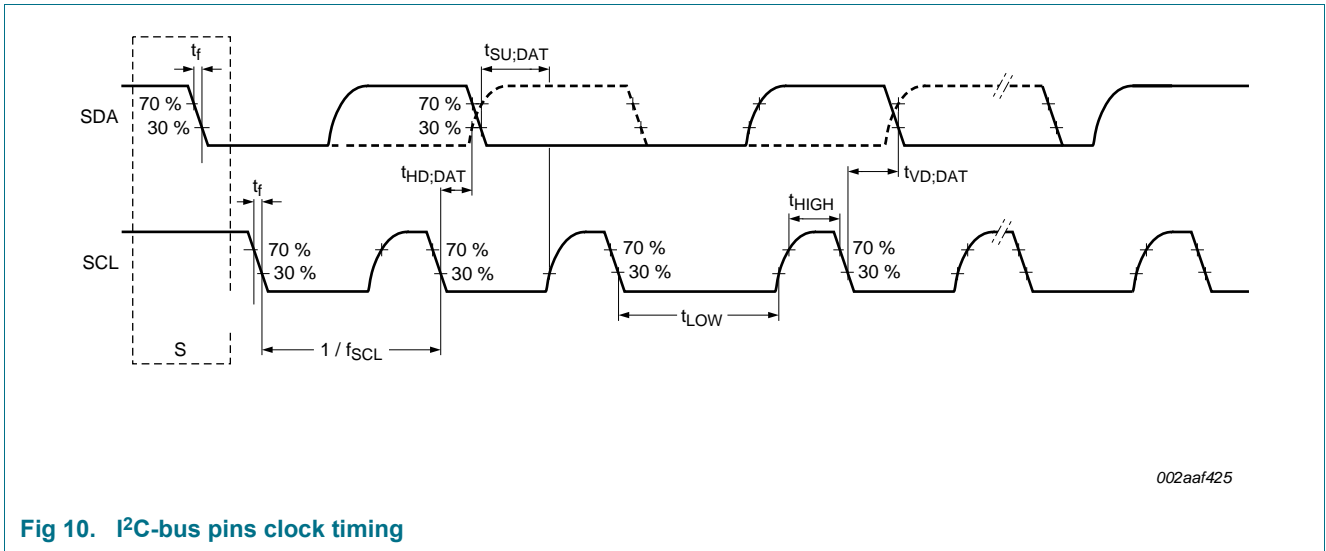


Fig 10. I²C-bus pins clock timing

14.8 I²S-bus interface**Table 39. Dynamic characteristics: I²S-bus interface pins [1][4]**

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $C_L = 10$, $VDDCORE = 1.13\text{ V}$ pF balanced loading on all pins; Input slew = 1.0 ns , Full Output Drive mode for all pins, SLEW setting = standard mode for all pins; Parameters sampled at the 50% level of the rising or falling edge.

| Symbol | Parameter | Conditions | Min | Typ ^[3] | Max | Unit |
|-----------------------------------|------------------------|-------------------------------------|-------------------|--------------------|-------------------|-------|
| Common to master and slave | | | | | | |
| t_{WH} | pulse width HIGH | on pins I2Sx_TX_SCK and I2Sx_RX_SCK | | | | |
| | | | $(T_{cyc}/2) - 1$ | - | $(T_{cyc}/2) + 1$ | ns |
| t_{WL} | pulse width LOW | on pins I2Sx_TX_SCK and I2Sx_RX_SCK | | | | |
| | | | $(T_{cyc}/2) - 1$ | - | $(T_{cyc}/2) + 1$ | ns |
| Master | | | | | | |
| $t_{v(Q)}$ | data output valid time | on pin I2Sx_TX_SDA | [2] | | | |
| | | | 0 | - | 20 | ns |
| | | on pin I2Sx_WS | | 0 | - | 20 |
| $t_{su(D)}$ | data input set-up time | on pin I2Sx_RX_SDA | [2] | 8 | - | ns |
| $t_{h(D)}$ | data input hold time | on pin I2Sx_RX_SDA | [2] | 0 | - | ns |
| Slave | | | | | | |
| $t_{v(Q)}$ | data output valid time | on pin I2Sx_TX_SDA | [2] | 0 | - | 20 ns |
| $t_{su(D)}$ | data input set-up time | on pin I2Sx_RX_SDA | [2] | | | |
| | | | 8 | - | - | ns |
| | | on pin I2Sx_WS | | 8 | - | - |
| $t_{h(D)}$ | data input hold time | on pin I2Sx_RX_SDA | [2] | | | |
| | | | 0 | - | - | ns |
| | | on pin I2Sx_WS | | 0 | - | - |

[1] Based on simulation; not tested in production.

[2] Clock Divider register (DIV) = 0x0.

[3] Typical ratings are not guaranteed.

[4] The Flexcomm Interface function clock frequency should not be above 48 MHz. See the data rates section in the I²S chapter (UM11147) to calculate clock and sample rates.

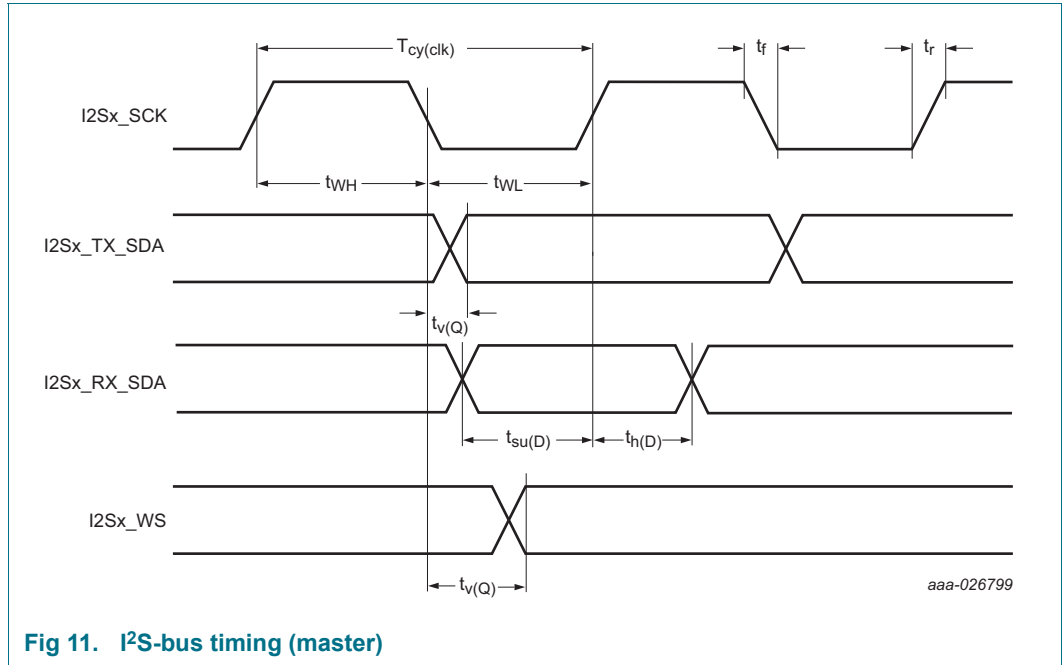


Fig 11. I²S-bus timing (master)

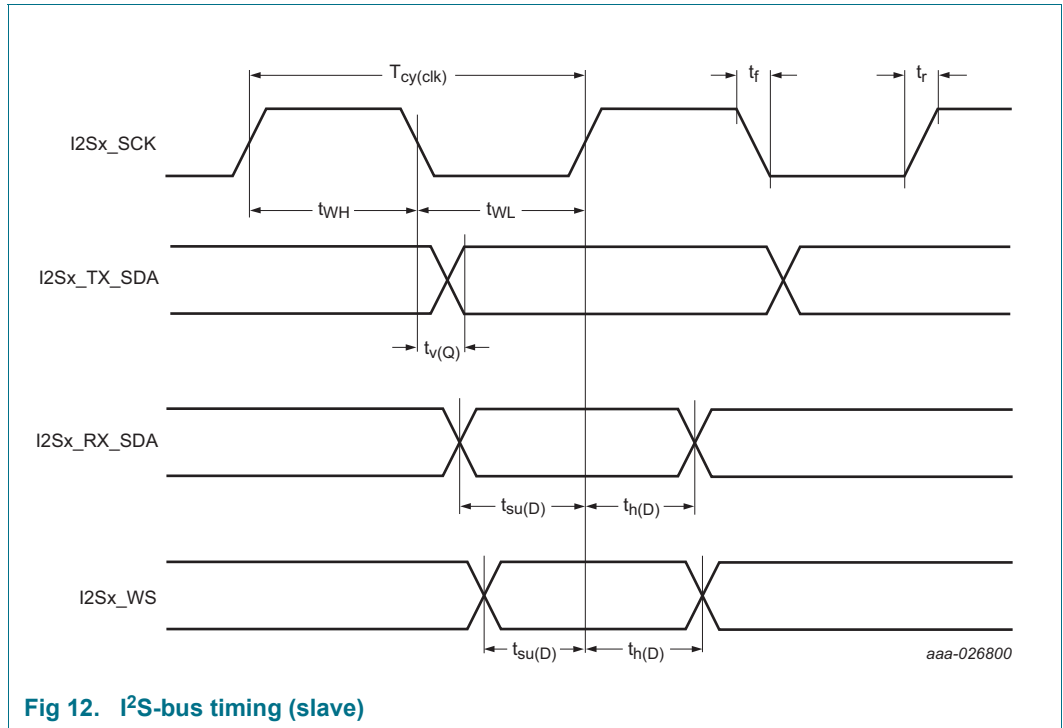


Fig 12. I²S-bus timing (slave)

14.9 USART interface

Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 20 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 20.0 Mbit/s.

Excluding delays introduced by external device and PCB, the maximum bit rates of 6.25 Mbit/s in asynchronous mode.

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading.

Table 40. USART dynamic characteristics^[1]

T_{amb} = 0 °C to 70 °C; VDDIO_x = 1.71 V to 1.89 V; C_L = 10, VDDCORE = 1.13 V pF balanced loading on all pins; Full Drive Mode on all pins, Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|------------------------|------------|------|-----|------|------|
| USART master (in synchronous mode) | | | | | | |
| t _{su(D)} | data input set-up time | | 12.0 | - | - | ns |
| t _{h(D)} | data input hold time | | 12.0 | - | - | ns |
| t _{v(Q)} | data output valid time | | -5.0 | - | 10.0 | ns |
| USART slave (in synchronous mode) | | | | | | |
| t _{su(D)} | data input set-up time | | 8.0 | - | - | ns |
| t _{h(D)} | data input hold time | | 0 | - | - | ns |
| t _{v(Q)} | data output valid time | | 0 | - | 20.0 | ns |

[1] Based on simulation; not tested in production.

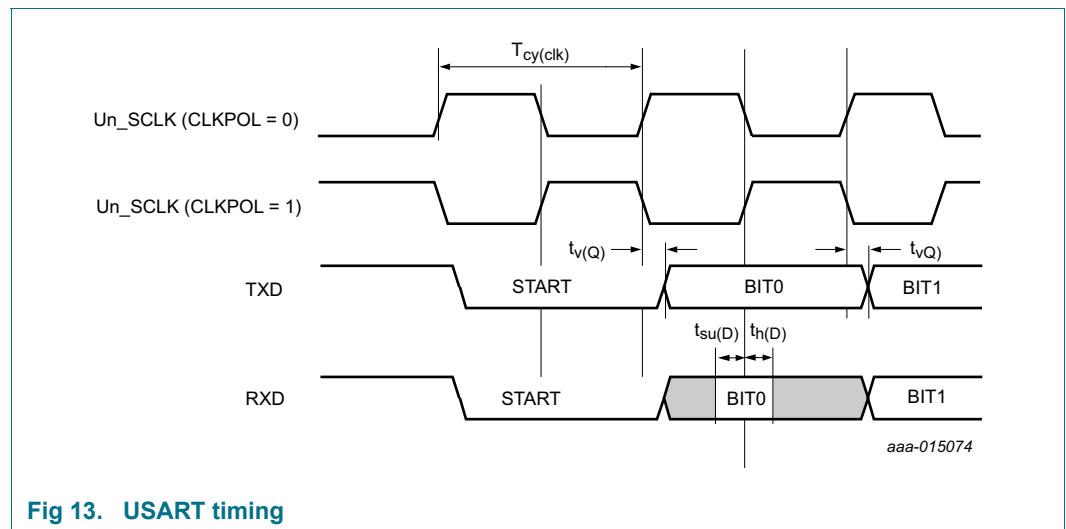


Fig 13. USART timing

14.10 SPI interfaces (Flexcomm Interfaces 0-7)

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading.

Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode (transmit/receive) is 25 Mbit/s and the maximum supported bit rate for SPI slave mode (transmit/receive) is 25 Mbit/s.

Table 41. SPI dynamic characteristics^[1]

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $C_L = 10\text{ pF}$ balanced loading on all pins; Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|------------------------|------------|-----|-----|-----|------|
| SPI master | | | | | | |
| t_{DS} | data set-up time | | 5 | - | - | ns |
| t_{DH} | data hold time | | 0 | - | - | ns |
| $t_{V(Q)}$ | data output valid time | | 0 | - | 13 | ns |
| SPI slave | | | | | | |
| t_{DS} | data set-up time | | 5 | - | - | ns |
| t_{DH} | data hold time | | 0 | - | - | ns |
| $t_{V(Q)}$ | data output valid time | | 0 | - | 13 | ns |

[1] Based on simulation; not tested in production.

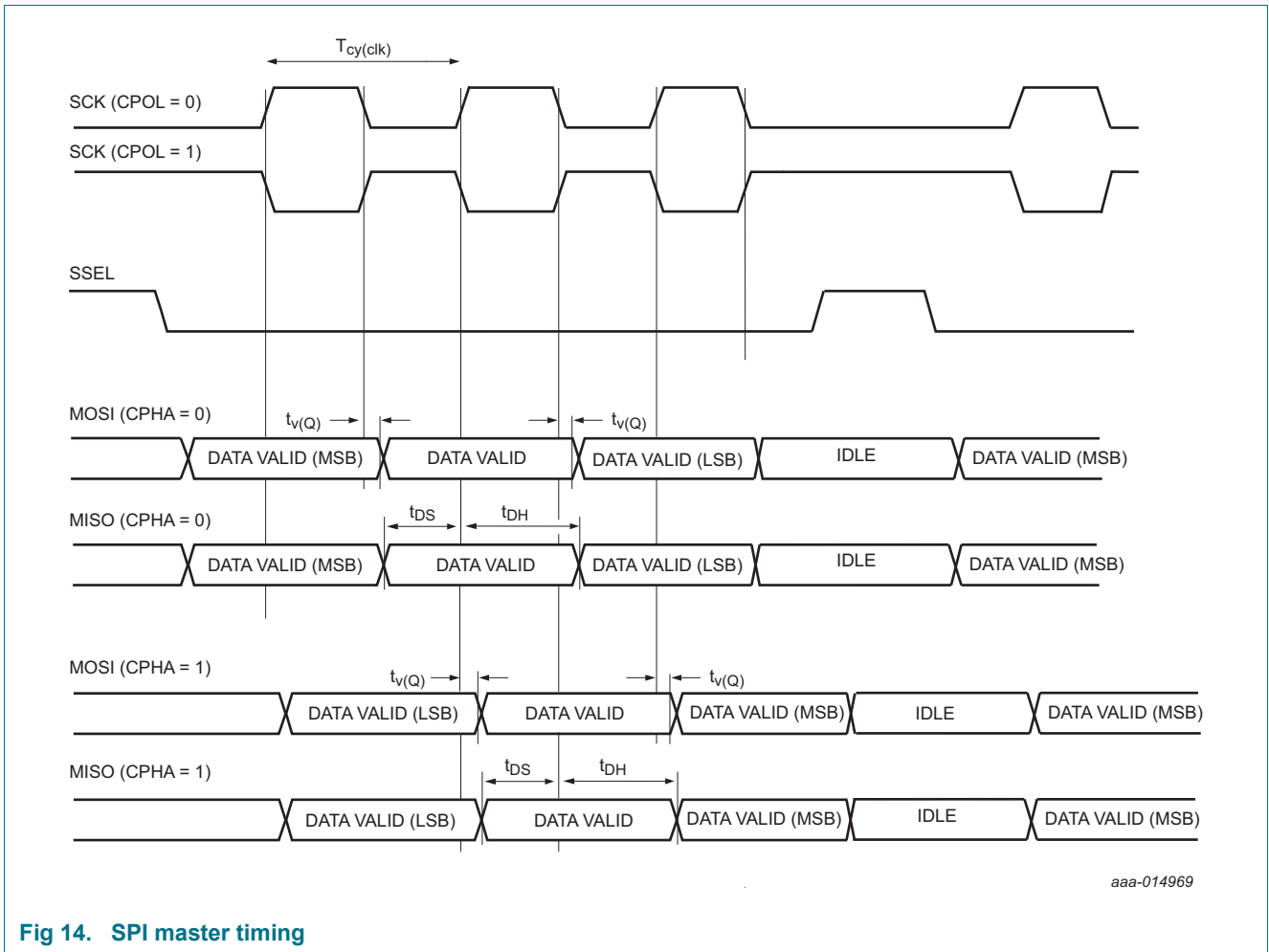


Fig 14. SPI master timing

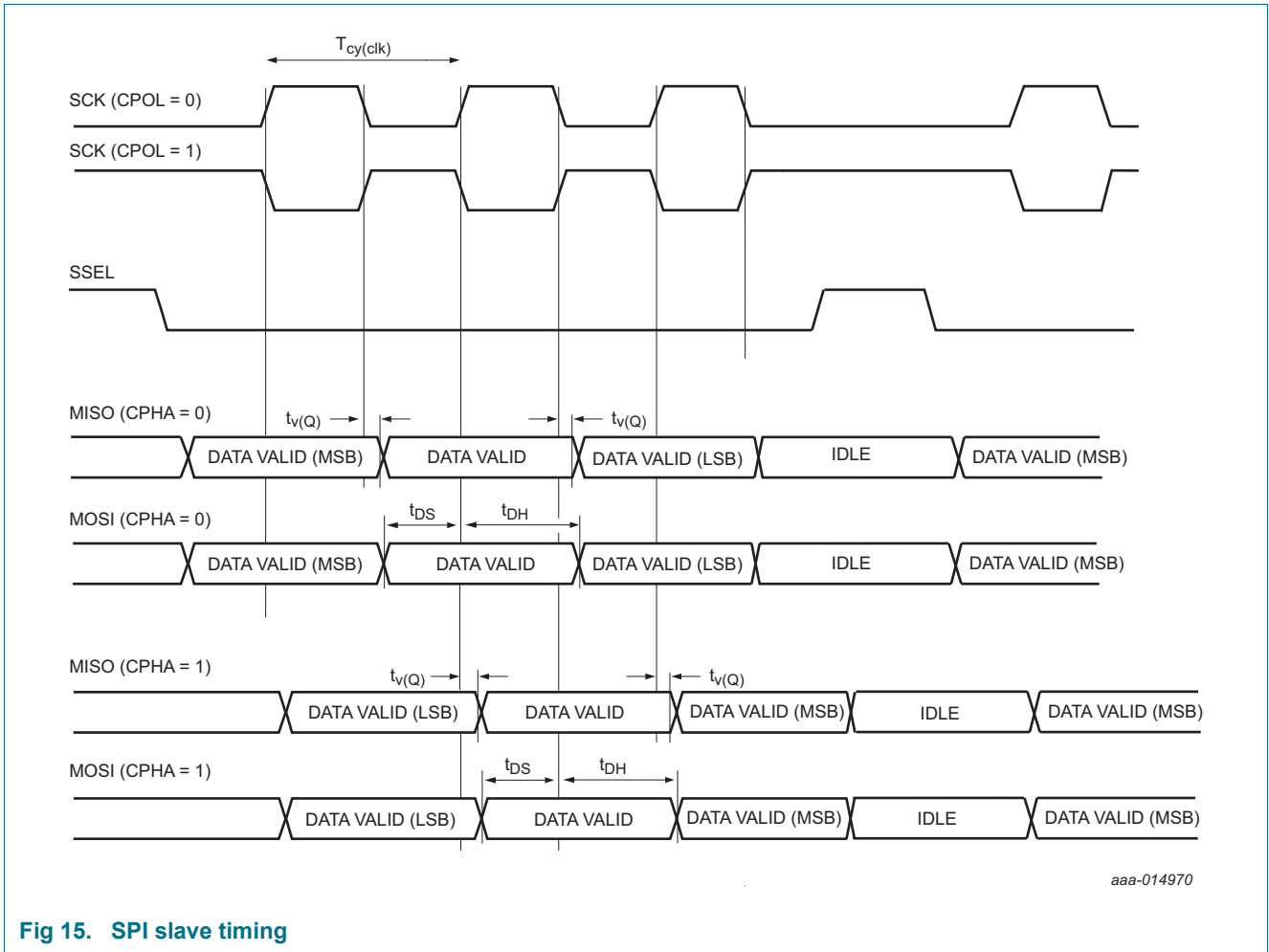


Fig 15. SPI slave timing

14.11 High Speed SPI Interface (Flexcomm Interface 14)

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode (transmit/receive) is 50 Mbit/s.

Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI slave mode (receive) is 50Mbit/s and for SPI slave mode (transmit) is 35 Mbit/s.

Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode (transmit/receive) is 25 Mbit/s and the maximum supported bit rate for SPI slave mode (transmit/receive) is 25 Mbit/s.

Table 42. High-Speed SPI dynamic characteristics^[1]

$T_{amb} = -0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; $VDDIO_X = 1.71\text{ V}$ to 1.89 V ; $C_L = 10\text{ pF}$ balanced loading on all pins; Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|------------------------|------------|-----|-----|-----|------|
| High-Speed SPI master | | | | | | |
| t_{DS} | data set-up time | | 4.0 | - | - | ns |
| t_{DH} | data hold time | | 0 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | | 0 | - | 6 | ns |
| High-Speed SPI slave | | | | | | |
| t_{DS} | data set-up time | | 3.0 | - | - | ns |
| t_{DH} | data hold time | | 0 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | | 0 | - | 10 | ns |

[1] Based on simulation; not tested in production.

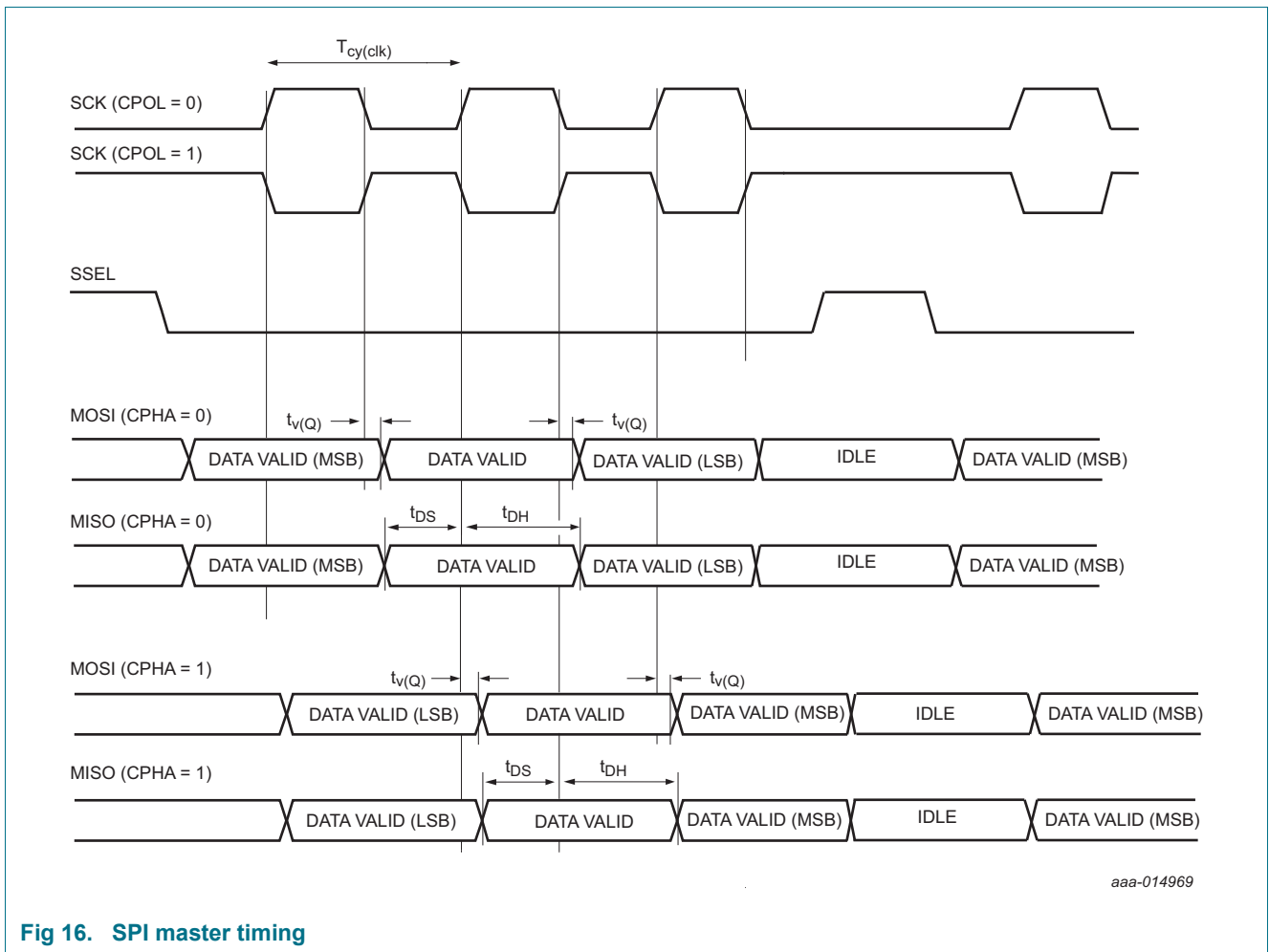


Fig 16. SPI master timing

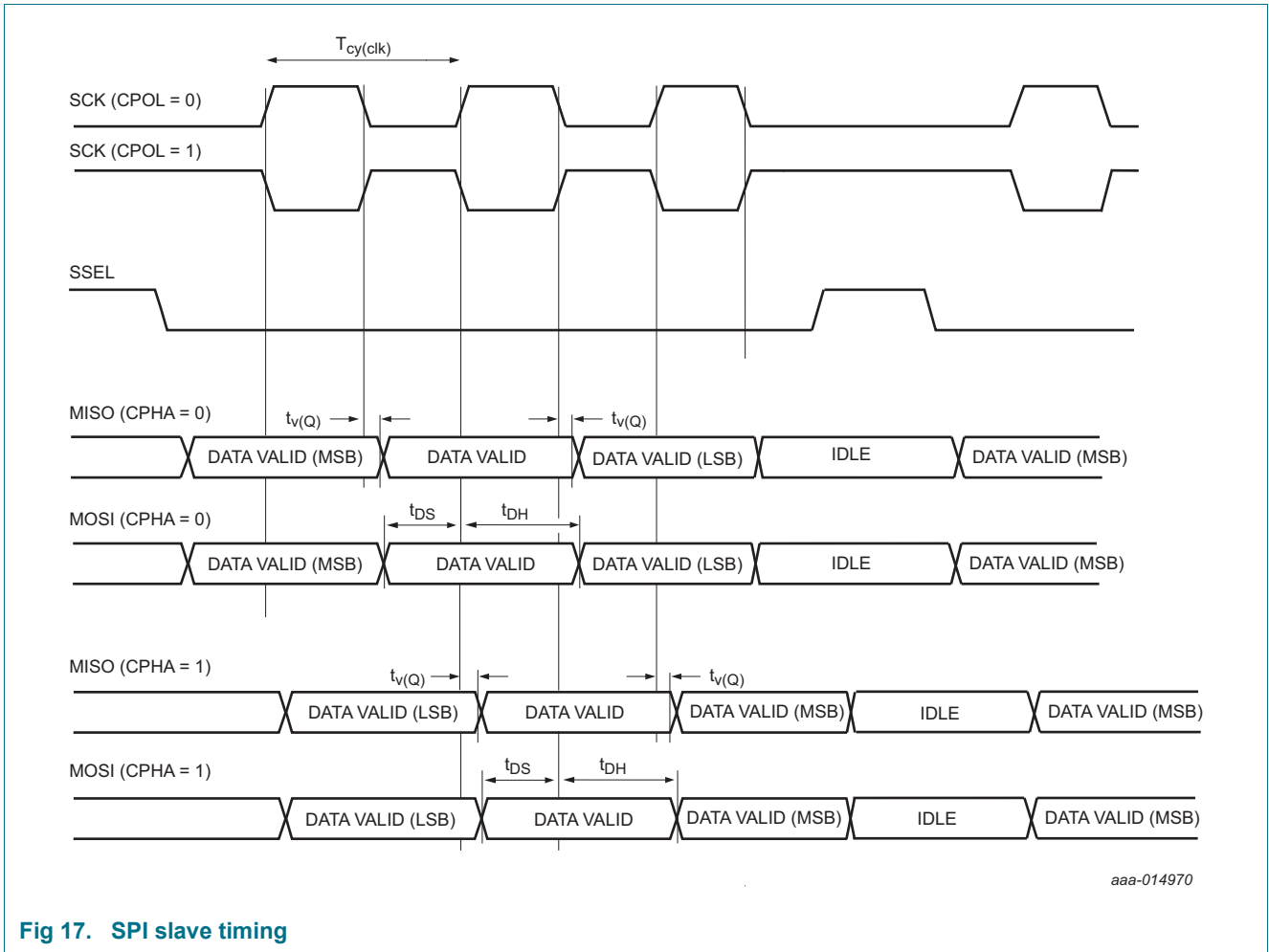


Fig 17. SPI slave timing

14.12 FlexSPI flash interface

Table 43. Dynamic characteristics: FlexSPI flash interface [1]

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $VDDCORE = 1.13\text{ V}$; $C_L = 10\text{ pF}$ balanced loading on all pins; Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|------------------------|--|-----|-----|--------------------|------|
| SDR Mode | | | | | | |
| f_{clk} | clock frequency | Transmit | - | - | 200 | MHz |
| | clock frequency | RX clock source = 0 | - | - | 60 | MHz |
| | clock frequency | RX clock source = 1 | - | - | 116 | MHz |
| | clock frequency | RX clock source = 3 | - | - | 200 | MHz |
| t_{DS} | data set-up time | RX clock source = 0 (internal dummy read strobe and loopbacked internally) | 6 | - | - | ns |
| | | RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad) | 1 | - | - | |
| | | source = 3 (external DQS, Flash provides read strobe) | 1 | - | - | |
| t_{DH} | data hold time | RX clock source = 0 (internal dummy read strobe and loopbacked internally) | 1 | - | - | ns |
| | | RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad) | 0 | - | - | |
| | | source = 3 (external DQS, Flash provides read strobe) | 0 | - | - | |
| $t_{V(Q)}$ | data output valid time | | 0 | - | 3 | ns |
| DDR Mode (with and without DQS) | | | | | | |
| f_{clk} | clock frequency | Transmit | - | - | 200 ^[2] | MHz |
| | clock frequency | RX clock source = 0 | - | - | 30 | MHz |
| | clock frequency | RX clock source = 1 | - | - | 58 ^[2] | MHz |
| | clock frequency | RX clock source = 3, with external DQS. | - | - | 200 | MHz |
| t_{DS} | data set-up time | RX clock source = 0 (internal dummy read strobe and loopbacked internally) | 6 | - | - | ns |
| | | RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad) | 1 | - | - | |
| | | source = 3 (external DQS, Flash provides read strobe) | 1 | - | - | |

Table 43. Dynamic characteristics: FlexSPI flash interface [1]

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $VDDCORE = 1.13\text{ V}$; $C_L = 10\text{ pF}$ balanced loading on all pins; Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|------------------------|--|-----|-----|-----|------|
| t_{DH} | data hold time | RX clock source = 0 (internal dummy read strobe and loopbacked internally) | 1 | - | - | ns |
| | | RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad) | 0 | | | |
| | | source = 3 (external DQS, Flash provides read strobe) | 0 | | | |
| $t_{v(Q)}$ | data output valid time | | 0 | - | 0.6 | ns |

[1] Based on simulation; not tested in production.

[2] DLLACR register [6:3] = 8, MISCCR2 register [1:0] = 2.

14.13 SD/MMC and SDIO

Table 44. Dynamic characteristics for following modes (SDR-12, SDR-25)

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $VDDCORE = 1.13\text{ V}$; $C_L = 10\text{ pF}$. $DLL_CTRL = 0x200$, Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|------------------------|---|-----|-----|-----|------|
| f_{clk} | clock frequency | on pin SD_CLK; data transfer mode, SDR-12 (12.5 MB/s) | - | - | 25 | MHz |
| f_{clk} | clock frequency | on pin SD_CLK; data transfer mode, SDR-25 (25 MB/s) | - | - | 50 | MHz |
| $t_{su(D)}$ | data input set-up time | on pins SD_DATn as inputs | 7.5 | - | - | ns |
| | | on pins SD_CMD as inputs | 7.5 | - | - | ns |
| $t_{h(D)}$ | data input hold time | on pins SD_DATn as inputs | 0 | - | - | ns |
| | | on pins SD_CMD as inputs | 0 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | on pins SD_DATn as outputs | 0 | - | 7.5 | ns |
| | | on pins SD_CMD as outputs | 0 | - | 7.5 | ns |

Table 45. Dynamic characteristics for following modes (SDR-50, SDR-104, SDR-200(HS-200))

$T_{amb} = -0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $VDDCORE = 1.13\text{ V}$; $C_L = 10\text{ pF}$. $DLL_CTRL = 0x200$, Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|------------------------|--|-----|-----|-----|------|
| f_{clk} | clock frequency | on pin SD_CLK; data transfer mode, SDR-50 (50 MB/s) | - | - | 100 | MHz |
| f_{clk} | clock frequency | on pin SD_CLK; data transfer mode, SDR-104 (104 MB/s) | - | - | 208 | MHz |
| f_{clk} | clock frequency | on pin SD_CLK; data transfer mode, SDR-200 (HS-200) (200 MB/s) | - | - | 200 | MHz |
| $t_{su(D)}$ | data input set-up time | on pins SD_DATn as inputs | 7.5 | - | - | ns |
| | | on pins SD_CMD as inputs | 7.5 | - | - | ns |
| $t_{h(D)}$ | data input hold time | on pins SD_DATn as inputs | 0 | - | - | ns |
| | | on pins SD_CMD as inputs | 0 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | on pins SD_DATn as outputs | 0 | - | 7.5 | ns |
| | | on pins SD_CMD as outputs | 0 | - | 7.5 | ns |

Table 46. Dynamic characteristics for following modes (DDR-50, DDR-100, HS DDR)

$T_{amb} = -0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $VDDCORE = 1.13\text{ V}$; $C_L = 10\text{ pF}$. $DLL_CTRL = 0x200$, Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production. HS-400 supported on SD port 0 only.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|-----------------|---|-----|-----|-----|------|
| f_{clk} | clock frequency | on pin SD_CLK; data transfer mode, DDR-50 (50 MB/s) | - | - | 50 | MHz |
| f_{clk} | clock frequency | on pin SD_CLK; data transfer mode, DDR-100 (100 MB/s) | - | - | 52 | MHz |
| f_{clk} | clock frequency | on pin SD_CLK; data transfer mode, HS DDR (104 MB/s) | - | - | 52 | MHz |

Table 46. Dynamic characteristics for following modes (DDR-50, DDR-100, HS DDR)

$T_{amb} = -0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $VDDCORE = 1.13\text{ V}$; $C_L = 10\text{ pF}$. $DLL_CTRL = 0x200$, Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production. HS-400 supported on SD port 0 only.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|------------------------|----------------------------|-----|-----|-----|------|
| $t_{su(D)}$ | data input set-up time | on pins SD_DATn as inputs | 4.8 | - | - | ns |
| | | on pins SD_CMD as inputs | 4.8 | - | - | ns |
| $t_{h(D)}$ | data input hold time | on pins SD_DATn as inputs | 0 | - | - | ns |
| | | on pins SD_CMD as inputs | 0 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | on pins SD_DATn as outputs | 0 | - | 5.0 | ns |
| | | on pins SD_CMD as outputs | 0 | - | 5.0 | ns |

Table 47. Dynamic characteristics for following modes (DDR-200 (HS-400))

$T_{amb} = -0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $VDDCORE = 1.13\text{ V}$; $C_L = 10\text{ pF}$. $DLL_CTRL = 0x200$, Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production. HS-400 supported on SD port 0 only.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|------------------------|--|-----|-----|-----|------|
| f_{clk} | clock frequency | on pin SD_CLK; data transfer mode, DDR-200 (HS-400) (400 MB/s) | - | - | 200 | MHz |
| $t_{su(D)}$ | data input set-up time | on pins SD_DATn as inputs | 0.5 | - | - | ns |
| | | on pins SD_CMD as inputs | 0.5 | - | - | ns |
| $t_{h(D)}$ | data input hold time | on pins SD_DATn as inputs | 0 | - | - | ns |
| | | on pins SD_CMD as inputs | 0 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | on pins SD_DATn as outputs | 0 | - | 1.0 | ns |
| | | on pins SD_CMD as outputs | 0 | - | 1.0 | ns |

14.14 DMIC subsystem

Table 48. Dynamic characteristics^[1]

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $VDDCORE = 1.13\text{ V}$; $C_L = 10\text{ pF}$ balanced loading on all pins; Input slew = 1 ns , SLEW set to standard mode for all pins; Bypass bit = 0 (PDM data in bypass mode); Parameters sampled at the 50% level of the rising or falling edge

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|------------------|------------|-----|-----|-----|------|
| t_{DS} | data set-up time | | 13 | - | - | ns |
| t_{DH} | data hold time | | 0 | - | - | ns |

[1] Based on simulated values.

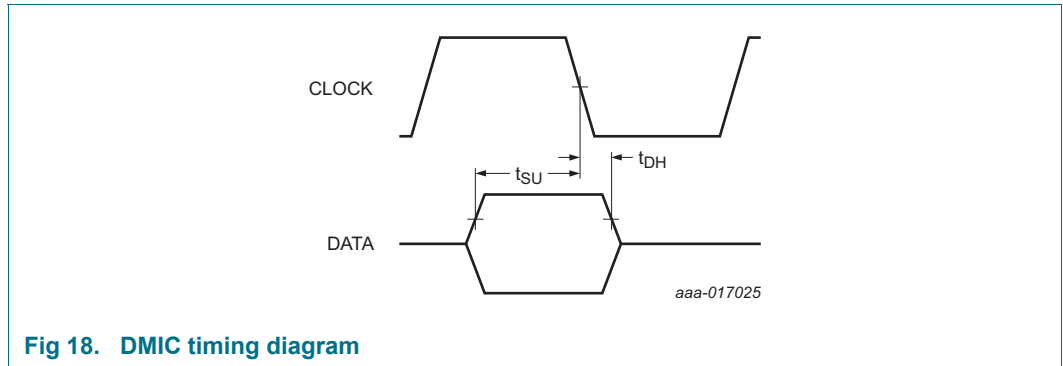


Fig 18. DMIC timing diagram

14.15 SCTimer/PWM output timing

Table 49. SCTimer/PWM output dynamic characteristics

$T_{amb} = -0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $VDDIO_x = 1.71\text{ V}$ to 1.89 V ; $VDDCORE = 1.13\text{ V}$; $C_L = 10\text{ pF}$. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 50% level of the rising or falling edge; values guaranteed by design.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|------------------|------------|-----|-----|-----|------|
| $t_{sk(o)}$ | output skew time | - | 0 | - | 2.8 | ns |

15. Analog characteristics

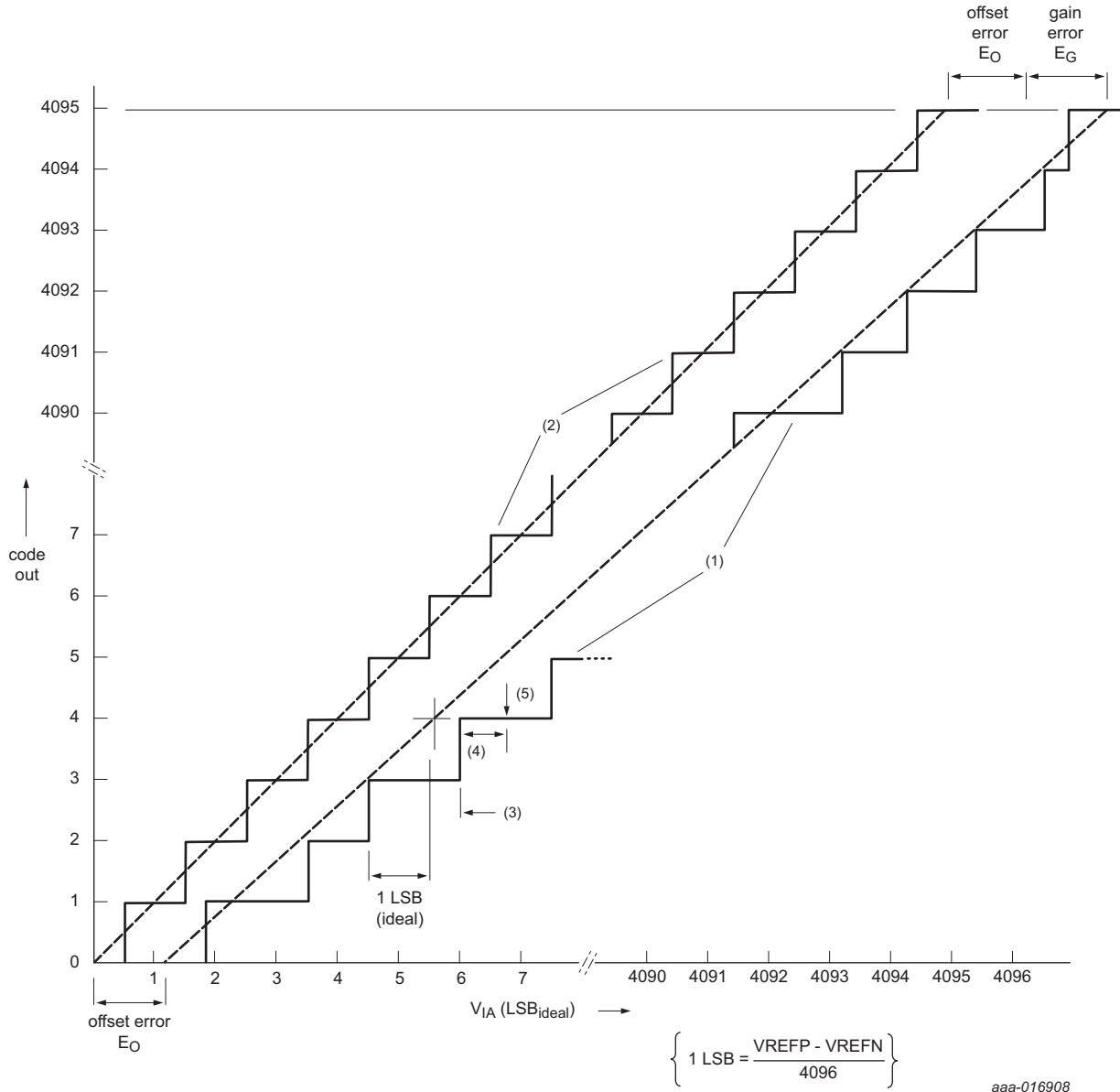
15.1 12-bit ADC characteristics

Table 50. 12-bit ADC static characteristics

$T_{amb} = -20\text{ °C to }+70\text{ °C}$; $VDD_{AO1V8} = 1.8\text{ V}$, $VDD1V8 = 1.8\text{ V}$, $VDDIO_0/1/2 = 1.8\text{ V}$, $VDDA_1V8 = VDDA_{BIAS} = VREFP = 1.8\text{ V}$; $V_{SSA} = VREFN = GND$. $f_{clk(ADC)} = 22\text{ MHz}$; Sample Time select (STS bit in CMDH register) = 0.

| Symbol | Parameter | Conditions | Min | Typ ^[2] | Max | Unit | |
|------------------|------------------------------|------------|--|--------------------|-------|------------|---|
| VADIN | analog input voltage | | See Figure 20 | VREFN | - | VREFP | V |
| $f_{clk(ADC)}$ | ADC clock frequency | | - | - | 60 | MHz | |
| f_s | sampling frequency | | - | - | 1.0 | Msamples/s | |
| $C_{samples}$ | Sample cycles | | 3.5 | - | 131.5 | | |
| $C_{compare}$ | Fixed compare cycles | | - | 17.5 | - | cycles | |
| $C_{conversion}$ | Conversion cycles | | $C_{conversion} = C_{samples} + C_{compare}$ | | | cycles | |
| CADIN | Analog Input Capacitance | | See Figure 20 . ^[3] | 4.5 | - | pF | |
| RADIN | Input Resistance | | See Figure 20 . | 500 | - | Ω | |
| RAS | Analog source resistance | | See Figure 20 . ^[8] | - | 5 | k Ω | |
| E_D | differential linearity error | | [1][4] | $< \pm 1$ | - | LSB | |
| $E_{L(adj)}$ | integral non-linearity | | [1][5] | $< \pm 1.1$ | - | LSB | |
| E_O | offset error | | [1][6] | $< \pm 1$ | - | LSB | |
| $V_{err(FS)}$ | full-scale error voltage | | [1][7] | ± 0.3 | - | % | |

- [1] Based on characterization; not tested in production.
- [2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
- [3] CADIN represents the external capacitance on the analog input channel for sampling speeds of 1.0 Msamples/s. No parasitic capacitances included. See [Figure 20](#)
- [4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See [Figure 19](#).
- [5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 19](#).
- [6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 19](#).
- [7] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 19](#).
- [8] This resistance is external to the MCU. To achieve the best results, the analog source resistance must be kept as low possible. The results in this data sheet were derived from a system that had $< 15\ \Omega$ analog source resistance. See [Figure 20](#).



- (1) Example of an actual transfer curve.
- (2) The ideal transfer curve.
- (3) Differential linearity error (E_D).
- (4) Integral non-linearity ($E_{L(adj)}$).
- (5) Center of a step of the actual transfer curve.

Fig 19. 12-bit ADC characteristics

15.1.1 ADC input impedance

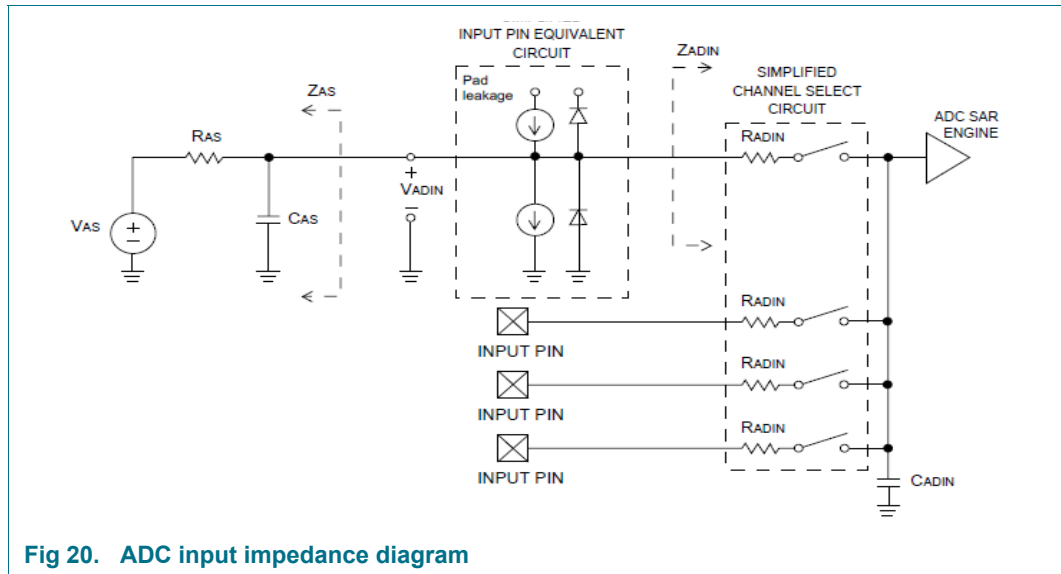


Fig 20. ADC input impedance diagram

15.2 Temperature sensor

Table 51. Temperature sensor static and dynamic characteristics

$V_{DDA_BIAS} = 3.3\text{ V}$, All other supplies = 1.8 V

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|-----------------------------|--|-----|-----|------|------|
| DT_{sen} | sensor temperature accuracy | $T_{amb} = -20\text{ °C to }+70\text{ °C}$ | [1] | - | 2.77 | °C |
| E_L | linearity error | $T_{amb} = -20\text{ °C to }+70\text{ °C}$ | - | - | 2.79 | °C |

[1] Absolute temperature accuracy.

Table 52. Temperature sensor Linear-Least-Square (LLS) fit parameters*VDDA_BIAS = 3.3 V, All other supplies = 1.8 V*

| Fit parameter | Range | | Min | Typ | Max | Unit |
|-----------------------|--|-----|-----|------|-----|-------|
| LLS slope | $T_{\text{amb}} = -20\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$ | [1] | - | -1.5 | - | mV/°C |
| LLS intercept at 0 °C | $T_{\text{amb}} = -20\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$ | [1] | - | 802 | - | mV |

[1] Measured over typical samples.

15.2.1 Comparator

Table 53. Comparator characteristics

 $T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ unless noted otherwise; All supplies = 1.8 V.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--------------------------------|-------------------------------------|--|-----|--------------------|-----|------|
| Static characteristics | | | | | | |
| V_{offset} | offset voltage | $V_{IC} = 0.1\text{ V}$ | - | 6 | - | mV |
| | | $V_{IC} = 0.9\text{ V}$ | - | 7 | - | mV |
| | | $V_{IC} = 1.7\text{ V}$ | - | 9 | - | mV |
| Dynamic characteristics | | | | | | |
| t_{PD} | propagation delay (Low speed mode) | HIGH to LOW; $T_{amb} = 25\text{ }^{\circ}\text{C}$ $V_{IC} = 0.1\text{ V}$; 100 mV overdrive input | - | 2 | - | us |
| | | $V_{IC} = 0.1\text{ V}$; rail-to-rail input | - | 915 | - | ns |
| | | $V_{IC} = 0.9\text{ V}$; 100 mV overdrive input | - | 525 | - | ns |
| | | $V_{IC} = 0.9\text{ V}$; rail-to-rail input | - | 600 | - | ns |
| | | $V_{IC} = 1.7\text{ V}$; 100 mV overdrive input | - | 500 | - | ns |
| | | $V_{IC} = 1.7\text{ V}$; rail-to-rail input | - | 350 | - | ns |
| t_{PD} | propagation delay (High speed mode) | HIGH to LOW; $T_{amb} = 25\text{ }^{\circ}\text{C}$ $V_{IC} = 0.1\text{ V}$; 100 mV overdrive input ^[3] | - | 270 | - | ns |
| | | $V_{IC} = 0.1\text{ V}$; rail-to-rail input | - | 310 | - | ns |
| | | $V_{IC} = 0.9\text{ V}$; 100 mV overdrive input ^[3] | - | 340 | - | ns |
| | | $V_{IC} = 0.9\text{ V}$; rail-to-rail input | - | 210 | - | ns |
| | | $V_{IC} = 1.7\text{ V}$; 100 mV overdrive input ^[3] | - | 150 | - | ns |
| | | $V_{IC} = 1.7\text{ V}$; rail-to-rail input | - | 125 | - | ns |
| t_{PD} | propagation delay (Low speed mode) | LOW to HIGH; $T_{amb} = 25\text{ }^{\circ}\text{C}$ $V_{IC} = 0.1\text{ V}$; 100 mV overdrive input ^[3] | - | 5.8 | - | us |
| | | $V_{IC} = 0.1\text{ V}$; rail-to-rail input | - | 470 | - | ns |
| | | $V_{IC} = 0.9\text{ V}$; 100 mV overdrive input ^[3] | - | 750 | - | ns |
| | | $V_{IC} = 0.9\text{ V}$; rail-to-rail input | - | 600 | - | ns |
| | | $V_{IC} = 1.7\text{ V}$; 100 mV overdrive input ^[3] | - | 5.5 | - | us |
| | | $V_{IC} = 1.7\text{ V}$; rail-to-rail input | - | 1.25 | - | us |
| t_{PD} | propagation delay (High speed mode) | LOW to HIGH; $T_{amb} = 25\text{ }^{\circ}\text{C}$ $V_{IC} = 0.1\text{ V}$; 100 mV overdrive input ^[3] | - | 105 | - | ns |
| | | $V_{IC} = 0.1\text{ V}$; rail-to-rail input | - | 115 | - | ns |
| | | $V_{IC} = 0.9\text{ V}$; 100 mV overdrive input ^[3] | - | 110 | - | ns |
| | | $V_{IC} = 0.9\text{ V}$; rail-to-rail input | - | 120 | - | ns |
| | | $V_{IC} = 1.7\text{ V}$; 100 mV overdrive input ^[3] | - | 110 | - | ns |
| | | $V_{IC} = 1.7\text{ V}$; rail-to-rail input | - | 120 | - | ns |
| V_{hys} | hysteresis voltage ^[2] | HYSTCR1[1:0] = 01 | - | 13 | - | mV |
| | | HYSTCR1[1:0] = 10 | - | 27 | - | mV |
| | | HYSTCR1[1:0] = 11 | - | 35 | - | mV |

[1] Characterized on typical samples, not tested in production.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

[3] 100 mV overdrive corresponds to a square wave from 50 mV below the reference (V_{IC}) to 50 mV above the reference.

16. Application information

16.1 Standard I/O pin configuration

Figure 21 shows the possible pin modes for standard I/O pins:

The default configuration for standard I/O pins is Z mode. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

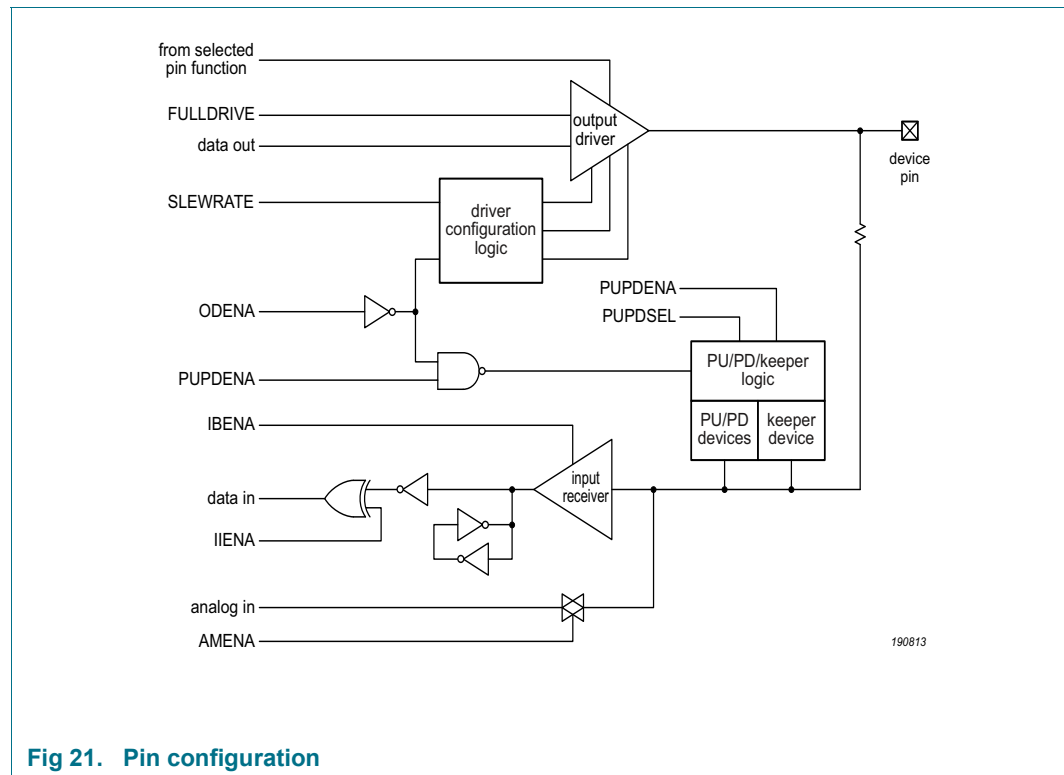


Fig 21. Pin configuration

16.2 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 30 for a given input voltage V_I . For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 30, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 30 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

16.3 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on RTCXIN and RTCXOUT. See [Figure 22](#).

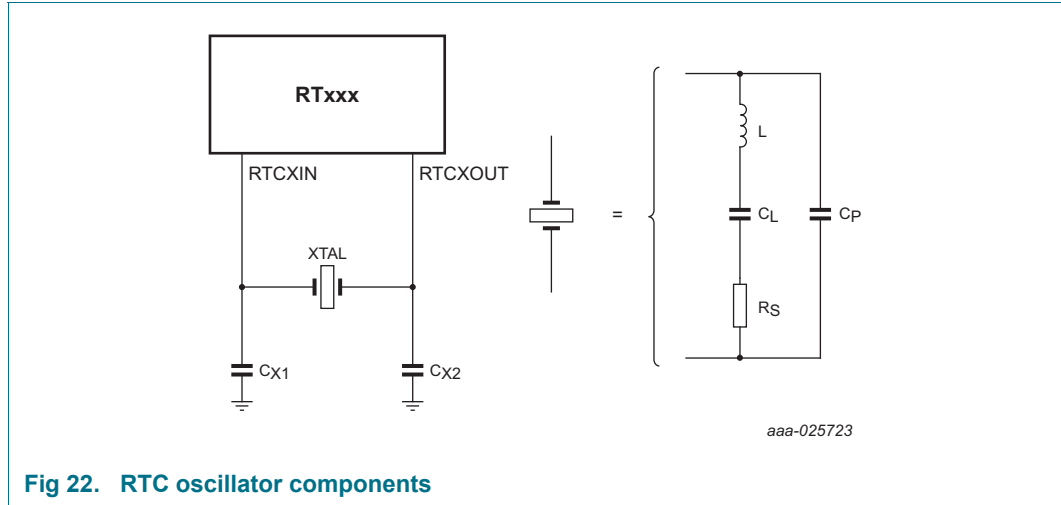


Fig 22. RTC oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (C_L), series resistance (R_S), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the RTCXIN and RTCXOUT pins (~3 pF).

$C_{Parasitic}$ - Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to the CLOCKOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

To use bypass mode on RTC, remove the crystal, drive an external clock to RTCIN pin, and float the RTCOUT pin.

16.3.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

16.4 XTAL oscillator

In the XTAL oscillator circuit, only the crystal (XTAL) and the capacitances C_x and C_y need to be connected externally on XTALIN and XTALOUT. See [Figure 23](#).

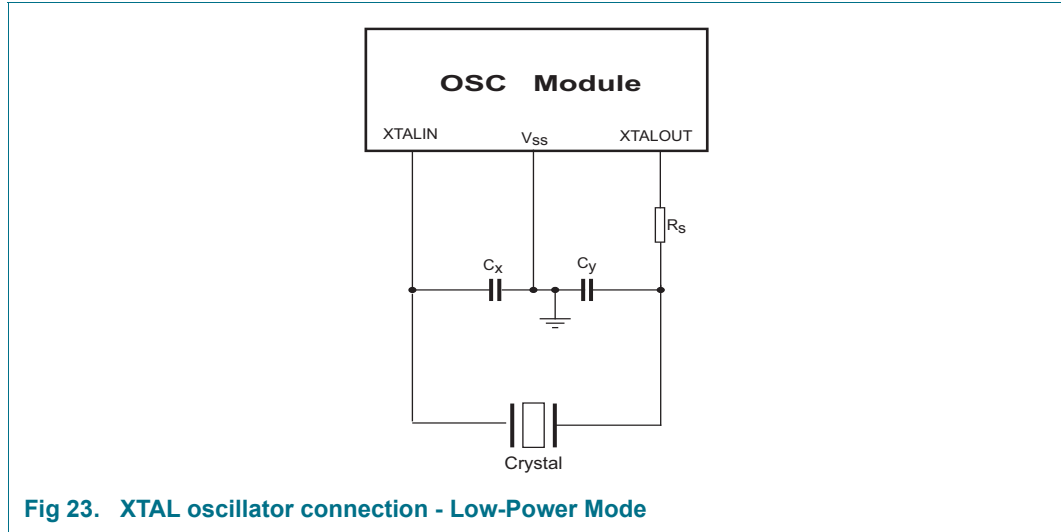


Fig 23. XTAL oscillator connection - Low-Power Mode

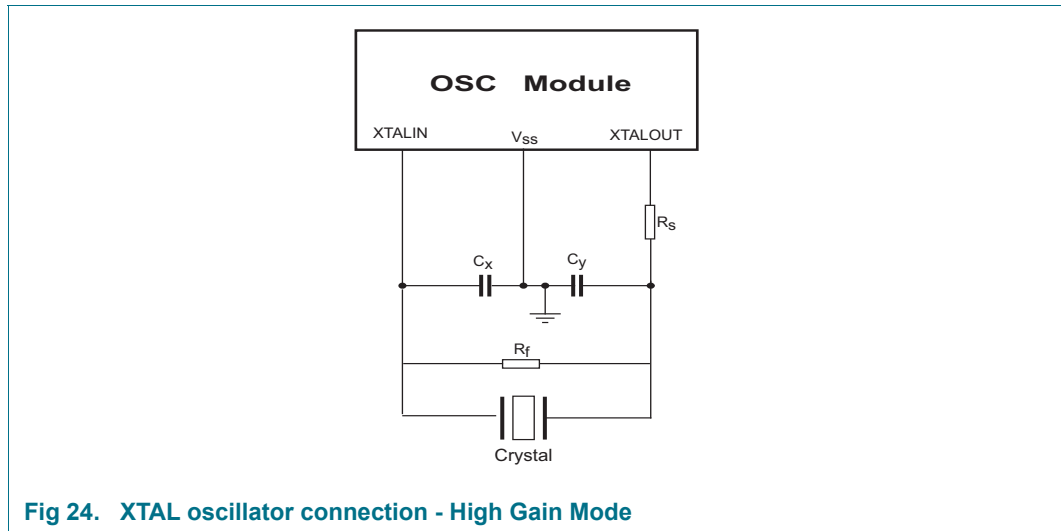


Fig 24. XTAL oscillator connection - High Gain Mode

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (C_L), series resistance (R_S), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_x and C_y values can also be generally determined by the following expression:

$$C_x = C_y = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF).

$C_{Parasitic}$ - Parasitic or stray capacitance of external circuit.

Although $C_{\text{Parasitic}}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the XTALOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

To use bypass mode on system oscillator, set bit 1 to '1' in the system oscillator control 0 (CLKCTL0_SYSOSCCTL0), float the XTALIN pin, and drive XTALOUT with < 0.7 V to 1.8V.

For oscillator high gain mode, a larger voltage swing is used at the crystal pin. This gives a higher noise immunity within the oscillator and less edge to edge jitter of the internal clock. When high gain mode is not required, power used by the crystal oscillator can be reduced by using low power mode.

Remark: High gain mode requires a 1 megohm resistor (R_F) to be inserted.

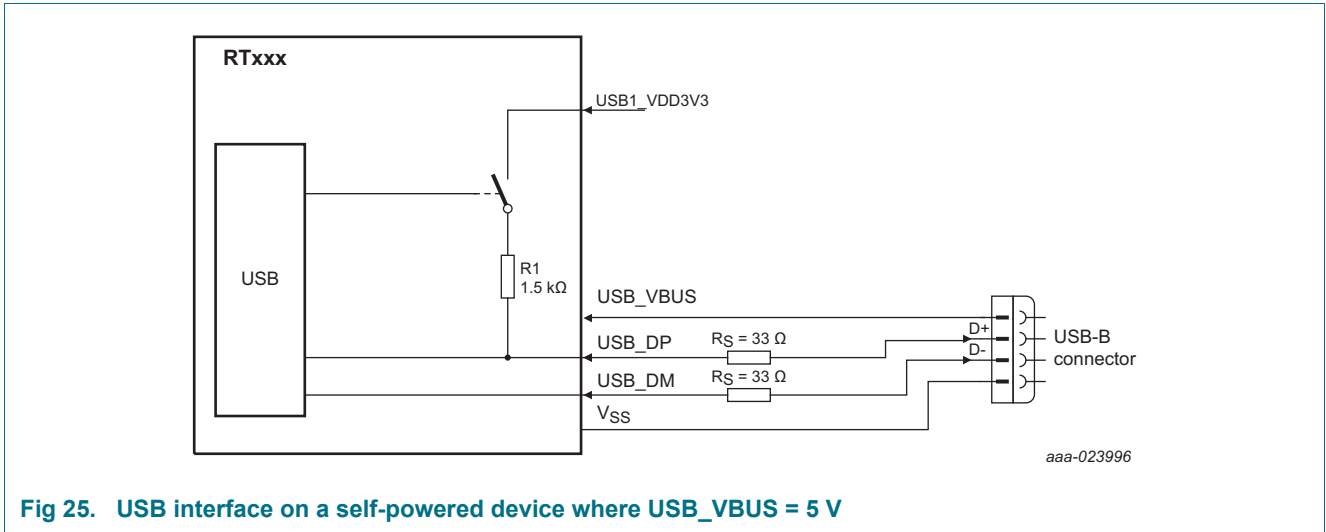
16.4.1 XTAL Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors C_x , C_y , and C_{X3} , in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

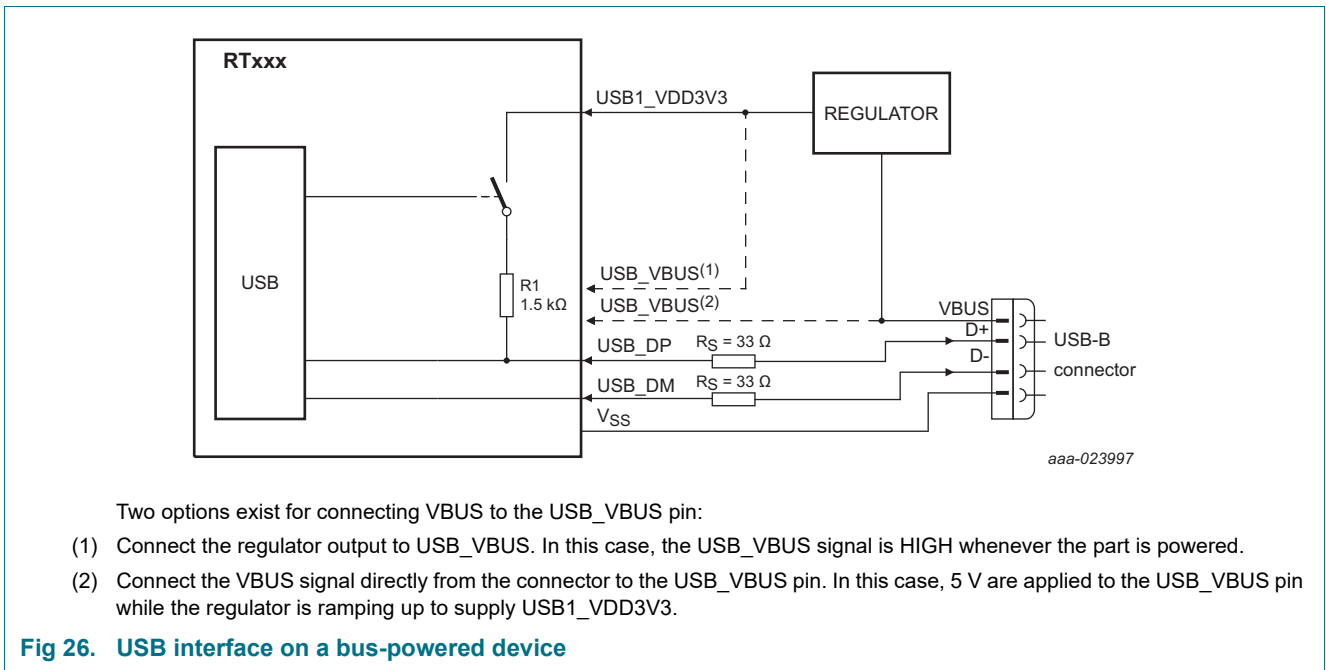
16.5 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see [Figure 25](#)) or bus-powered device (see [Figure 26](#)).

On the RT600, the USB_VBUS pin is 5 V tolerant pin regardless of whether USB1_VDD3V3 or VDD pins are present or not.



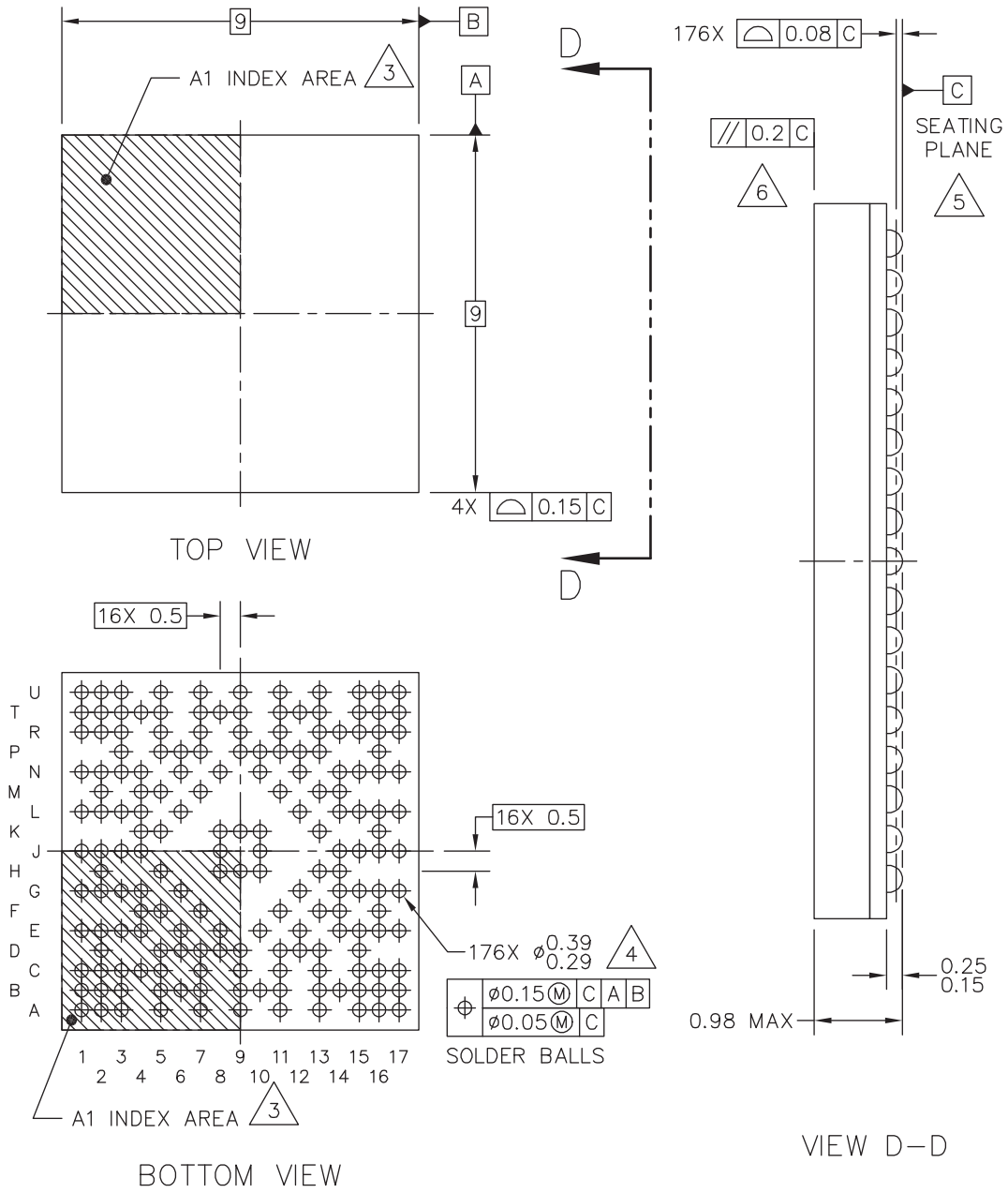
The internal pull-up (1.5 kΩ) can be enabled by setting the DCON bit in the DEVCMSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required.



Two options exist for connecting VBUS to the USB_VBUS pin:

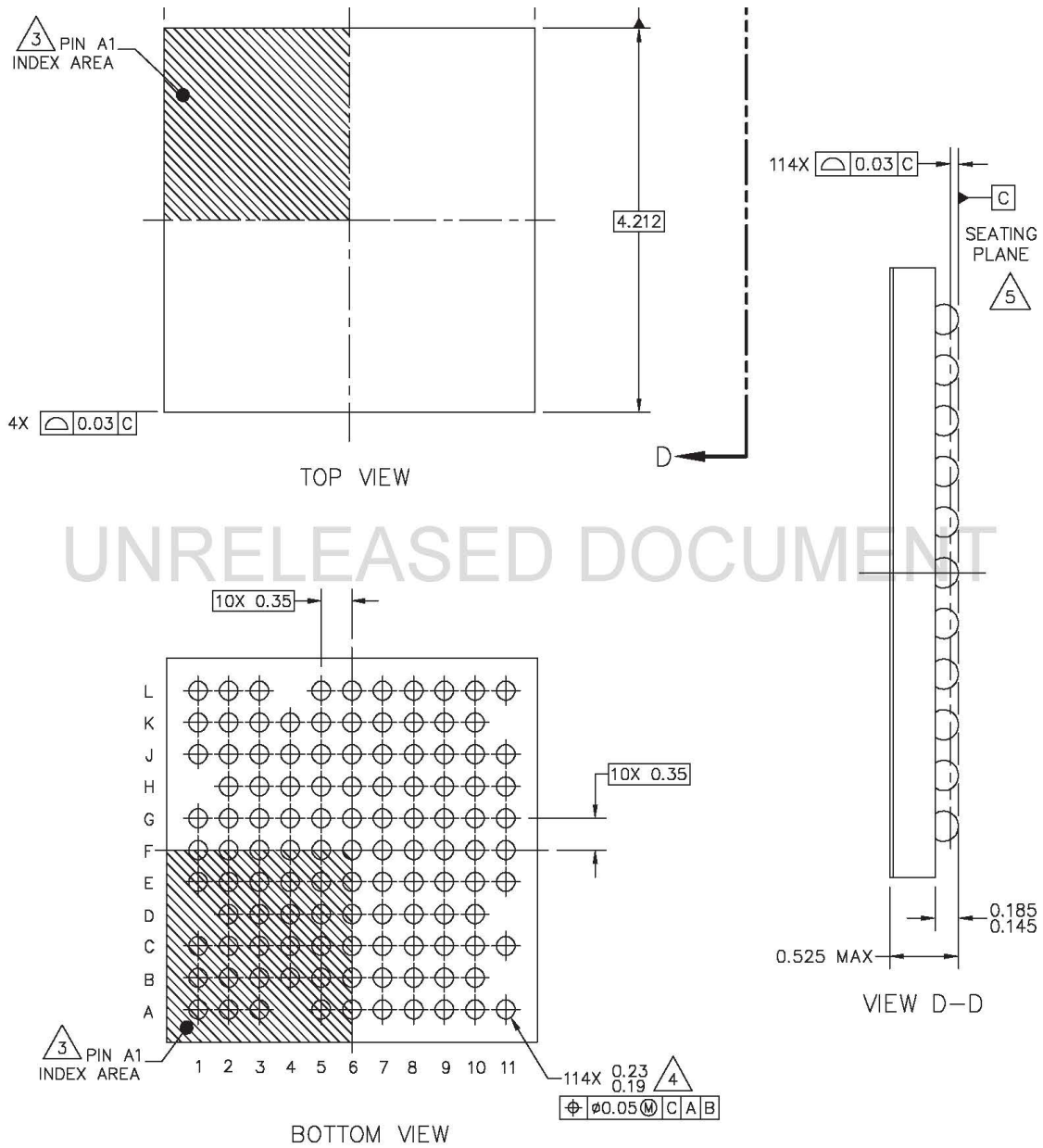
- (1) Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.
- (2) Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to supply USB1_VDD3V3.

17. Package outline



| | | | |
|--|------------------------|--------------------------------|----------------|
| © NXP B.V. ALL RIGHTS RESERVED | | DATE: 13 JUL 2018 | |
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA00942D | REVISION: A |
| | | | PAGE: |

Fig 27. VFBGA176 package



UNRELEASED DOCUMENT

RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

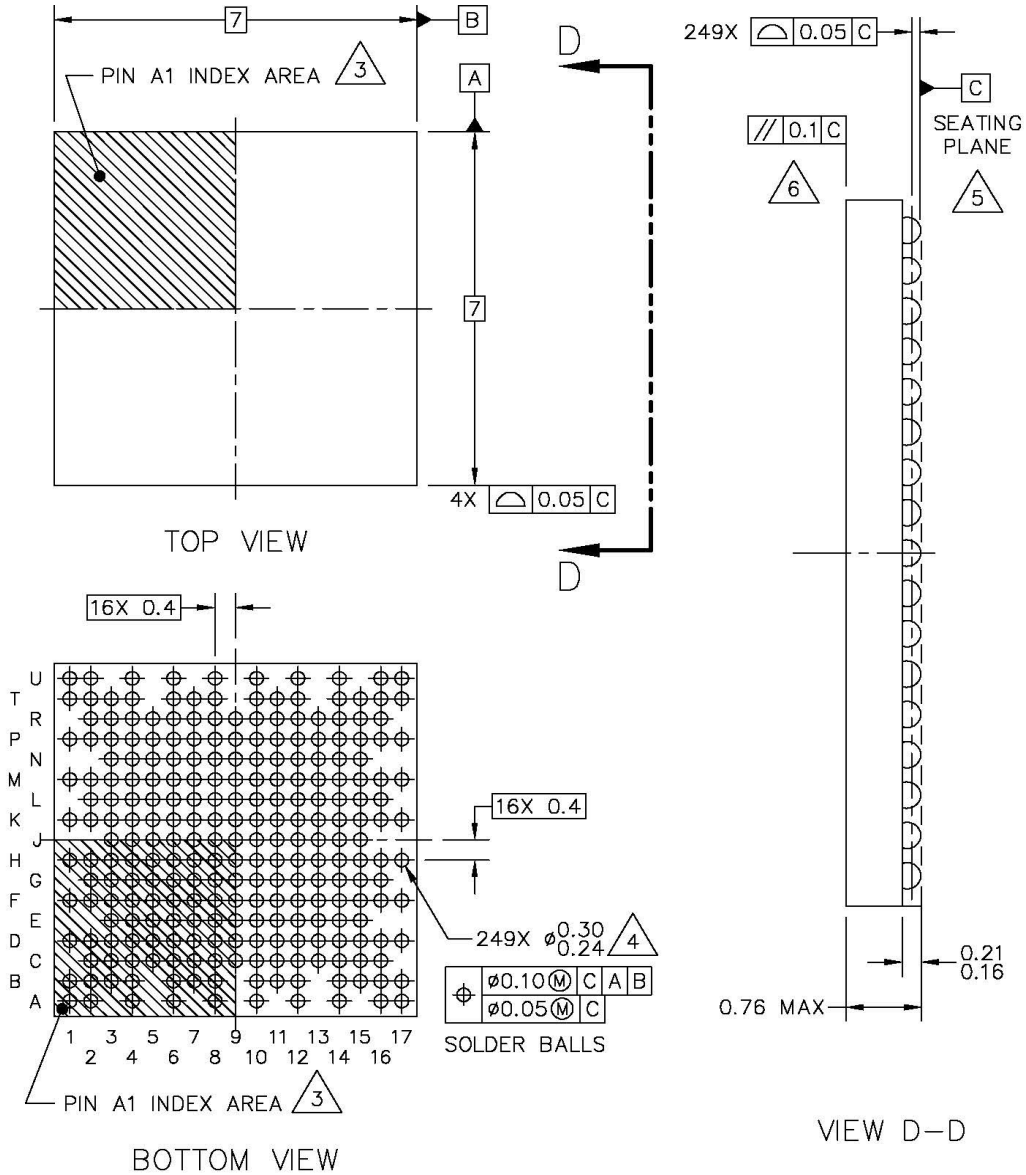


© NXP B.V. ALL RIGHTS RESERVED

DATE: 06 MAR 2019

| | | | | |
|--|------------------------|--------------------------------|-----------------|-----------------|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA01389D | REVISION: X0 | PAGE: 1 OF 3 |
|--|------------------------|--------------------------------|-----------------|-----------------|

Fig 28. WLCSP114 package



RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.



© NXP B.V. ALL RIGHTS RESERVED

DATE: 19 NOV 2018

| | | | | |
|--|------------------------|--------------------------------|----------------|-----------------|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON-JEDEC | DRAWING NUMBER: 98ASA01357D | REVISION: 0 | PAGE: 1 OF 6 |
|--|------------------------|--------------------------------|----------------|-----------------|

Fig 29. FOWLP249 package

18. Soldering

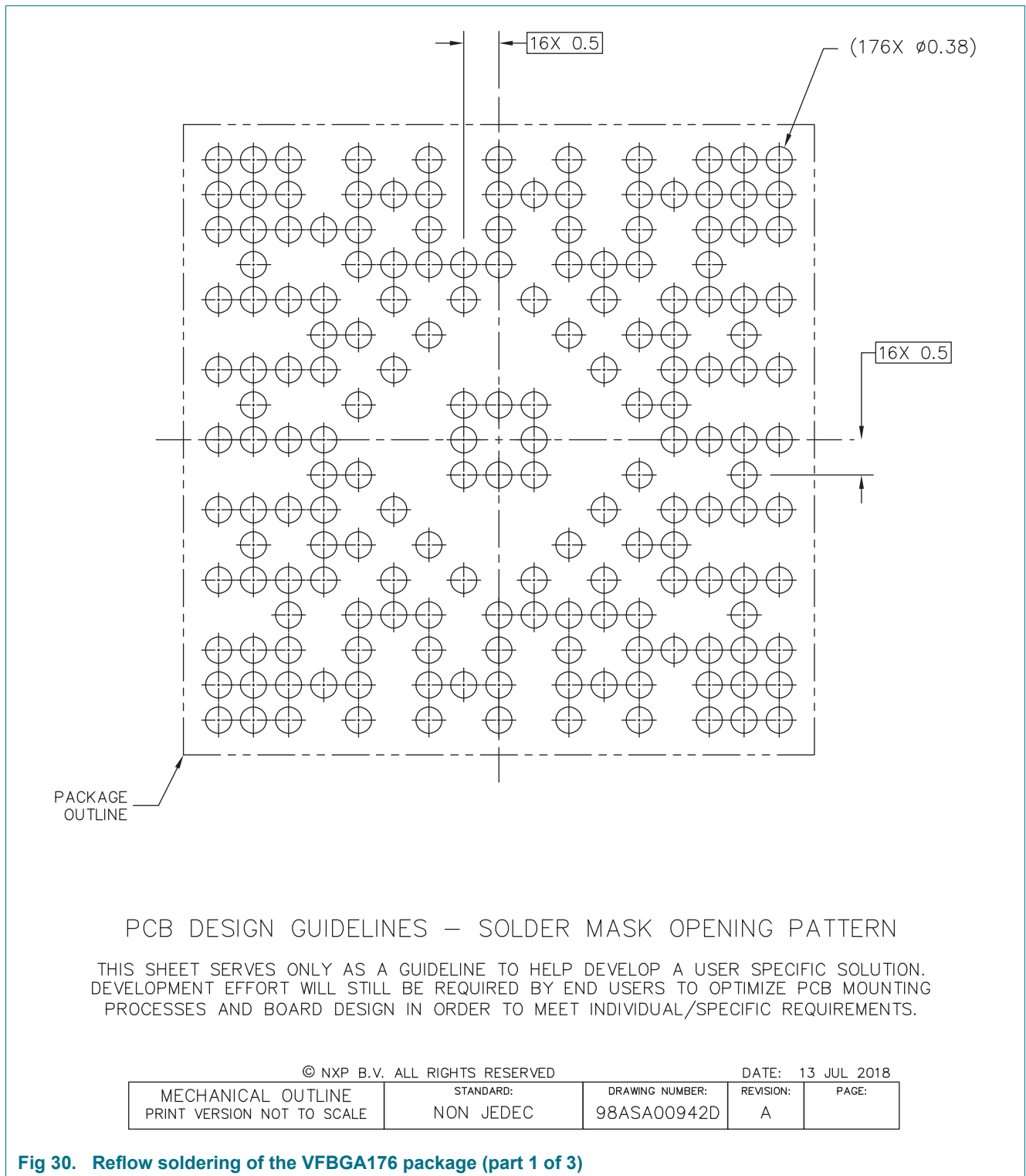
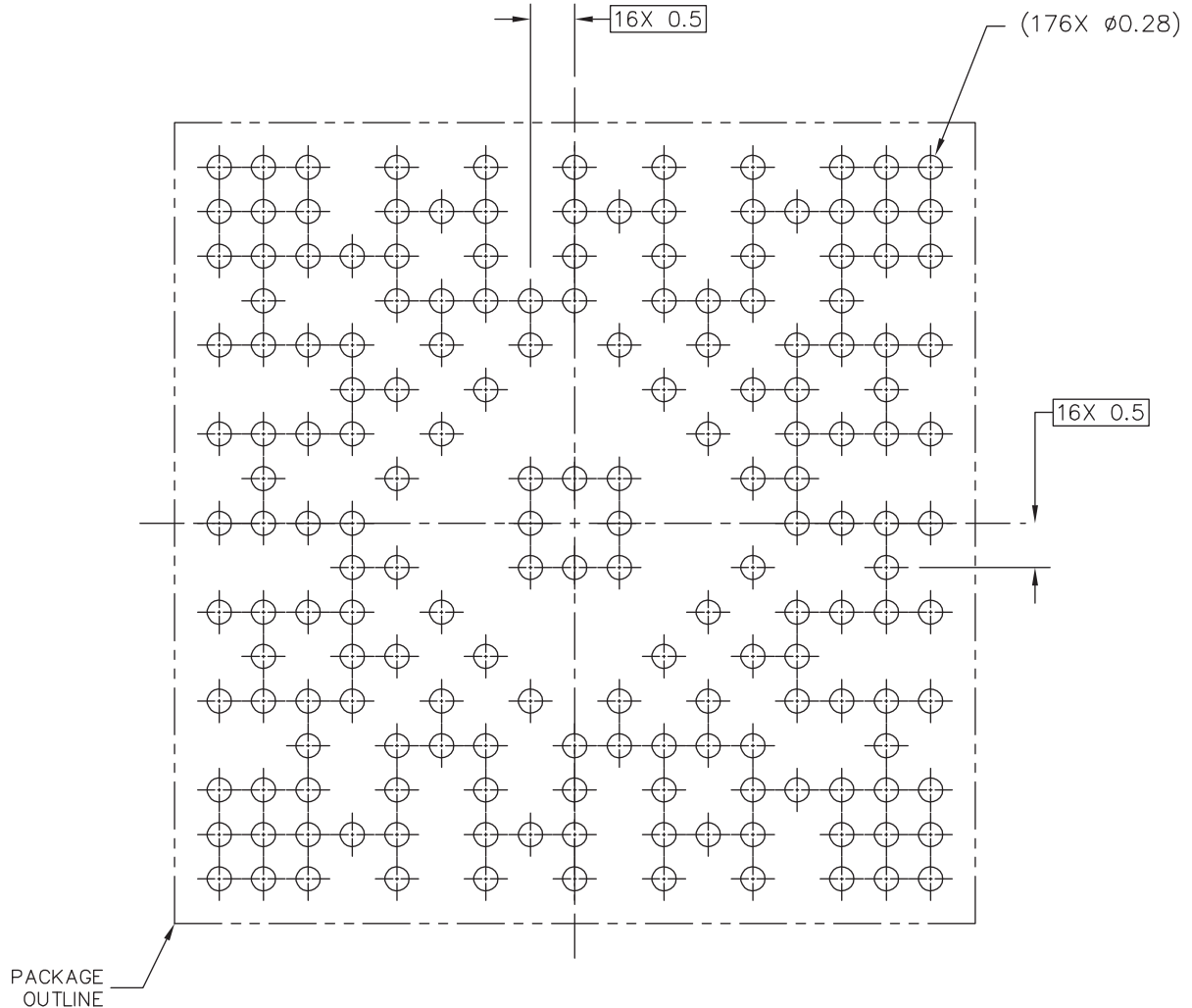


Fig 30. Reflow soldering of the VFBGA176 package (part 1 of 3)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

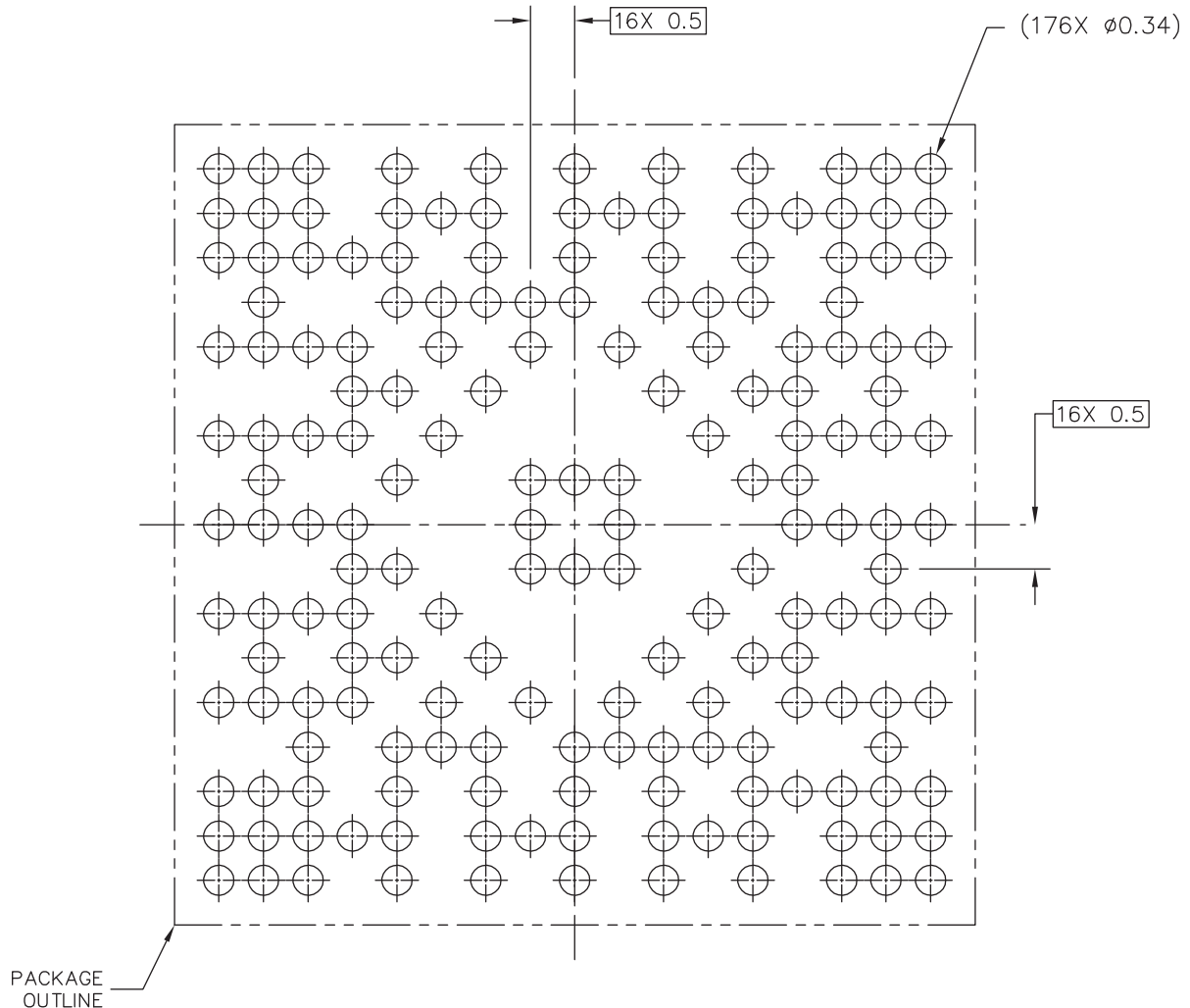
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 13 JUL 2018

| | | | | |
|--|------------------------|--------------------------------|----------------|-------|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA00942D | REVISION: A | PAGE: |
|--|------------------------|--------------------------------|----------------|-------|

Fig 31. Reflow soldering of the VFBGA176 package (part 2 of 3)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

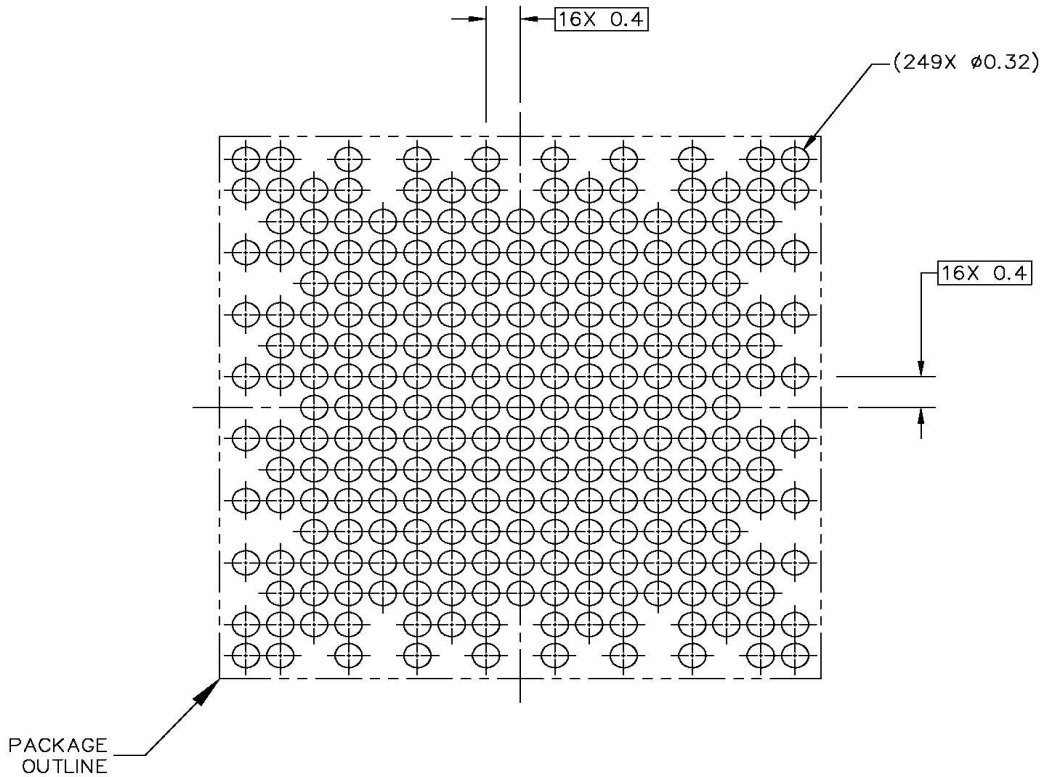
DATE: 13 JUL 2018

| | | | | |
|--------------------|-----------|-----------------|-----------|-------|
| MECHANICAL OUTLINE | STANDARD: | DRAWING NUMBER: | REVISION: | PAGE: |
|--------------------|-----------|-----------------|-----------|-------|

Fig 32. Reflow soldering of the VFBGA176 package (part 3 of 3)

FOWLP-249 I/O
7 X 7 X 0.725 PKG, 0.4 MM PITCH

SOT2003-1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



© NXP B.V. ALL RIGHTS RESERVED

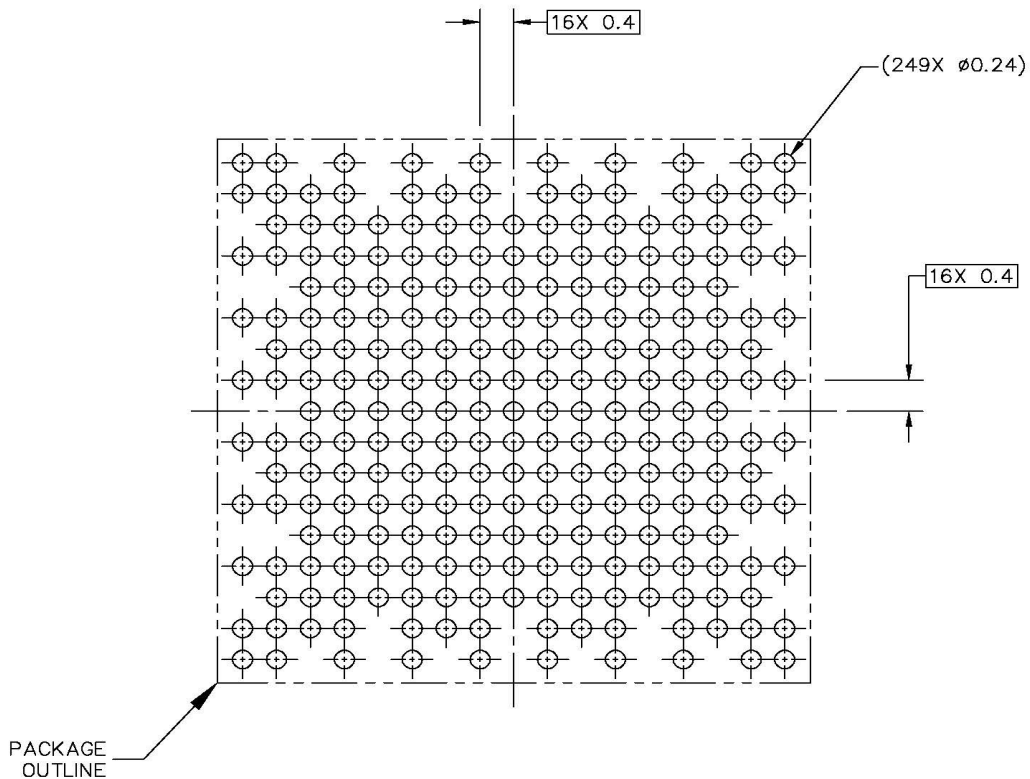
DATE: 19 NOV 2018

| | | | | |
|--|------------------------|--------------------------------|----------------|-----------------|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA01357D | REVISION: 0 | PAGE: 2 OF 6 |
|--|------------------------|--------------------------------|----------------|-----------------|

Fig 33. Reflow soldering of the FOWLP249 package (part 1 of 4)

FOWLP-249 I/O
7 X 7 X 0.725 PKG, 0.4 MM PITCH

SOT2003-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



© NXP B.V. ALL RIGHTS RESERVED

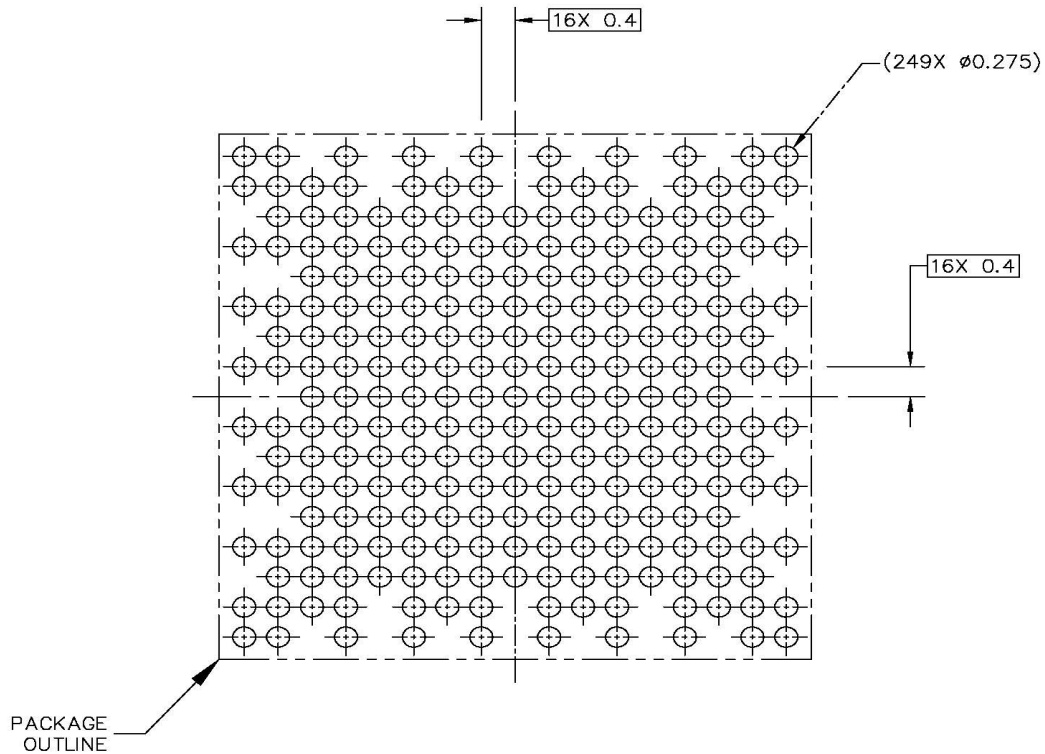
DATE: 19 NOV 2018

| | | | | |
|--|------------------------|--------------------------------|----------------|-----------------|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA01357D | REVISION: 0 | PAGE: 3 OF 6 |
|--|------------------------|--------------------------------|----------------|-----------------|

Fig 34. Reflow soldering of the FOWLP249 package (part 2 of 4)

FOWLP-249 I/O
7 X 7 X 0.725 PKG, 0.4 MM PITCH

SOT2003-1



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



© NXP B.V. ALL RIGHTS RESERVED

DATE: 19 NOV 2018

| | | | | |
|--|------------------------|--------------------------------|----------------|-----------------|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA01357D | REVISION: 0 | PAGE: 4 OF 6 |
|--|------------------------|--------------------------------|----------------|-----------------|

Fig 35. Reflow soldering of the FOWLP249 package (part 3 of 4)

FOWLP-249 I/O
7 X 7 X 0.725 PKG, 0.4 MM PITCH

SOT2003-1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.



© NXP B.V. ALL RIGHTS RESERVED

DATE: 19 NOV 2018

| | | | | |
|--|------------------------|--------------------------------|----------------|-----------------|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA01357D | REVISION: 0 | PAGE: 5 OF 6 |
|--|------------------------|--------------------------------|----------------|-----------------|

Fig 36. Reflow soldering of the FOWLP249 package (part 4 of 4)

19. Abbreviations

Table 54. Abbreviations

| Acronym | Description |
|----------------|--|
| AHB | Advanced High-performance Bus |
| APB | Advanced Peripheral Bus |
| API | Application Programming Interface |
| DMA | Direct Memory Access |
| FRO oscillator | Internal Free-Running Oscillator, tuned to the factory specified frequency |
| GPIO | General Purpose Input/Output |
| FRO | Free Running Oscillator |
| LSB | Least Significant Bit |
| MCU | MicroController Unit |
| PDM | Pulse Density Modulation |
| PLL | Phase-Locked Loop |
| SPI | Serial Peripheral Interface |
| TCP/IP | Transmission Control Protocol/Internet Protocol |
| TTL | Transistor-Transistor Logic |
| USART | Universal Asynchronous Receiver/Transmitter |

20. References

- [1] RT600. User manual UM11147
- [2] RT600. Errata sheet.
- [3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf
- [4] Cortex-M33 DGUG - ARM Cortex-M33 Devices Generic User Guide

21. Revision history

Table 55. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|----------------------------------|--------------------|---------------|------------|
| RT600 v.1.1 | 20200302 | Product data sheet | - | 1.0 |
| Modifications: | Updated minor fixes. | | | |
| RT600 v.1.0 | 20200224 | Product data sheet | - | - |
| Modifications: | Total update for product release | | | |

22. Legal information

22.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

22.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

22.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors

products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

22.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

23. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

24. Contents

| | | | | | |
|--------------|---|-----------|-----------|--|----|
| 1 | General description | 1 | 10.13.4 | Clock Generation | 66 |
| 1.1 | Peripherals | 1 | 10.13.5 | Safety | 68 |
| 1.2 | Shared system SRAM | 2 | 10.14 | Power control | 68 |
| 2 | Features and benefits | 2 | 10.14.1 | Sleep mode | 69 |
| 3 | Applications | 7 | 10.14.2 | Deep-sleep mode | 69 |
| 4 | Ordering information | 8 | 10.14.3 | Deep power-down mode and Full Deep power-down mode | 69 |
| 4.1 | Ordering options | 9 | 10.14.4 | Peripheral configuration in reduced power modes 69 | |
| 5 | Marking | 10 | 10.15 | General Purpose I/O (GPIO) | 72 |
| 6 | Block diagram | 11 | 10.15.1 | Features | 72 |
| 7 | Pinning information | 14 | 10.16 | Pin interrupt/pattern engine | 72 |
| 8 | Power Supply for pins | 48 | 10.16.1 | Features | 73 |
| 9 | Termination of unused pins | 49 | 10.17 | Communications peripherals | 73 |
| 9.0.1 | Pin states in different power modes | 49 | 10.17.1 | High-speed USB Host/Device interface (USB1) 73 | |
| 10 | Functional description | 50 | 10.17.1.1 | USB1 device controller | 73 |
| 10.1 | Architectural overview | 50 | 10.17.1.2 | USB1 host controller | 74 |
| 10.2 | Arm Cortex-M33 processor | 50 | 10.17.2 | FlexSPI Flash Interface | 74 |
| 10.3 | Arm Cortex-M33 integrated Floating Point Unit (FPU) | 50 | 10.17.2.1 | Features | 74 |
| 10.4 | Xtensa HiFi 4 advanced Audio Digital Signal Processor | 50 | 10.17.3 | SD/eMMC Interfaces | 75 |
| 10.5 | Memory Protection Unit (MPU) | 51 | 10.17.4 | Flexcomm Interface serial communication | 75 |
| 10.6 | Nested Vectored Interrupt Controller (NVIC) for Cortex-M33 | 51 | 10.17.4.1 | Features | 75 |
| 10.6.1 | Features | 51 | 10.17.4.2 | SPI serial I/O controller (Flexcomm Interfaces 0 - 7) | 75 |
| 10.6.2 | Interrupt sources | 51 | 10.17.4.3 | I ² C-bus interface | 76 |
| 10.7 | System Tick timer (SysTick) | 51 | 10.17.4.4 | USART | 76 |
| 10.8 | PowerQuad Hardware Accelerator | 51 | 10.17.4.5 | I ² S-bus interface | 77 |
| 10.9 | On-chip static RAM | 52 | 10.17.5 | High-Speed SPI interface (Flexcomm Interface 14) | 78 |
| 10.10 | On-chip ROM | 52 | 10.17.6 | I3C interface | 78 |
| 10.11 | OTP | 52 | 10.17.6.1 | Features | 78 |
| 10.12 | Memory mapping | 52 | 10.18 | Counter/timer peripherals | 78 |
| 10.12.1 | AHB multilayer matrix | 52 | 10.18.1 | General-purpose 32-bit timers/external event counter | 78 |
| 10.12.2 | Memory Protection Unit (MPU) | 52 | 10.18.1.1 | Features | 79 |
| 10.12.3 | TrustZone and Cortex-M33 busing on this device 53 | | 10.18.2 | SCTimer/PWM | 79 |
| 10.12.4 | Links to specific memory map descriptions and tables | 53 | 10.18.2.1 | Features | 80 |
| 10.12.5 | Device overview | 55 | 10.18.3 | Windowed WatchDog Timer (WWDT) | 80 |
| 10.12.6 | Cortex-M33 Memory overview | 57 | 10.18.3.1 | Features | 80 |
| 10.12.7 | Shared RAM detail | 58 | 10.18.4 | Real Time Clock (RTC) timer | 81 |
| 10.12.8 | APB peripherals | 60 | 10.18.5 | Multi-Rate Timer (MRT) | 81 |
| 10.12.9 | AHB peripherals | 61 | 10.18.5.1 | Features | 81 |
| 10.12.10 | HiFi 4 memory map | 63 | 10.18.6 | OS/Event Timer | 81 |
| 10.12.10.1 | Using cacheable and non-cacheable memory regions | 64 | 10.18.6.1 | Features | 81 |
| 10.13 | System control | 64 | 10.18.7 | Micro-Tick Timer | 82 |
| 10.13.1 | Clock sources | 64 | 10.18.7.1 | Features | 82 |
| 10.13.1.1 | 12 MHz Free Running Oscillator (FRO) | 64 | 10.19 | Other digital peripherals | 82 |
| 10.13.1.2 | 48/60 MHz Free Running Oscillator (FRO) | 64 | 10.19.1 | DMA controller | 82 |
| 10.13.1.3 | 1 MHz Low-Power oscillator | 65 | 10.19.1.1 | Features | 82 |
| 10.13.1.4 | Crystal oscillator | 65 | 10.19.2 | DMIC subsystem | 82 |
| 10.13.1.5 | 32 kHz oscillator | 65 | 10.19.2.1 | Features | 82 |
| 10.13.2 | System PLL (PLL0) | 65 | 10.19.3 | CRC engine | 83 |
| 10.13.3 | Audio PLL (PLL2) | 65 | 10.19.3.1 | Features | 83 |
| | | | 10.20 | Analog peripherals | 83 |
| | | | 10.20.1 | 12-bit Analog-to-Digital Converter (ADC) | 83 |

| | | | | | |
|-----------|--|------------|-----------|---|------------|
| 10.20.1.1 | Features | 83 | 16.2 | I/O power consumption | 128 |
| 10.20.2 | Temperature sensor | 84 | 16.3 | RTC oscillator | 129 |
| 10.20.3 | Analog Comparator | 84 | 16.3.1 | RTC Printed Circuit Board (PCB) design guidelines | 130 |
| 10.21 | Security features | 84 | 16.4 | XTAL oscillator | 131 |
| 10.21.1 | Features | 84 | 16.4.1 | XTAL Printed Circuit Board (PCB) design guidelines | 132 |
| 10.21.2 | AES256 | 84 | 16.5 | Suggested USB interface solutions | 132 |
| 10.21.3 | SHA-1 and SHA-2 | 85 | 17 | Package outline | 134 |
| 10.21.3.1 | Features | 85 | 18 | Soldering | 137 |
| 10.21.4 | PUF | 85 | 19 | Abbreviations | 144 |
| 10.21.4.1 | Features | 85 | 20 | References | 144 |
| 10.21.5 | CASPER co-processor | 85 | 21 | Revision history | 145 |
| 10.21.6 | Random Number Generator (RNG) | 85 | 22 | Legal information | 146 |
| 10.21.7 | On-the-Fly Decryption on Octal/Quad SPI interface (OTFAD) | 85 | 22.1 | Data sheet status | 146 |
| 10.21.8 | Universally Unique Identifier (UUID) | 86 | 22.2 | Definitions | 146 |
| 10.21.9 | Device Identifier Composition Engine (DICE) | 86 | 22.3 | Disclaimers | 146 |
| 10.22 | Emulation and debugging | 86 | 22.4 | Trademarks | 147 |
| 11 | Limiting values | 87 | 23 | Contact information | 147 |
| 12 | Thermal characteristics | 89 | 24 | Contents | 148 |
| 13 | Static characteristics | 90 | | | |
| 13.1 | General operating conditions | 90 | | | |
| 13.2 | Power Sequencing | 93 | | | |
| 13.3 | CoreMark data | 95 | | | |
| 13.4 | Power consumption | 95 | | | |
| 13.5 | Pin characteristics | 101 | | | |
| 14 | Dynamic characteristics | 103 | | | |
| 14.1 | Wake-up process | 103 | | | |
| 14.2 | IRC (48 MHz/60 MHz and 16 MHz) | 103 | | | |
| 14.3 | Internal Low Power Oscillator (1 MHz) | 104 | | | |
| 14.4 | Crystal oscillator | 104 | | | |
| 14.5 | RTC oscillator | 104 | | | |
| 14.6 | External Clock Input (CLKIN pin) | 105 | | | |
| 14.7 | I ² C-bus | 106 | | | |
| 14.8 | I ² S-bus interface | 108 | | | |
| 14.9 | USART interface | 110 | | | |
| 14.10 | SPI interfaces (Flexcomm Interfaces 0-7) | 111 | | | |
| 14.11 | High Speed SPI Interface (Flexcomm Interface 14) | 114 | | | |
| 14.12 | FlexSPI flash interface | 117 | | | |
| 14.13 | SD/MMC and SDIO | 119 | | | |
| 14.14 | DMIC subsystem | 121 | | | |
| 14.15 | SCTimer/PWM output timing | 121 | | | |
| 15 | Analog characteristics | 122 | | | |
| 15.1 | 12-bit ADC characteristics | 122 | | | |
| 15.1.1 | ADC input impedance | 124 | | | |
| 15.2 | Temperature sensor | 124 | | | |
| 15.2.1 | Comparator | 126 | | | |
| 16 | Application information | 128 | | | |
| 16.1 | Standard I/O pin configuration | 128 | | | |

continued >>

