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MAX22007

Four-Channel 12-Bit Configurable Analog Output with Integrated Voltage Reference

General Description

The MAX22007 is a software-configurable four-channel analog output device that drives a voltage or current output on each channel. All outputs are protected to ±42V_{P-P} for high-voltage supply of HVDD = 8V to 20V and HVSS = -2V to 0V.

Each output channel of the MAX22007 features a 12-bit DAC with fast settling time using a shared internal voltage reference. The device offers low-offset, high-voltage amplifiers to condition the signal from low-voltage DAC outputs to high-voltage or current outputs. If one output is miswired, all other outputs remain unaffected and function normally. For each channel, an internal comparator can be used to determine the load impedance and allows the microcontroller to intelligently select for voltage or current output mode. All outputs are kept safe by integrated current protection for functional and thermal robustness. The MAX22007 also includes a thermal shutdown circuit that protects the device when the junction temperature exceeds 165°C (typ).

The MAX22007 communicates with a microcontroller using a SPI interface at clock rates up to 30MHz with an optional eight-bit CRC for improved data integrity. Eight GPIOs can be used to interface and control other resources in the application circuit. The MAX22007 operates from a 2.7V to 5.5V V_{DD} low-voltage supply and an 8V to 24V HVDD positive high-voltage supply. The negative voltage supply HVSS can be set between -2V and 0V.

The MAX22007 is available in an 8mm x 8mm 56-pin TQFN package and operates over the -40°C to +85°C temperature range with 2.5kV HBM ESD protection on all pins.

Applications

- Building Automation Analog Outputs
- Configurable Analog Output Cards
- Factory Automation Analog Outputs
- Process Automation
- Programmable Logic Controllers

Benefits and Features

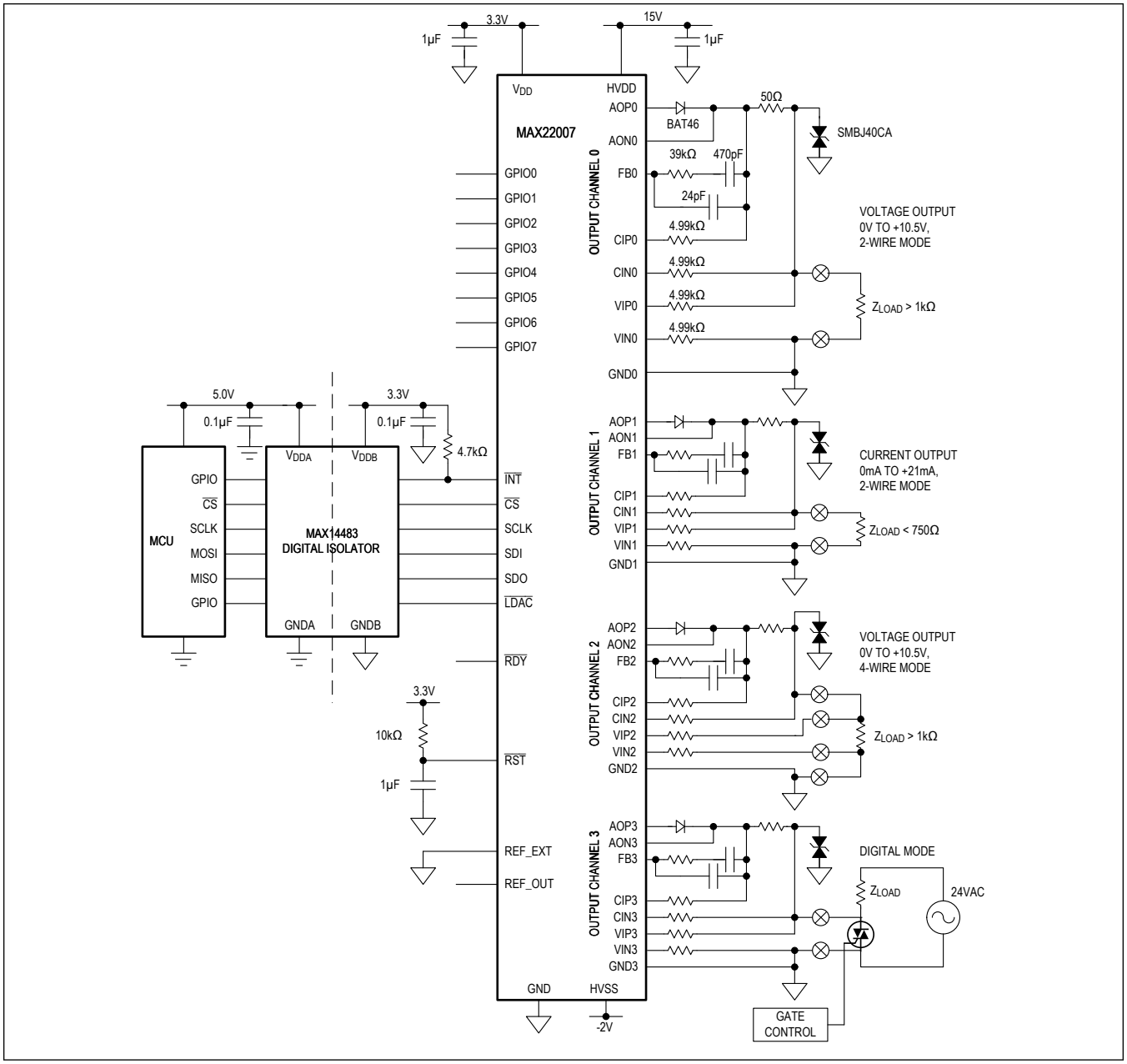
- Configurable Outputs
  - Each Output Individually Configurable
  - Internal Comparator to Allow Calculating Load Impedance for Voltage-Mode or Current-Mode
  - Voltage Mode is 0V to 10.5V Linear Range with 12.5V Overrange for Loads from 1kΩ to 1MΩ
  - Current Mode is 0mA to 21mA Linear Range with 25mA Overrange for Loads from 0Ω to 750Ω
- System Accuracy
  - V/I Output Resolution is 12-Bits
  - Factory Calibrated for Gain and Offset Error within ± 0.2% at +25°C
  - V/I Total Unadjusted Error Less Than ± 1% from -40°C to +85°C
- Robust with Integrated Diagnostics
  - ±42V_{P-P} Protection for Output Drivers
  - ±1kV Surge Protection with 4.99kΩ Series Resistors at Input Pins
  - ±2.5kV HBM ESD Protection on All Pins
  - Outputs have Short-Circuit and Overvoltage Protection with External Diodes
  - Thermal Monitoring and Shutdown Protection
- Simple and Low-Cost Interface
  - Up to 30MHz SPI Serial Interface with Optional 8-Bit CRC
  - Daisy-Chain Mode to Reduce System Cost
  - V_{DD} = 2.7V to 5.5V for Easy Interface to the Microcontroller
  - High Voltage Output Supplies:
    - HVDD: +8V to +24V
    - HVSS: -2V to 0V
- Robust Performance in a Compact Package
  - -40°C to 85°C Operating Temperature Range
  - 56-pin TQFN, 8mm x 8mm

***Ordering Information* and *Typical Application Circuits* appear at the end of the datasheet.**

19-100860; Rev 0; 9/20

maxim integrated™

Quad Configurable Analog Output



Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V to +6V
V_{DD} to HVSS ..... -0.3V to +6V
GND_ to GND ..... -0.3V to +0.3V
HVDD to HVSS ..... -0.3V to +40V
HVDD to AON_ ..... -70V to +70V
HVDD to GND ..... -0.3V to +40V
HVDD to GND_ ..... -0.3V to +40V
GND to HVSS ..... -0.3V to +6V
GND_ to HVSS ..... -0.3V to +6V
AOP_ to HVDD ..... -70V to +0.3V
FB_, CIP_, CIN_, VIP_, VIN_ to HVSS ..... -0.3V to min(+40V, ((V_{HVDD} - V_{HVSS}) + 0.3V))
CIP_, CIN_, VIP_, VIN_ to HVSS (with 4.99kΩ series resistors) ..... -42V to +42V
AON_ to HVSS ..... -70V to +70V
INT, CS, SCLK, SDI to GND ..... -0.3V to +6V
All Other Pins to GND ..... -0.3V to min(+6V, (V_{DD} + 0.3V))
Maximum Current into AOP_, AON_ ..... ±100mA
Maximum Current into Any Other Pin ..... ±50mA
Continuous Power Dissipation (T_A = +70ºC)
56-TQFN (derate 47.6mW/°C above +70°C) 3809.5mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

56-PIN TQFN

Package Code	T5688+4C
Outline Number	21-0135
Land Pattern Number	90-0047
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	21°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 3.3V, V_{HVDD} = +15V, V_{HVSS} = 0V, Internal Reference, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG OUTPUT-VOLTAGE MODE						
Output-Voltage Range	V_{OUT}	DAC full-scale range (Note 2)		0 to 12.5		V
		Linear range, V_{HVSS} = 0V (Notes 2, 3)	0.3		10.5	
		Linear Range, V_{HVSS} = -2V (Notes 2, 3)	0.02		10.5	
Dropout Voltage		V_{OUT} = 12.5V, sourcing 25mA, measured between HVDD and AOP_, gain compression < 1%			1.0	V
Output-Current Protection		Output shorted to HVDD or HVSS, threshold current (Note 4)		50		mA
		Output shorted to HVDD or HVSS, average current (Note 4)		7		

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{HVDD} = +15V, V_{HVSS} = 0V, Internal Reference, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AOP_ and AON_ High-Impedance Leakage Current		V_{OUT} = 0V to +10.5V		±25		µA
Offset Error	V_{OFF}	T_A = +25°C, no load, extrapolated from the linear range (Note 5)			±10	mV
Offset Drift		T_A = -40°C to 85°C (Note 6)		±10		µV/°C
Gain Error		T_A = +25°C, no load (Note 5)			±0.2	%
Gain Drift		T_A = -40°C to 85°C (Note 6)		±10		ppm/°C
INL Error	INL	T_A = +25°C, no load (Note 5)	-1	±0.5	+1	LSB
INL Drift		T_A = -40°C to 85°C (Note 6)		±1		µV/°C
Output Noise	V_n	10kHz BW		100		μV_{RMS}
Voltage Output Total Unadjusted Error	V_{TUE}	V_{OUT} = 0.02V to 10.5V, no load (Notes 5, 7)			±100	mV
Voltage Crosstalk	V_{CT}	Channel under test is in voltage mode with V_{OUT} = 10.5V, I_{OUT} = 10mA. All other channels are in current mode forcing 0mA and 20mA to a 0Ω load. The crosstalk is the voltage variation of the channel under test. (Note 6)			25	mV
Supply Rejection Ratio	PSRR	DC, V_{OUT} = 300mV, V_{HVDD} = +8V to +24V		100		dB
Load Regulation		0 ≤ I_{LOAD} ≤ +10.5mA, measured at V_{OUT} = +10.5V, output change due to self-heating excluded		±0.1		mV
VIP_ and VIN_ Input-Voltage Range		(Note 3)	V_{HVSS}		V_{HVDD} - 2.5	V
VIP_ and VIN_ Input Current		$V_{VIP\_}$, $V_{VIN\_}$ = 20mV to 10.5V		±2		µA
Settling Time		Resistive load from 1kΩ to 10MΩ; settling to 1% of step size for V_{OUT} = 20mV to 10.5V		0.3		ms
		Capacitive load up to 1µF; settling to 1% of step size for V_{OUT} = 20mV to 10.5V		1		
ANALOG OUTPUT-CURRENT MODE						
Output-Current Range	I_{OUT}	R_{SENSE} = 50Ω, DAC full-scale range (Note 8)		0 to 25		mA
		Linear range, V_{HVSS} = 0V (Notes 3, 8)	1.5		21	
		Linear range, V_{HVSS} = -2V (Notes 3, 8)	0.04		21	
Dropout Voltage		V_{HVDD} = 12V, Sourcing 25mA, measured between HVDD and AOP_, gain compression < 1%			0.85	V
Offset Error	I_{OFF}	T_A = +25°C, R_{LOAD} = 250Ω, extrapolated from the linear range (Note 5)			±20	µA

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{HVDD} = +15V, V_{HVSS} = 0V, Internal Reference, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Offset Drift		T_A = -40°C to 85°C (Note 6)		±20		nA/°C
Gain Error		T_A = +25°C, R_{LOAD} = 250Ω (Note 5)			±0.2	%
Gain Drift		T_A = -40°C to 85°C (Note 6)		±10		ppm/°C
INL Error	INL	TA = +25°C, R_{LOAD} = 250Ω (Note 5)	-1	+0.5	+1	LSB
INL Drift		T_A = -40°C to 85°C (Note 6)		±5		nA/°C
Output Noise	I_n	10kHz BW		0.5		μA_{RMS}
Current Output Total Unadjusted Error	I_{TUE}	I_{OUT} = 40µA to 21mA, R_{LOAD} = 250Ω (Notes 5, 9)			±200	µA
Current Crosstalk	I_{CT}	Channel under test is in current mode with I_{OUT} = 21mA, V_{OUT} = 10V. All other channels are in current mode forcing 0mA and 20mA to a 0Ω load. The crosstalk is the current variation of the channel under test. (Note 6)			50	µA
Supply Rejection	PSR	DC, I_{OUT} = 3mA, V_{HVDD} = +8V to +24V		0.1		µA/V
CIP_ and CIN_ Input-Voltage Range		(Note 3)	V_{HVSS}		V_{HVDD} - 2.5	V
CIP_ and CIN_ Input Current		$V_{CIP\_}$, $V_{CIN\_}$ = 0V to +12V		±2		µA
Common-Mode Rejection	CMR	Current mode, $V_{CIN\_}$ = 0V to +11V, measured at I_{OUT} = 1.5mA			10	µA/V
CIP_ to CIN_ Differential-Input Range				1.25		V
CIP_ to CIN_ Differential-Input Impedance				100		kΩ
Settling Time		Resistive load up to 250Ω; settling to 1% of step size for I_{OUT} = 40µA to 21mA		0.5		ms
		Resistive load up to 500Ω; settling to 1% of step size for I_{OUT} = 40µA to 21mA		1.0		
		Inductive load up to 1mH; settling to 1% of step size for I_{OUT} = 40µA to 21mA		0.5		
COMPARATOR						
Offset	V_{OFF}			±50		mV
Delay	t_{DELAY}			64		µs
Nominal Trip Voltage	V_{TH}			500		mV
REFERENCE						
REF_OUT Output Voltage	V_{REF_OUT}	T_A = +25°C	2.494	2.5	2.506	V
Output-Voltage Temperature Coefficient		T_A = -40°C to +85°C (Note 6)		±10	±25	ppm/°C

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{HVDD} = +15V, V_{HVSS} = 0V, Internal Reference, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input Logic-Low Voltage	V_{IL}				0.3 × V_{DD}	V
Input Logic-High Voltage	V_{IH}		0.7 × V_{DD}			V
Input Hysteresis	V_{HYS}			300		mV
Input Leakage Current	I_{IN}		-1		+1	µA
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUTS						
Output Logic-Low Voltage	V_{OL}	I_{OL} = 4mA, sinking			0.4	V
Output Logic-High Voltage (SDO, $\overline{RDY}$, GPIO7 to GPIO0)	V_{OH}	I_{OH} = 4mA, sourcing	0.9 × V_{DD}			V
Three-State Leakage Current			-10		+10	µA
Three-State Output Capacitance				10		pF
SPI TIMEOUT						
Timeout Interval Accuracy		With respect to nominal value	-50		+50	%
SUPPLIES						
Analog Supply Voltage	V_{DD}		2.7	3.3	V_{HVSS} + 5.5	V
Positive High-Voltage Supply	V_{HVDD}		8		V_{HVSS} + 24	V
		±42V_{P-P} output protection (Note 6)	8		20	
Negative High-Voltage Supply	V_{HVSS}		-2	0	0	V
Analog Supply Quiescent Current	I_{DD}	All channels and comparators powered up		1.5		mA
High-Voltage Quiescent Current	I_{HV}	All channels and comparators powered up, no load current		4.5		mA
TIMING CHARACTERISTICS						
SCLK Frequency	f_{SCLK}				30	MHz
SCLK Clock Period	t_{CP}		33			ns
SCLK Pulse-Width High	t_{CH}		13			ns
SCLK Pulse-Width Low	t_{CL}	Read transactions must also meet t_{DOT}	13			ns
$\overline{CS}$ Fall Setup Time	t_{CSS0}	$\overline{CS}$ falling edge to 1st SCLK rising edge setup time	10			ns

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{HVDD} = +15V, V_{HVSS} = 0V, Internal Reference, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Rise Setup Time	t_{CSS1}	SCLK rising edge to $\overline{CS}$ rising edge setup time	5			ns
$\overline{CS}$ Fall Hold Time	t_{CSH0}	SCLK rising edge to $\overline{CS}$ falling edge hold time	0			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}	Minimum $\overline{CS}$ pulse-width high	150			ns
SDI Setup Time	t_{DS}	SDI setup time to SCLK rising edge	10			ns
SDI Hold Time	t_{DH}	SDI hold time after SCLK rising edge	5			ns
SDO Transition Time	t_{DOT}	SDO transition valid after SCLK falling edge			20	ns
SDO Hold Time	t_{DOH}	Output remains valid after falling edge of SCLK	3			ns
SDO Disable Time	t_{DOD}	Last SCLK falling edge to SDO disable, C_{LOAD} = 20pF			25	ns
$\overline{RDY}$ Fall Transition Time	t_{RT0}	Last SCLK falling edge to $\overline{RDY}$ falling edge			40	ns
$\overline{RDY}$ Rise Transition Time	t_{RT1}	$\overline{CS}$ rise to $\overline{RDY}$ rise			40	ns
THERMAL PROTECTION						
Chip Thermal Shutdown Temperature	T_{CSHDN}	Temperature rising		165		°C
Chip Thermal Warning Temperature	T_{CWARN}	Temperature rising		145		°C
Chip Thermal Warning Hysteresis	T_{HYS}			10		°C
EMC PROTECTION						
ESD	V_{ESD}	All pins, Human Body Model		±2.5		kV
Surge	V_{SURGE}	AOP_, AON_, FB_, CIP_, CIN_, VIP_, VIN_ to GND, IEC 61000-4-5 with external 4.99kΩ series resistors on CIP_, CIN_, VIP_ and VIN_ pins, and a bidirectional TVS on AOP_ and AON_ pins.		±1		kV

Note 1: Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.

Note 2: The output voltage is measured at the sense voltage input (VIP_). The minimum supply voltage required is the sum of the output voltage V_{OUT}, the voltage across the sense resistor, the diode forward voltage, and the dropout voltage. For a 25mA load current, a +12V output, a 50Ω sense resistor, and a diode forward voltage of 550mV (BAT46), the minimum required supply voltage is +14.8V.

Note 3: Offset Error, Gain Error, INL Error, and Settling Times are only guaranteed in the linear range. For Analog Output Current Mode Offset Error, Gain Error, INL Error, and Settling Times are only guaranteed in the specified Input Common-Mode Range ($V_{CIP\_}$ + $V_{CIN\_}$)/2 of 0V to +12V. Offset Error, Gain Error, and INL Error are measured using the following DAC codes:

- Analog Output Voltage Mode:
  - V_{HVSS} = 0V: code 98 and code 3441
  - V_{HVSS} = -2V: code 6 and code 3441
- Analog Output Current Mode:
  - V_{HVSS} = 0V: code 245 and code 3441
  - V_{HVSS} = -2V: code 6 and code 3441

The minimum and maximum specification of the linear range and input-voltage range are guaranteed through Offset Error, Gain Error, and INL Error.

Note 4: The threshold current specifies the typical current that triggers the short-circuit protection. The average current that accounts for self-heating of the device is significantly smaller due to the duty cycle when OVC_CNFG is set to logic low.

Note 5: Measured with only one channel powered up.

Note 6: Guaranteed by design and characterization. Not tested in production.

Note 7: The Voltage Output Total Unadjusted Error (V_{TUE}) does not include errors caused by Voltage Crosstalk and Load Regulation.

Note 8: The minimum supply voltage required is the output current times the sum of the load and cable resistors, the voltage across the sense resistor, the diode forward voltage, and the dropout voltage. For a 25mA output current, a load resistor of 500Ω, a cable resistance of 250Ω, a 50Ω sense resistor, and a diode forward voltage of 550mV (BAT46), the minimum required supply voltages is +21.4V.

Note 9: The Current Output Total Unadjusted Error (I_{TUE}) does not include errors caused by Current Crosstalk and Common-Mode Rejection (if a load resistance other than 250Ω is used).

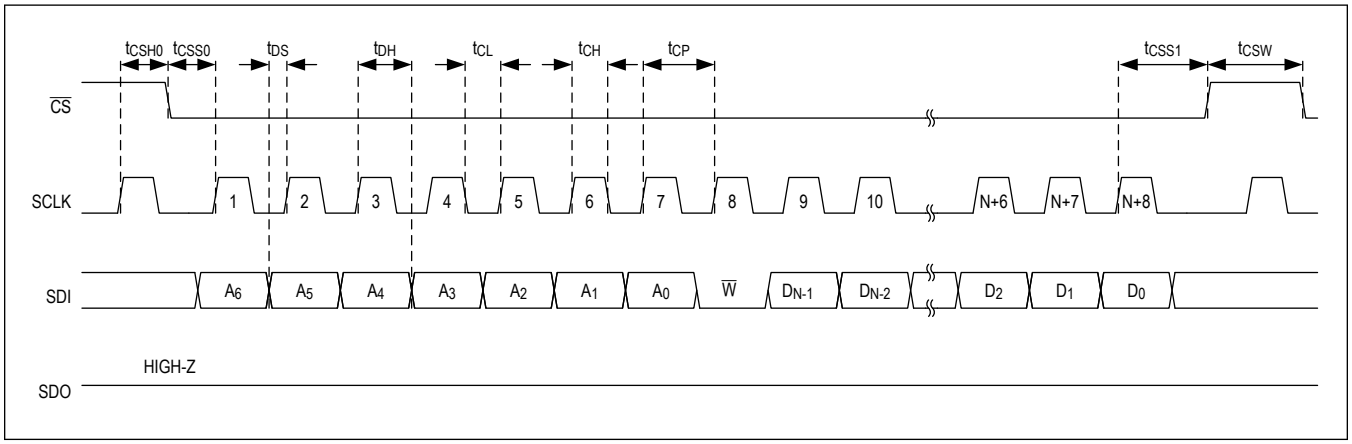


Figure 1. SPI Write Timing (N = 16 when CRC is disabled, and N = 24 when CRC is enabled)

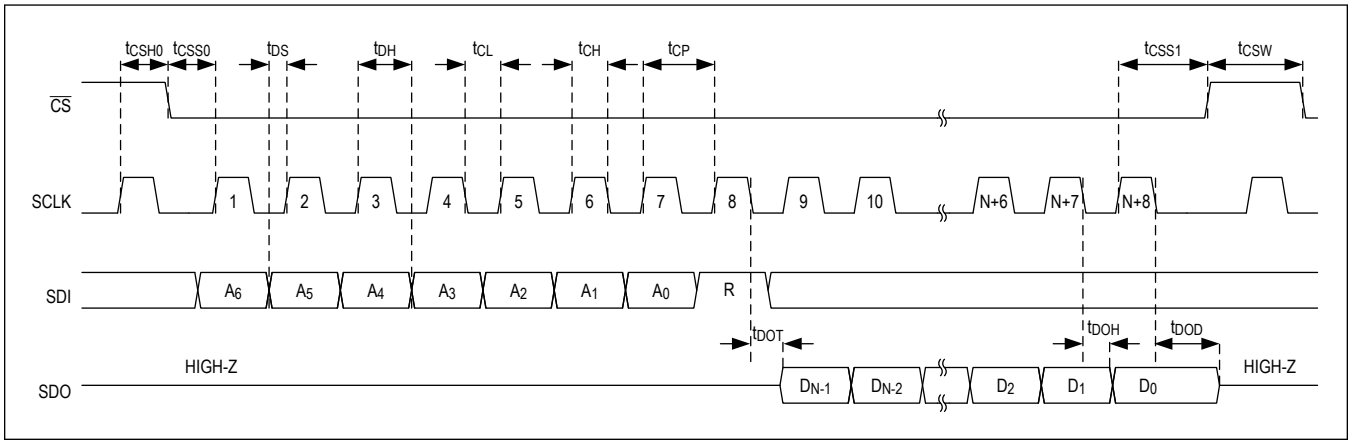


Figure 2. SPI Read Timing (N = 16 when CRC is disabled, and N = 24 when CRC is enabled)

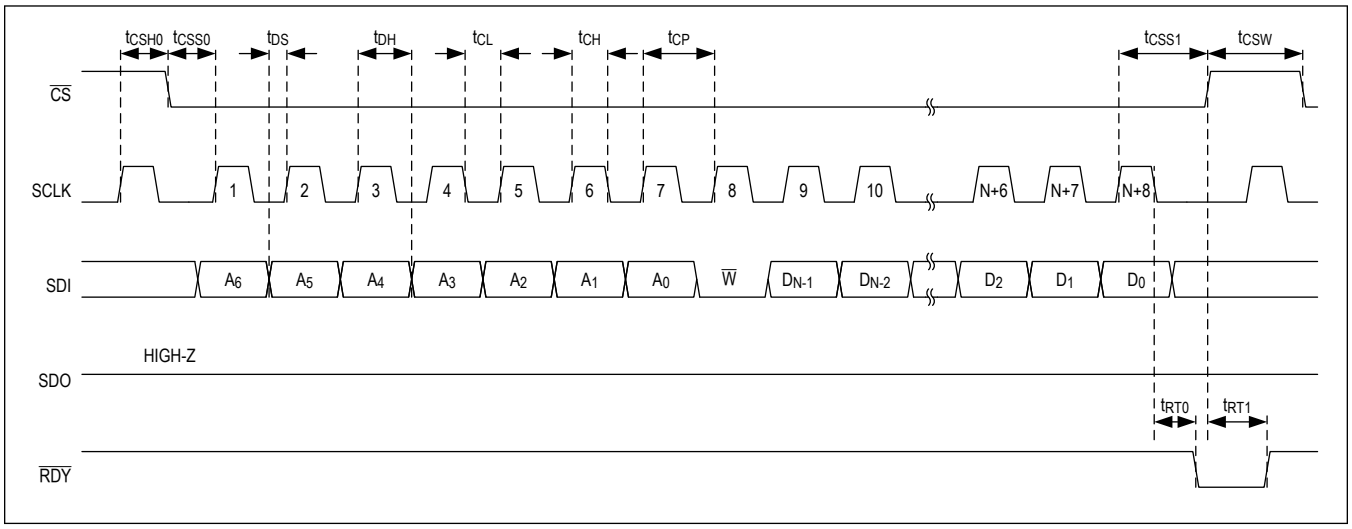
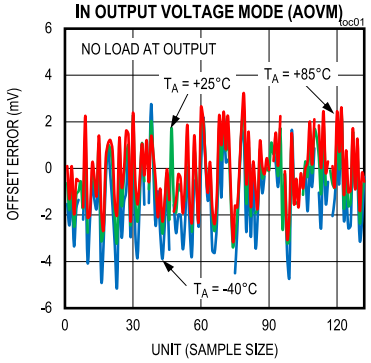


Figure 3. Elongated SPI Write Timing for Daisy-Chain Applications (N = 16 when CRC is disabled, and N = 24 when CRC is enabled)

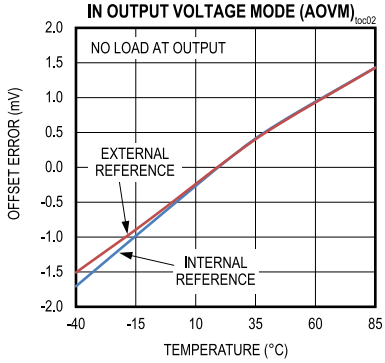
Typical Operating Characteristics

(V_{DD} = +3.3V, V_{HVDD} = +15V, V_{HVSS} = 0V, Internal Reference, T_A = 25°C, unless otherwise noted)

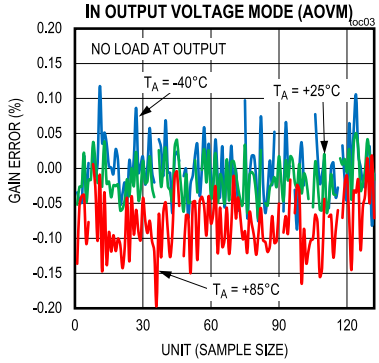
OFFSET-ERROR DISTRIBUTION IN OUTPUT VOLTAGE MODE (AOVM)



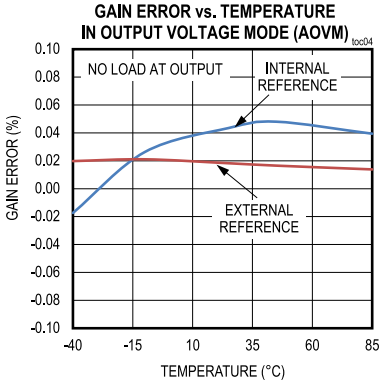
OFFSET ERROR vs. TEMPERATURE IN OUTPUT VOLTAGE MODE (AOVM)



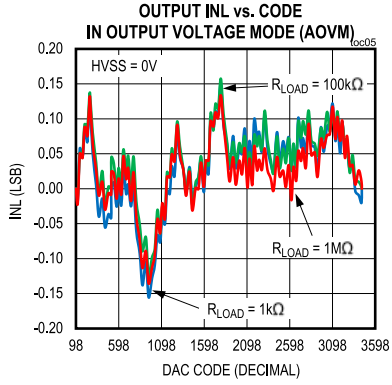
GAIN-ERROR DISTRIBUTION IN OUTPUT VOLTAGE MODE (AOVM)



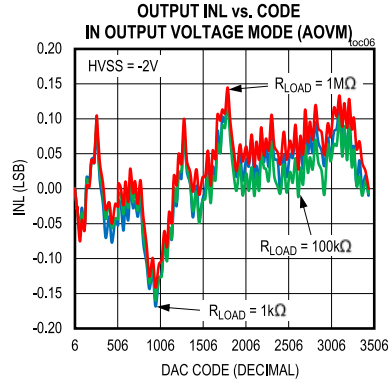
GAIN ERROR vs. TEMPERATURE IN OUTPUT VOLTAGE MODE (AOVM)



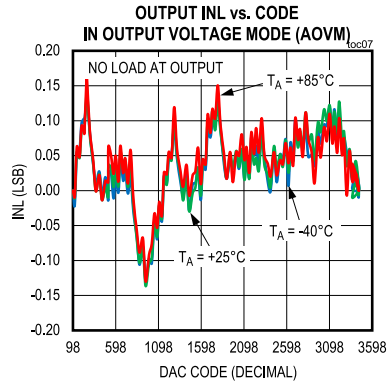
OUTPUT INL vs. CODE IN OUTPUT VOLTAGE MODE (AOVM)



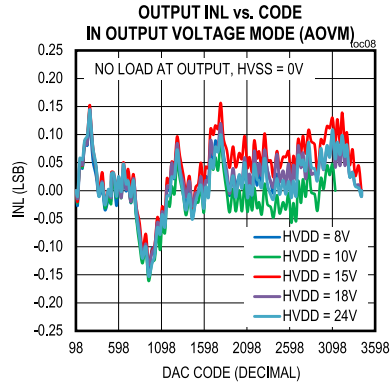
OUTPUT INL vs. CODE IN OUTPUT VOLTAGE MODE (AOVM)



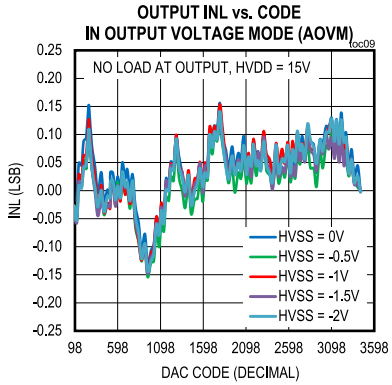
OUTPUT INL vs. CODE IN OUTPUT VOLTAGE MODE (AOVM)



OUTPUT INL vs. CODE IN OUTPUT VOLTAGE MODE (AOVM)



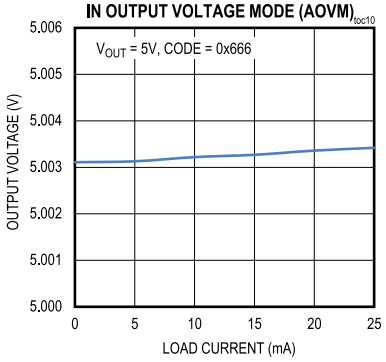
OUTPUT INL vs. CODE IN OUTPUT VOLTAGE MODE (AOVM)



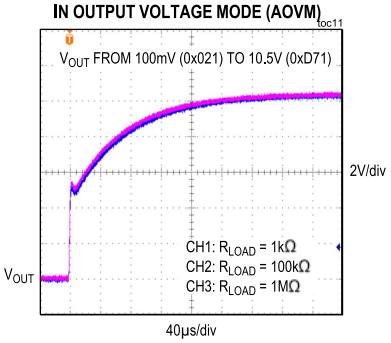
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, V_{HVDD} = +15V, V_{HVSS} = 0V, Internal Reference, T_A = 25°C, unless otherwise noted)

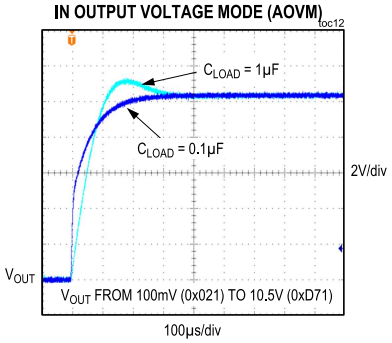
OUTPUT VOLTAGE vs. LOAD CURRENT IN OUTPUT VOLTAGE MODE (AOVM)



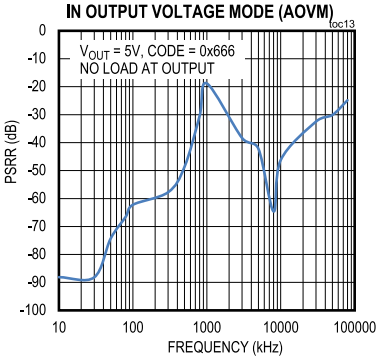
LARGE SIGNAL-STEP RESPONSE IN OUTPUT VOLTAGE MODE (AOVM)



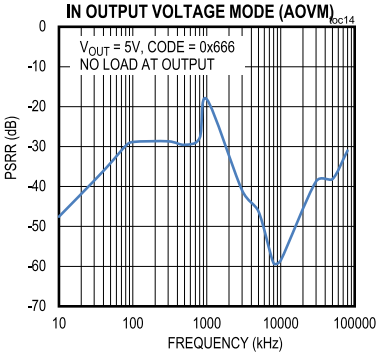
LARGE SIGNAL-STEP RESPONSE IN OUTPUT VOLTAGE MODE (AOVM)



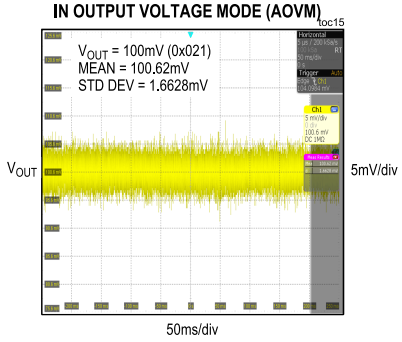
HVDD SUPPLY REJECTION RATIO vs. FREQUENCY IN OUTPUT VOLTAGE MODE (AOVM)



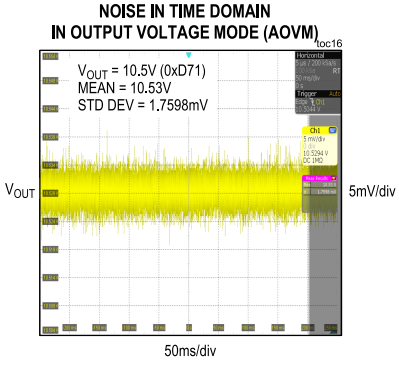
V_{DD} SUPPLY REJECTION RATIO vs. FREQUENCY IN OUTPUT VOLTAGE MODE (AOVM)



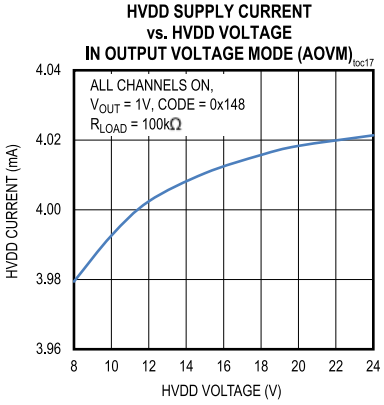
NOISE IN TIME DOMAIN IN OUTPUT VOLTAGE MODE (AOVM)



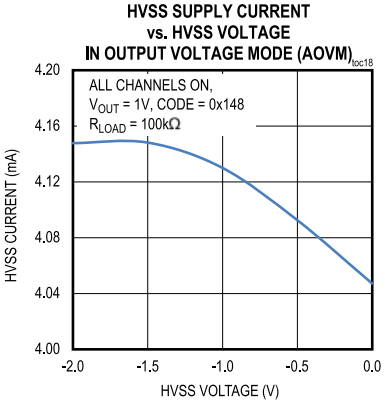
NOISE IN TIME DOMAIN IN OUTPUT VOLTAGE MODE (AOVM)



HVDD SUPPLY CURRENT vs. HVDD VOLTAGE IN OUTPUT VOLTAGE MODE (AOVM)



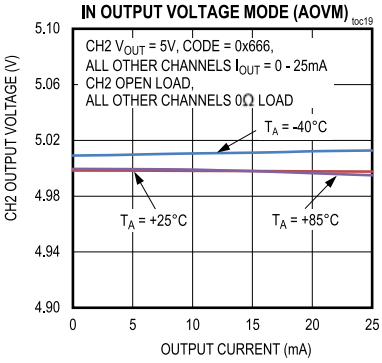
HVSS SUPPLY CURRENT vs. HVSS VOLTAGE IN OUTPUT VOLTAGE MODE (AOVM)



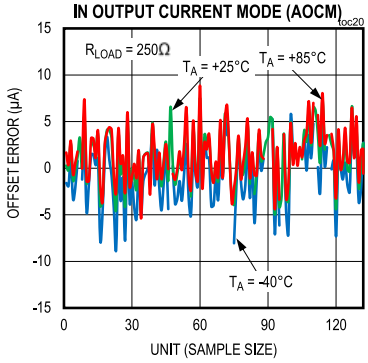
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, V_{HVDD} = +15V, V_{HVSS} = 0V, Internal Reference, T_A = 25°C, unless otherwise noted)

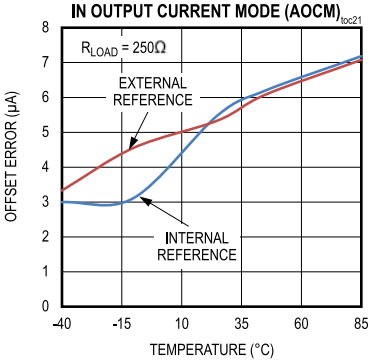
CH2 VOLTAGE vs. OTHER CHANNELS OUTPUT CURRENT IN OUTPUT VOLTAGE MODE (AOVM)



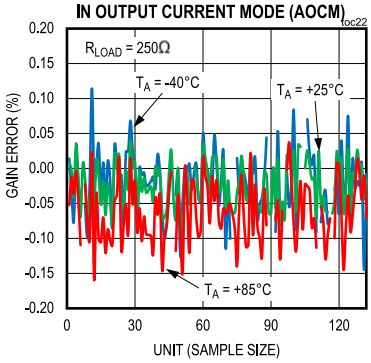
OFFSET-ERROR DISTRIBUTION IN OUTPUT CURRENT MODE (AOCM)



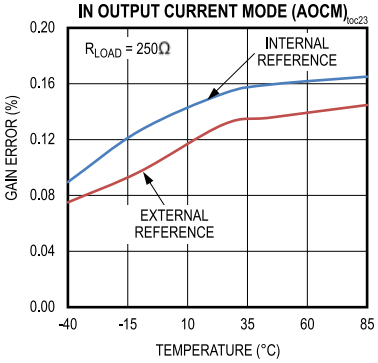
OFFSET ERROR vs. TEMPERATURE IN OUTPUT CURRENT MODE (AOCM)



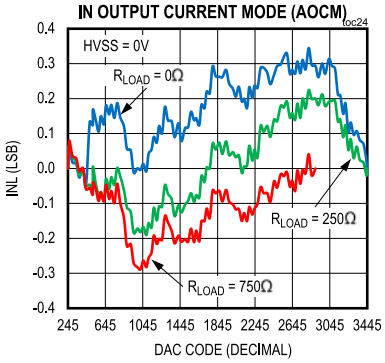
GAIN-ERROR DISTRIBUTION IN OUTPUT CURRENT MODE (AOCM)



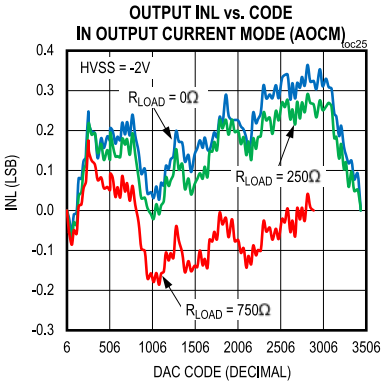
GAIN ERROR vs. TEMPERATURE IN OUTPUT CURRENT MODE (AOCM)



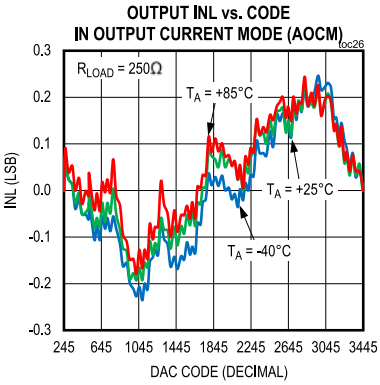
OUTPUT INL vs. CODE IN OUTPUT CURRENT MODE (AOCM)



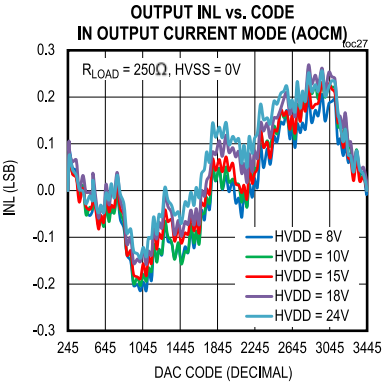
OUTPUT INL vs. CODE IN OUTPUT CURRENT MODE (AOCM)



OUTPUT INL vs. CODE IN OUTPUT CURRENT MODE (AOCM)



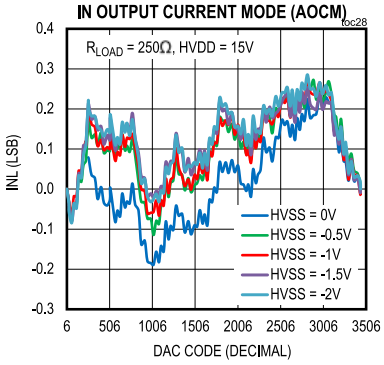
OUTPUT INL vs. CODE IN OUTPUT CURRENT MODE (AOCM)



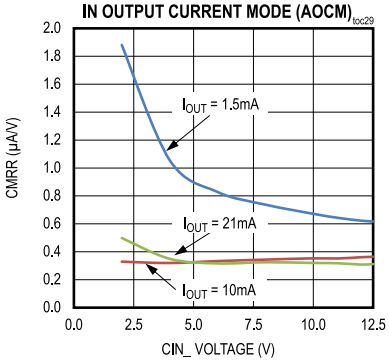
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, V_{HVDD} = +15V, V_{HVSS} = 0V, Internal Reference, T_A = 25°C, unless otherwise noted)

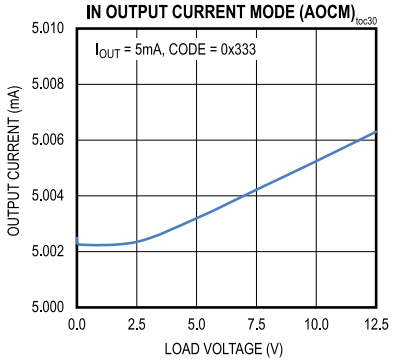
OUTPUT INL vs. CODE
IN OUTPUT CURRENT MODE (AOCM)



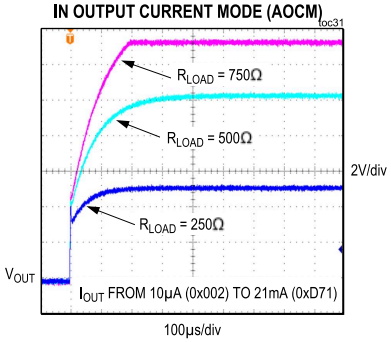
COMMON-MODE REJECTION RATIO
vs. OUTPUT VOLTAGE
IN OUTPUT CURRENT MODE (AOCM)



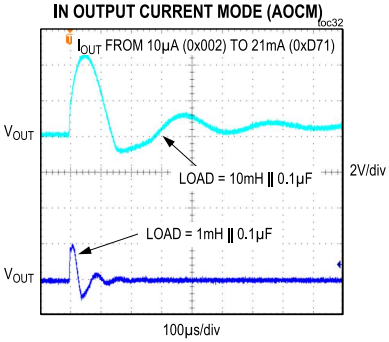
OUTPUT CURRENT vs. LOAD VOLTAGE
IN OUTPUT CURRENT MODE (AOCM)



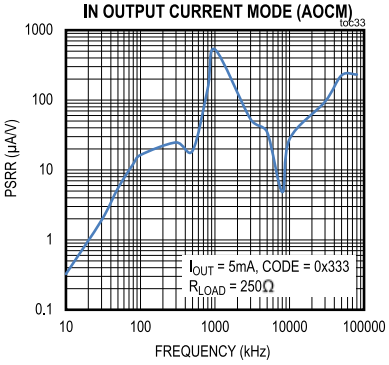
LARGE SIGNAL-STEP RESPONSE
IN OUTPUT CURRENT MODE (AOCM)



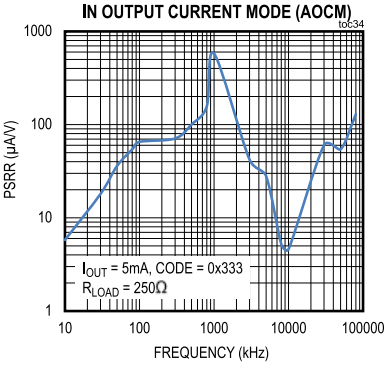
LARGE SIGNAL-STEP RESPONSE
IN OUTPUT CURRENT MODE (AOCM)



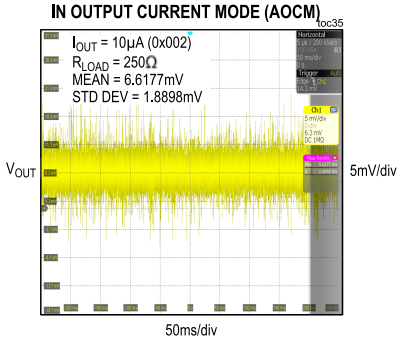
HVDD SUPPLY REJECTION RATIO
vs. FREQUENCY
IN OUTPUT CURRENT MODE (AOCM)



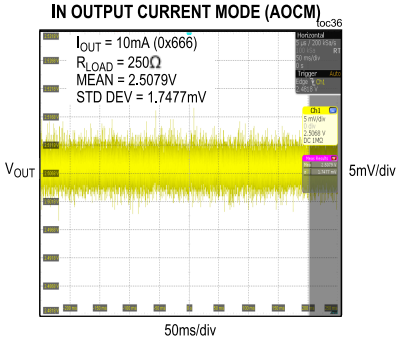
V_{DD} SUPPLY REJECTION RATIO
vs. FREQUENCY
IN OUTPUT CURRENT MODE (AOCM)



NOISE IN TIME DOMAIN
IN OUTPUT CURRENT MODE (AOCM)



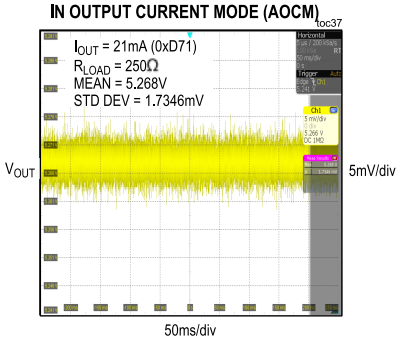
NOISE IN TIME DOMAIN
IN OUTPUT CURRENT MODE (AOCM)



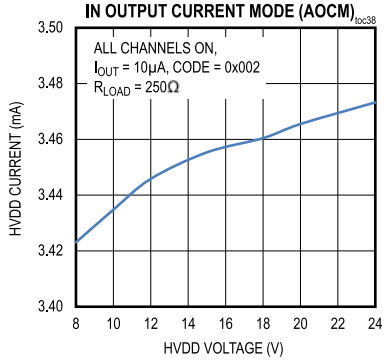
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, V_{HVDD} = +15V, V_{HVSS} = 0V, Internal Reference, T_A = 25°C, unless otherwise noted)

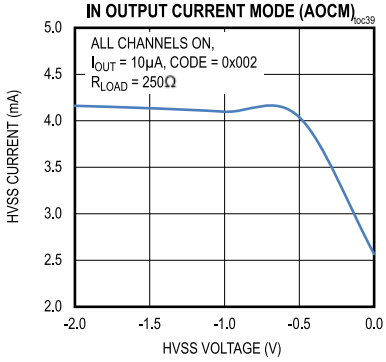
NOISE IN TIME DOMAIN
IN OUTPUT CURRENT MODE (AOCM)



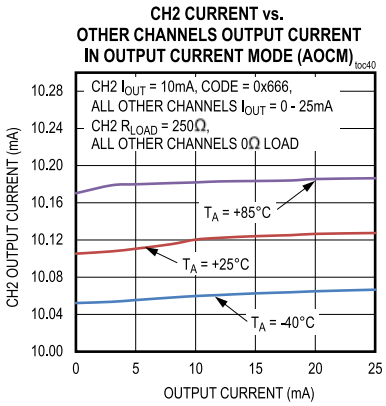
HVDD SUPPLY CURRENT
vs. HVDD VOLTAGE
IN OUTPUT CURRENT MODE (AOCM)



HVSS SUPPLY CURRENT
vs. HVSS VOLTAGE
IN OUTPUT CURRENT MODE (AOCM)

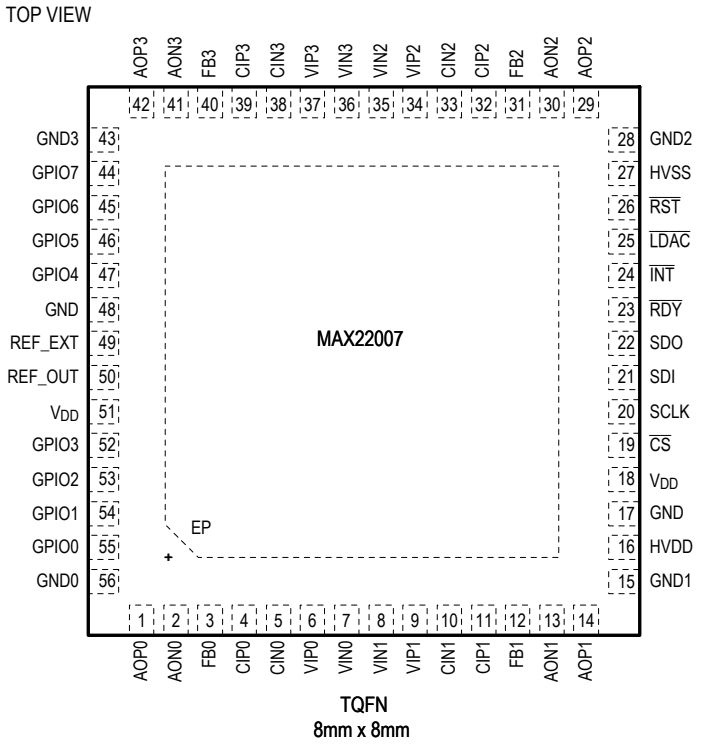


CH2 CURRENT vs.
OTHER CHANNELS OUTPUT CURRENT
IN OUTPUT CURRENT MODE (AOCM)



Pin Configuration

MAX22007



Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
POWER SUPPLY				
16	HVDD	Positive High-Voltage Power Supply from +8V to (HVSS +24V) for the Output Channels. Bypass HVDD to GND with a minimum 1µF ceramic capacitor as close to the device pin as possible.	HVDD	Power
17, 48	GND	Logic/Analog Ground	V_{DD}	Ground
18, 51	V_{DD}	Low-Voltage Power Supply from +2.7V to +5.5V. Connect both V_{DD} pins together and bypass each pin to GND with a minimum 1µF ceramic capacitor as close to the device pin as possible.	V_{DD}	Power
27	HVSS	Negative High-Voltage Power Supply from -2V to 0V for the Output Channels. For most applications connect HVSS to GND (0V), but in cases where the output must be down to 0V (or 0mA), connect HVSS to a -2V supply and in this case, bypass HVSS to GND with a minimum 1µF ceramic capacitor as close to the device pin as possible.	HVDD	Power
EP	EP	Exposed Pad. Connect the exposed pad on the bottom of the package to HVSS. Refer to the *PCB Layout Recommendations* section for layout recommendations.	HVDD	Power
VOLTAGE REFERENCE				
49	REF_EXT	External Reference Voltage Input. Instead of the internal voltage reference, an external precision 2.500V reference can be connected between REF_EXT and GND. The REF_SEL bit in the *Configuration* register must be set appropriately. If an external reference is connected to the REF_EXT pin, bypass it to GND with a minimum 1µF ceramic capacitor as close to the device pin as possible. If the internal reference is selected, tie this pin to GND.	V_{DD}	Input
50	REF_OUT	Voltage Reference Output. The REF_OUT pin can be used to supply multiple devices from the same reference source. If not in use, leave REF_OUT unconnected.	V_{DD}	Output
ANALOG OUTPUT CHANNEL 0				
1	AOP0	Channel 0 Positive Amplifier Output. Connect to the anode of an external diode.	HVDD	Output
2	AON0	Channel 0 Negative Amplifier Output. Connect to the cathode of an external diode.	HVDD	Output
3	FB0	Channel 0 Compensation Network Input. Refer to the *Feedback (FB_) Inputs* section for details.	HVDD	Input
4	CIP0	Channel 0 Positive Current-Sense Input	HVDD	Input
5	CIN0	Channel 0 Negative Current-Sense Input	HVDD	Input
6	VIP0	Channel 0 Positive Voltage-Sense Input	HVDD	Input
7	VIN0	Channel 0 Negative Voltage-Sense Input	HVDD	Input
56	GND0	Channel 0 Ground. Connect GND0 to GND.	HVDD	Ground
ANALOG OUTPUT CHANNEL 1				
14	AOP1	Channel 1 Positive Amplifier Output. Connect to the anode of an external diode.	HVDD	Output

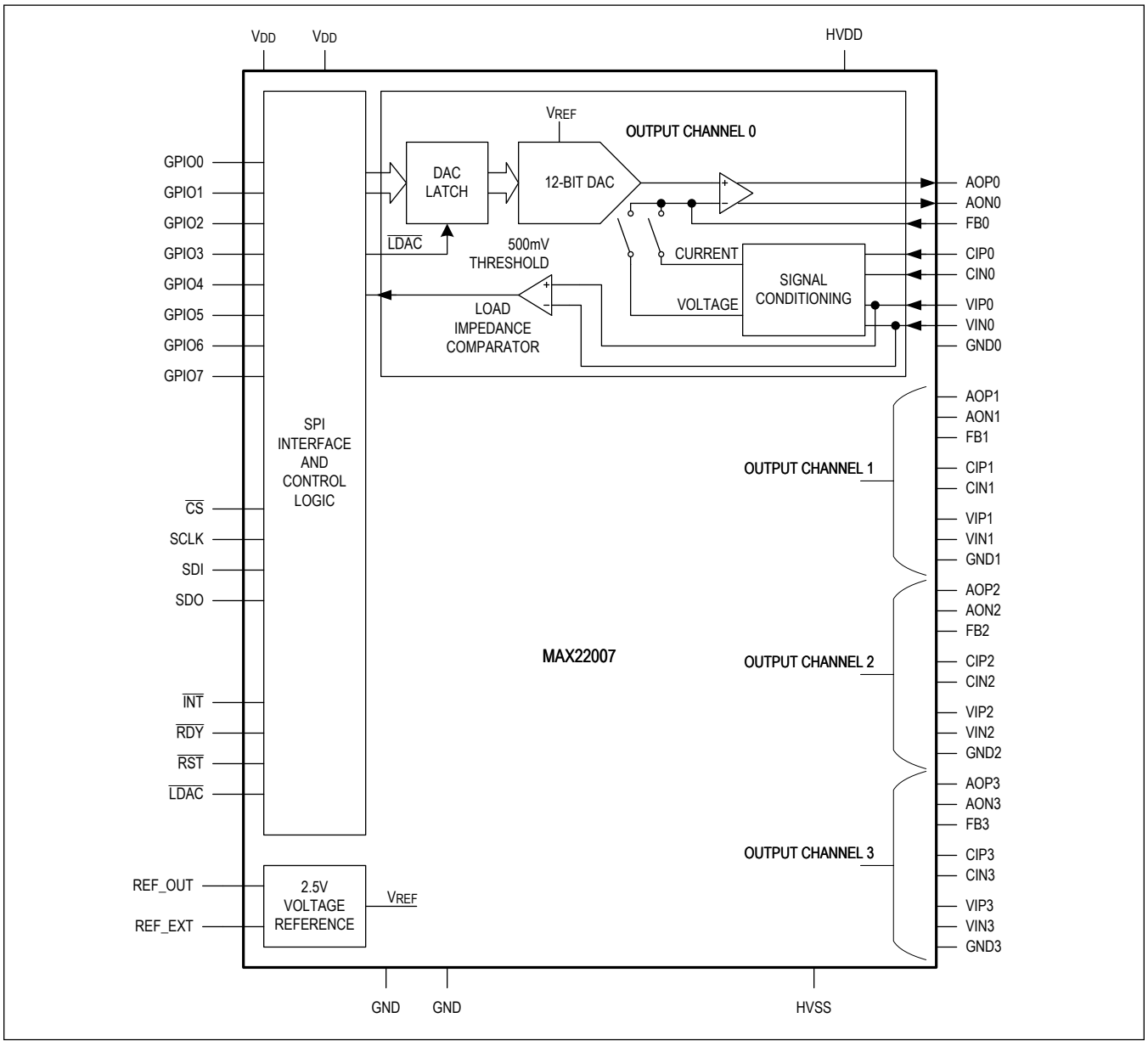
Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
13	AON1	Channel 1 Negative Amplifier Output. Connect to the cathode of an external diode.	HVDD	Output
12	FB1	Channel 1 Compensation Network Input. Refer to the *Feedback (FB_) Inputs* section for details.	HVDD	Input
11	CIP1	Channel 1 Positive Current-Sense Input	HVDD	Input
10	CIN1	Channel 1 Negative Current-Sense Input	HVDD	Input
9	VIP1	Channel 1 Positive Voltage-Sense Input	HVDD	Input
8	VIN1	Channel 1 Negative Voltage-Sense Input	HVDD	Input
15	GND1	Channel 1 Ground. Connect GND1 to GND.	HVDD	Ground
ANALOG OUTPUT CHANNEL 2				
29	AOP2	Channel 2 Positive Amplifier Output. Connect to the anode of an external diode.	HVDD	Output
30	AON2	Channel 2 Negative Amplifier Output. Connect to the cathode of an external diode.	HVDD	Output
31	FB2	Channel 2 Compensation Network Input. Refer to the *Feedback (FB_) Inputs* section for details.	HVDD	Input
32	CIP2	Channel 2 Positive Current-Sense Input	HVDD	Input
33	CIN2	Channel 2 Negative Current-Sense Input	HVDD	Input
34	VIP2	Channel 2 Positive Voltage-Sense Input	HVDD	Input
35	VIN2	Channel 2 Negative Voltage-Sense Input	HVDD	Input
28	GND2	Channel 2 Ground. Connect GND2 to GND.	HVDD	Ground
ANALOG OUTPUT CHANNEL 3				
42	AOP3	Channel 3 Positive Amplifier Output. Connect to the anode of an external diode.	HVDD	Output
41	AON3	Channel 3 Negative Amplifier Output. Connect to the cathode of an external diode.	HVDD	Output
40	FB3	Channel 3 Compensation Network Input. Refer to the *Feedback (FB_) Inputs* section for details.	HVDD	Input
39	CIP3	Channel 3 Positive Current-Sense Input	HVDD	Input
38	CIN3	Channel 3 Negative Current-Sense Input	HVDD	Input
37	VIP3	Channel 3 Positive Voltage-Sense Input	HVDD	Input
36	VIN3	Channel 3 Negative Voltage-Sense Input	HVDD	Input
43	GND3	Channel 3 Ground. Connect GND3 to GND.	HVDD	Ground
LOGIC INTERFACE				
19	$\overline{CS}$	Active-Low Chip Select Input from Controller. The SPI interface responds only when $\overline{CS}$ is low.	V_{DD}	Input
20	SCLK	Serial Clock Input from Controller	V_{DD}	Input
21	SDI	Serial Data Input. SPI MOSI data input from controller.	V_{DD}	Input
22	SDO	Serial Data Output. SPI MISO data output to controller.	V_{DD}	Output

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
23	$\overline{RDY}$	Active-Low Ready Output. $\overline{RDY}$ is asserted low after the last SCLK falling edge of an SPI transaction and is used to drive the $\overline{CS}$ input of the next MAX22007 when used for daisy-chain applications. If the MAX22007 is not used in daisy-chain mode, or is the last device in the daisy chain, $\overline{RDY}$ can be left unconnected.	V_{DD}	Output
24	$\overline{INT}$	Active-Low Open-Drain Interrupt Output. $\overline{INT}$ is asserted low when any interrupt source is detected and flagged in the *Status & Interrupts* register, provided that interrupt source has been enabled by setting the corresponding bit in the *Interrupt Enable* register. Connect a pullup resistor from $\overline{INT}$ to V_{DD}.	V_{DD}	Output
25	$\overline{LDAC}$	Active-Low DAC Load Input. When asserted low, transfers the contents of the DAC Channel Data registers and updates all the DAC outputs simultaneously. $\overline{LDAC}$ is ignored whilst $\overline{RST}$ is low. Connect to V_{DD} if not used.	V_{DD}	Input
26	$\overline{RST}$	Active-Low Reset Input. When asserted low, reconfigures all registers to their power-on default states, analog outputs go high impedance, and DAC conversions stop.	V_{DD}	Input
55	GPIO0	General Purpose Digital Input/Output 0	V_{DD}	I/O
54	GPIO1	General Purpose Digital Input/Output 1	V_{DD}	I/O
53	GPIO2	General Purpose Digital Input/Output 2	V_{DD}	I/O
52	GPIO3	General Purpose Digital Input/Output 3	V_{DD}	I/O
47	GPIO4	General Purpose Digital Input/Output 4	V_{DD}	I/O
46	GPIO5	General Purpose Digital Input/Output 5	V_{DD}	I/O
45	GPIO6	General Purpose Digital Input/Output 6	V_{DD}	I/O
44	GPIO7	General Purpose Digital Input/Output 7	V_{DD}	I/O

Functional Diagrams



Note: Only one channel is shown for clarity.

Detailed Description

The MAX22007 is a software-configurable four-channel analog output device that drives a voltage or current output on each channel. All outputs are protected to ±42V_{P-P} for high-voltage supply of HVDD = 8V to 20V and HVSS = -2V to 0V.

Each output channel of the MAX22007 features a 12-bit DAC with fast settling time using a shared internal voltage reference.

The MAX22007 offers low-offset high-voltage amplifiers to condition the signal from low-voltage DAC outputs to high-voltage or current outputs. If one output is miswired, all other outputs remain unaffected and function normally. An internal comparator can be used to determine the load impedance and allows the microcontroller to intelligently select for voltage- or current-output mode. All outputs are kept safe by integrated current protection for functional and thermal robustness. The MAX22007 also includes a thermal shutdown circuit that protects the device when the junction temperature exceeds 165°C (typ).

The MAX22007 communicates to a microcontroller using an SPI interface at clock rates up to 30MHz with an optional eight-bit CRC for improved data integrity. Eight GPIOs can be used to interface and control other resources on the circuit board. The MAX22007 operates from a 2.7V to 5.5V low-voltage supply, a +8V to +24V high-voltage positive supply, and a -2V to 0V high-voltage negative supply. The MAX22007 is available in an 8mm x 8mm 56-pin TQFN package and operates over the -40°C to +85°C temperature range with ±2.5kV HBM ESD protection on all pins.

DAC

Each output channel features a separate low-power 12-bit DAC. The input value for each DAC is held in the corresponding Channel Data register. Each output channel uses a DAC latch between the Channel Data register and the DAC that contains the digital representation of the value that is currently presented at the channel output. The default configuration is to use the latch but it can be configured for transparent mode by setting the bits LD_CNFG[3:0] in the *Configuration* register to 1. When LD_CNFG[3:0] bits are set to 0, the operation of the latch is controlled by making the hardware pin $\overline{LDAC}$ active low, or by setting LD_CTRL[3:0] bits in the *Control* register using a SPI write operation. The LD_CTRL[3:0] bits are self-clearing.

The MAX22007 offers several options to update the DAC output to accommodate different application requirements as shown in Figure 4. In order for any of the analog outputs to change value, the values contained in the Channel Data registers need to be transferred to the DAC latch output. In transparent latch mode (LD_CNFG[3:0] bits = 1), a write to the Channel Data register automatically updates the channel output value. In latch mode, a write transaction to one or all of the Channel Data registers does not necessarily change the channel output value. The options of controlling the $\overline{LDAC}$ pin or setting the LD_CTRL[3:0] bits allow for individual or simultaneous update of the channel output values, and to be able to control the exact timing of the update. Using the $\overline{LDAC}$ pin over an SPI transaction to update the DAC latches has the advantage that the exact timing of the update can be controlled.

If no tight control of the output update timing is required, the step of loading the DAC latch can be eliminated by setting bits LD_CNFG[3:0] in the *Configuration* register to 1 (transparent mode) and if one of the LD_CNFG[x] bits is set for a certain channel, then writing to the Channel x Data register immediately updates the analog output value, bypassing the DAC latch altogether. Alternatively, if the $\overline{LDAC}$ pin is tied to ground, the DAC latch automatically updates the DAC with the Channel Data register values.

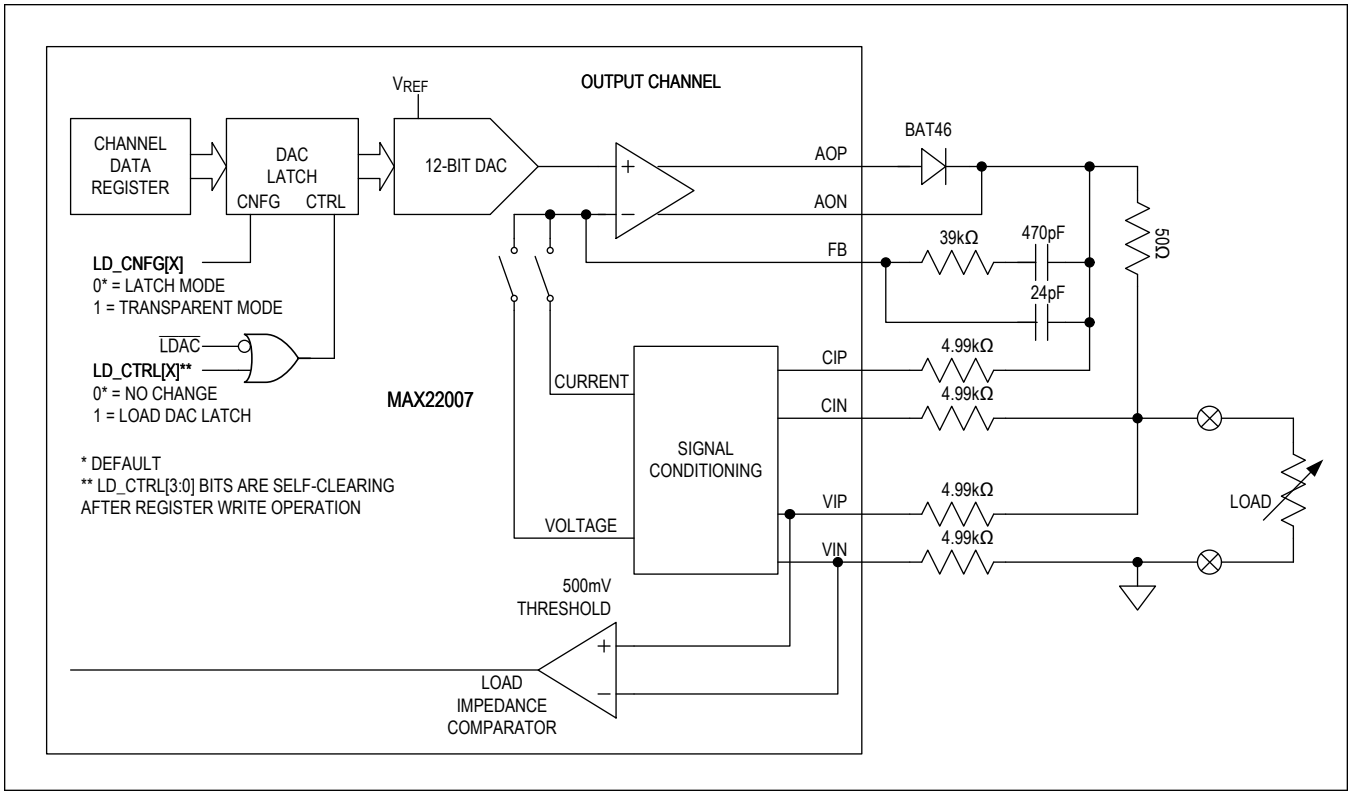


Figure 4. MAX22007 Output Channel

High-Voltage Analog Output

The MAX22007 offers the following modes of operation:

- Analog Output-Voltage Mode (AOVM)
- Analog Output-Current Mode (AOCM)

The nominal output voltage range in AOVM is 0V to +10V, while linearity is guaranteed up to +10.5V. The DAC full-scale range is 0V to +12.5V to offer 25% overrange of the nominal output voltage range. In AOVM, the load voltage is sensed through the VIP_ and VIN_ inputs.

The ideal output voltage is given as:

$$V_{OUT} = 5 \times V_{REF} \times \frac{D}{2^N}$$

where,

D = Input code in the Channel x Data register

V_{REF} = Reference voltage

N = Resolution of the DAC (N = 12)

The MAX22007 is factory calibrated using the internal reference. The full-scale range in AOVM is calibrated to 12.5V based on the internal reference; thus, $V_{OUT} = 12.5 \times \frac{D}{2^N}$. When using the external reference, V_{REF} in the equation is the external reference voltage.

The nominal output current range in AOCM is 0mA to +20mA, while linearity is guaranteed up to +21mA. The DAC full-scale range is 0mA to +25mA to offer 25% overrange of the nominal output current range. In AOCM, the load current is sensed through the CIP_ and CIN_ inputs using an external 50Ω resistor. A value of 50Ω is required to produce the correct output-current range.

The ideal output current is given as:

$$I_{OUT} = \frac{V_{REF}}{2 \times R_{SENSE}} \times \frac{D}{2^N}$$

where,

D = Input code in the Channel x Data register

V_{REF} = Reference voltage

R_{SENSE} = External 50Ω sense resistor

N = Resolution of the DAC (N = 12)

The MAX22007 is factory calibrated using the internal reference and an ideal 50Ω sense resistor. The full-scale range in AOCM is calibrated to 25mA based on the external sense resistor; thus, $I_{OUT} = \frac{1.25}{R_{SENSE}} \times \frac{D}{2^N}$. The accuracy and temperature coefficient of the sense resistor contributes to the output accuracy. When using the external reference, V_{REF} in the equation is the external reference voltage.

Two-, Three-, and Four-Wire Operation

The MAX22007 can operate in two-wire, three-wire, or four-wire configurations, depending on the external connection of the CIN_, VIP_, and VIN_ pins. Refer to the *Typical Application Circuits* section for examples of two-wire and four-wire applications.

Feedback (FB_) Inputs

The MAX22007 offers a feedback input pin (FB_) per channel that allows access to the inverting input of the output amplifier to add an external compensation network as shown in the *Typical Application Circuits*. The type of network and component values depend on the output load requirements. A recommended compensation network that offers stable amplifier performance over a wide range of resistive and capacitive loads for output voltage mode and a wide range of resistive and inductive loads for output current mode is shown in the *Typical Application Circuits*.

Comparator

The MAX22007 offers a comparator that monitors the output voltage through VIP_ and VIN_ per channel and sets a bit in the *Status & Interrupts* register if the output voltage exceeds a threshold of 500mV (typical). This comparator can be used to determine the load impedance to automatically detect whether a connected load requires output current mode or output voltage mode.

In order to determine the load impedance, set the output in question to output current mode. Increase the output current until the comparator trips, and the COMP_INT[x] bit is set in the *Status & Interrupts* register. The load impedance is then simply the comparator threshold voltage of 500mV divided by the programmed output current.

The two bits COMP_EDGE_CNFG[1:0] in the *Configuration* register can be programmed to select different operating modes for the comparators, which in turn trigger the COMP_INT[3:0] bits and assert the $\overline{INT}$ pin if enabled. This setting applies to all output channels. Programming COMP_EDGE_CNFG[1:0] to be 0b01 detects a rising edge at the comparator output, 0b10 detects a falling edge at the comparator output, and 0b11 shows the comparator output level, either a 0 or a 1, using the COMP_INT[3:0] bits.

Input and Output Protection

The AOP_ and AON_ outputs feature devices with a maximum operating voltage of 65V. The outputs can therefore tolerate $\pm 42V_{P-P}$ for a high-voltage supply HVDD up to +20V. The AOP_ output uses an external small-signal diode. This series protection limits the current flowing into the MAX22007 to very small amounts in the µA-range in case the output

voltage is pulled above HVDD. A suitable external diode is BAT46. If the output is pulled below HVSS, an internal diode prevents any large current from flowing.

The protection of the FB_, CIP_, CIN_, VIP_, and VIN_ inputs includes an external series resistor with a recommended value of 4.99kΩ. As long as the HVDD and HVSS supply voltages are actively driven, the voltages at these inputs remain within approximately 0.7V of HVDD or HVSS, irrespective of the actual external input voltage.

If an external DC-DC converter supplying HVDD malfunctions and is no longer capable of sinking or sourcing current, then the resistive feedback network around the DC-DC converter can be used to effectively protect the input pins of the MAX22007 as shown in Figure 5. To protect the MAX22007 in this failure mode, the total resistance R_{PATH} of the feedback network of the DC-DC converter should be chosen as 30kΩ to limit the voltage at the input pins to a safe value of 36V.

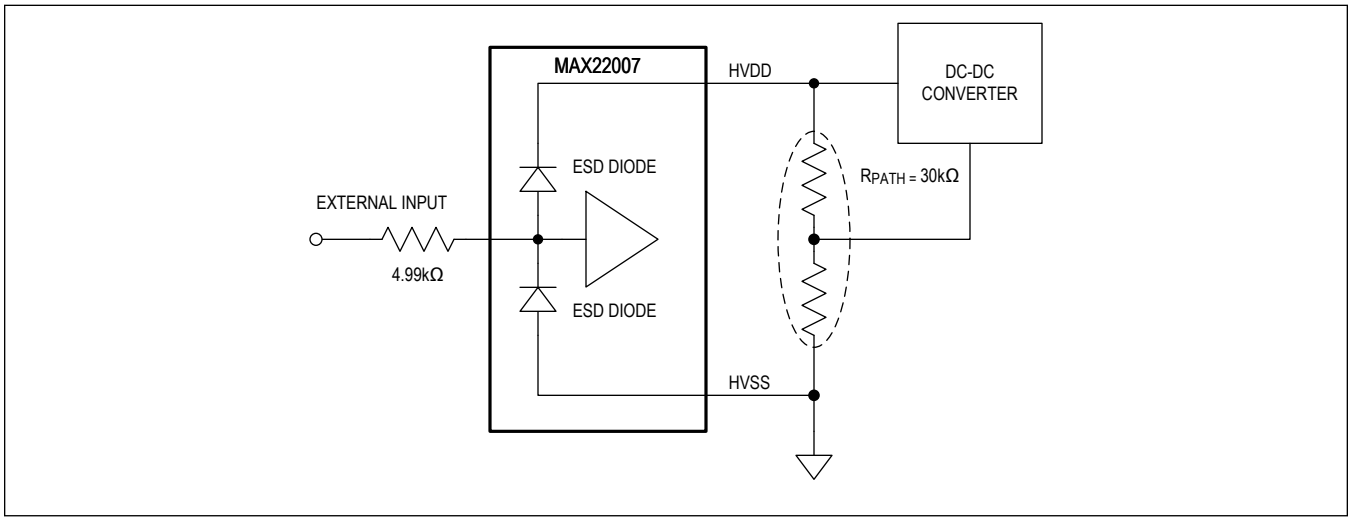


Figure 5. Input Protection of the MAX22007 In Case of External DC-DC Converter Failure

Output Correction

To ease system calibration, reduce system test cost, and improve long-term system accuracy, all MAX22007 ICs are factory calibrated during final test for gain and offset adjustment. This output correction is applicable when operating in analog output-voltage mode (AOVM) or analog output-current mode (AOCM). The analog output is accurate to ±0.2% at room temperature and to ±1% over the full operating temperature range.

Internal and External Reference

The MAX22007 includes an internal precision 2.500V reference with ±10ppm/°C (typ) performance. Instead of the internal reference, an external 2.500V reference can be connected between REF_EXT and GND. The typical input impedance of the REF_EXT input is 100kΩ.

The REF_SEL bit in the *Configuration* register is used to select between the internal reference and an external reference. At power-up, the internal reference is selected. The output voltage of the internal reference is available at the REF_OUT pin, independent of the value of the REF_SEL bit. The REF_OUT pin is not designed to drive large capacitive loads and is provided to allow sharing of one internal voltage reference among multiple devices. REF_OUT should be left unconnected if not used. If an external reference is selected and connected to the REF_EXT pin, bypass it with a 1µF capacitor as close to the pin as possible. Otherwise, if the internal reference is selected, tie the REF_EXT pin to GND. The MAX22007 is factory calibrated using the internal reference. The Electrical Characteristics are tested and guaranteed to the internal reference (see the *Electrical Characteristics* section). An external reference can provide better thermal performance; however, the factory calibration cannot be guaranteed.

Short-Circuit Protection

When operating in analog output-voltage mode (AOVM), the analog output is constantly monitored for overcurrent conditions. Two modes of operation can be selected by the OVC_CNFG bit in the *Configuration* register. In automatic mode, the output amplifier is powered down after an excessive output current is detected, and powers up approximately every 8ms for 400µs while the overcurrent condition exists. Once the overcurrent condition is resolved, the output amplifier remains in power-up mode. In host-controlled mode, the output amplifier is powered down after an excessive output current is detected, and the corresponding CHNL_PWR[x] bit in the *Channel Mode* register is reset. The host is then responsible to rewrite the CHNL_PWR[x] bit to enable the corresponding output channel.

In both cases, the interrupt bit OVC_INT[x] in the *Status & Interrupts* register is set to logic high to indicate the overcurrent condition. In automatic mode, bit OVC_INT[x] is automatically cleared once the overcurrent condition is resolved.

To allow capacitive loads to be charged up quickly, once an overcurrent condition is detected, the MAX22007 waits for approximately 400µs before the output amplifiers are powered down. This time window is sufficient to charge a completely discharged capacitive load of 1µF from 0V to +10V or vice versa without interrupting normal operation.

When the MAX22007 operates in analog output-current mode (AOCM), the short-circuit protection is disabled.

Thermal Monitoring and Shutdown

The die temperature of the MAX22007 is constantly monitored. If the die temperature reaches 145°C (typical), the THWRNG_INT bit in the *Status & Interrupts* register is set to logic high, and an interrupt is issued if bit THWRNG_INTEN in the *Interrupt Enable* register is set to logic high. If the die temperature falls below 135°C (typical), bit THWRNG_INT in the *Status & Interrupts* register is automatically cleared.

If the die temperature exceeds 165°C (typical), the THSHDN_INT bit in the *Status & Interrupts* register is set to logic high, and the MAX22007 is shut down by powering down all amplifiers. The CHNL_PWR[3:0] settings in the *Channel Mode* register are reset to their power-up values. Under this condition, an interrupt is always issued, i.e., the $\overline{INT}$ pin is pulled low.

In order to allow the voltage reference to power up and not produce false thermal shutdown and thermal warning interrupts, the thermal monitoring system is blocked from operation for the first 100ms after a power-on reset.

SPI Interface

The MAX22007 features an SPI interface with clock speed up to 30MHz. An eight-bit cyclic redundancy check (CRC) is offered to improve the SPI data integrity in harsh environments. CRC checking can be enabled and disabled by setting the CRC_EN bit in the *Configuration* register. The default condition for CRC_EN bit is 1, meaning the CRC is enabled by default. The SPI transactions are 32-bits long if CRC is enabled as shown in Table 1.

Table 1. SPI Transaction with CRC Enabled

BITS 31:25	BIT 24	BITS 23:8	BITS 7:0
Register Address	R/$\overline{W}$	16-bit Payload	CRC

If CRC is disabled, the SPI transactions are 24-bits long as shown in Table 2.

Table 2. SPI Transaction with CRC Disabled

BITS 23:17	BIT 16	BITS 15:0
Register Address	R/$\overline{W}$	16-bit Payload

The MAX22007 implements the CRC-8/MAXIM algorithm with a 0x31 polynomial ($x^8 + x^5 + x^4 + x^0$), the same polynomial that is used in Maxim's 1-wire® products. This CRC algorithm uses reflected input and output bytes (i.e., LSB first instead of MSB first on a byte basis; the byte order of the input sequence is not changed). The initial value is 0x00, and the output is reported as is without any XOR operation. This CRC can detect the following types of errors:

- Any odd number of errors anywhere within the 32-bit number
- All double-bit errors anywhere within the 32-bit number
- Any cluster of errors that can be contained within an 8-bit window (1-8 bits incorrect)
- Most large clusters of errors

For write transactions, the CRC is calculated on the 24 bits that precede it, namely the 7-bit register address, the 1-bit read or write control, and the 16-bit payload. Here are two examples of write operations:

- Write 0xF000 to the *Interrupt Enable* register: 0x04F0_0007
- Write 0x53FA to the *Channel 1 Data* register: 0x1053_FA62

For read transactions, the CRC sent back to the host by the MAX22007 is calculated on the 24 bits comprised of the 8-bit header received from the host (register address and read control) and the 16 bits of payload. Here are two examples of read operations:

- Read the default value from the *Configuration* register: 0x0700_007A
- Read the default value from the *Channel Mode* register: 0x0B00_00C1

Refer to AN27 for more details at: *https://www.maximintegrated.com/en/app-notes/index.mvp/id/27*.

SPI Timeout

The MAX22007 offers timeout detection that monitors the SPI interface for transactions. In particular, the MAX22007 expects to see a properly formatted SPI transaction during the timeout interval. A properly formatted SPI transaction requires a falling edge of $\overline{CS}$, at least 24 SCLK cycles if CRC is disabled, or at least 32 SCLK cycles if CRC is enabled, and a rising edge of $\overline{CS}$. A valid CRC code is not required for an SPI transaction to be considered properly formatted. The timeout interval starts with the completion of every properly formatted SPI transaction and can be selected to last from 100ms to 1.6s (typical values) using the TMOUT_SEL[3:0] bits in the *Configuration* register. If no additional completion of a properly formatted SPI transaction is detected during the timeout interval, the TMOUT_INT bit in the *Status & Interrupts* register is set. If the TMOUT_CNFG bit in the *Configuration* register is set, in addition to setting the TMOUT_INT bit, all registers are reset to their power-on default values, except for the TMOUT_INT interrupt bit, the TMOUT_INTEN bit of the *Interrupt Enable* register, and the CRC_EN and REF_SEL bit settings in the *Configuration* register.

Timeout detection is disabled by default and must be enabled by setting the TMOUT_EN bit in the *Configuration* register. The first timeout interval starts at the completion of the SPI transaction that enables TMOUT_EN.

The timeout interval accuracy is ±50% with respect to the nominal value that is selected using the TMOUT_SEL[3:0] bits in the *Configuration* register.

SPI Daisy-Chain Operation

The MAX22007 offers an elongated programming operation that is typically used for devices in daisy-chain applications. The $\overline{RDY}$ output of the MAX22007 feeds the $\overline{CS}$ input of the next device in the daisy-chain as shown in Figure 6.

The MAX22007 pulls the $\overline{RDY}$ output low on the 24^{th} or 32^{nd} SCLK falling edge, depending on whether CRC is enabled or not, allowing the next device in the chain to begin its SPI operation, commencing with the 25^{th} or 33^{rd} SCLK falling edge, respectively. The timing for the SPI signals and the three chip select signals is shown in Figure 7.

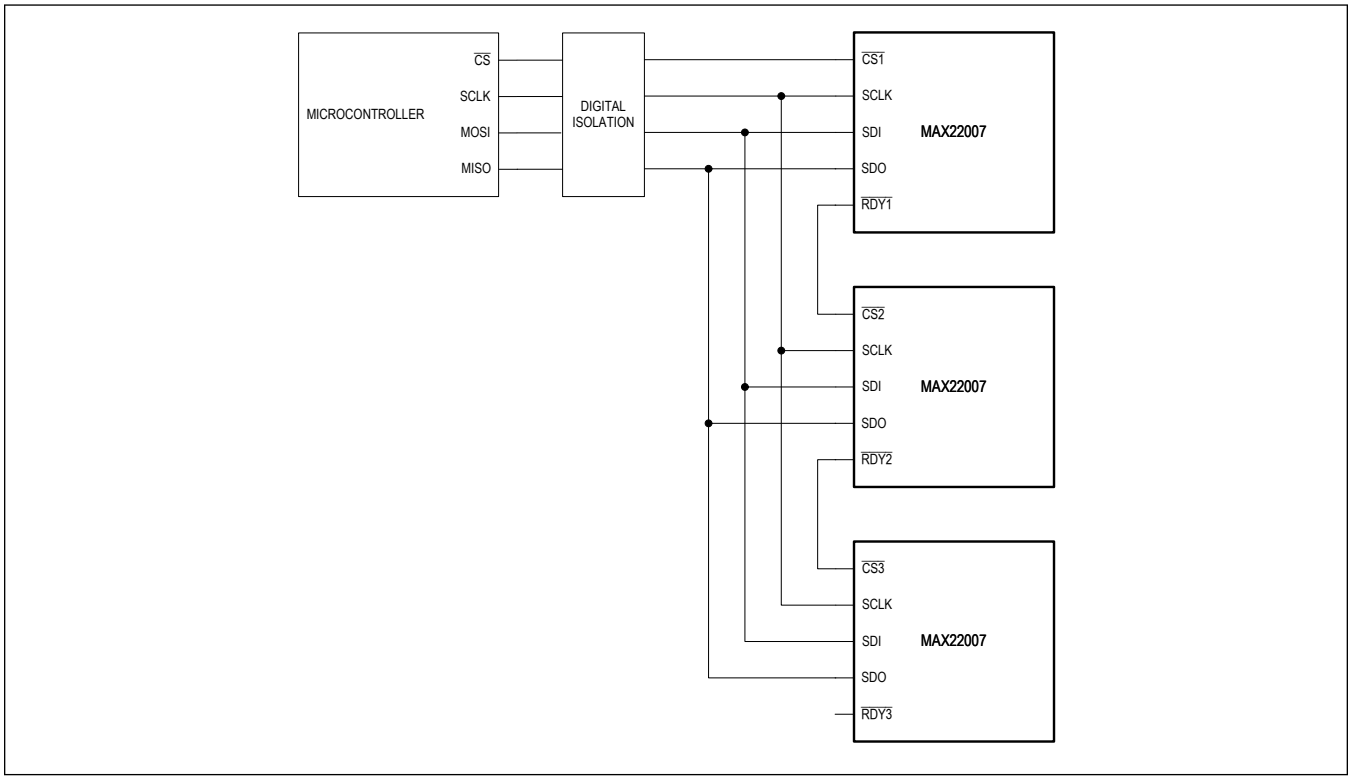


Figure 6. Daisy-Chain Operation

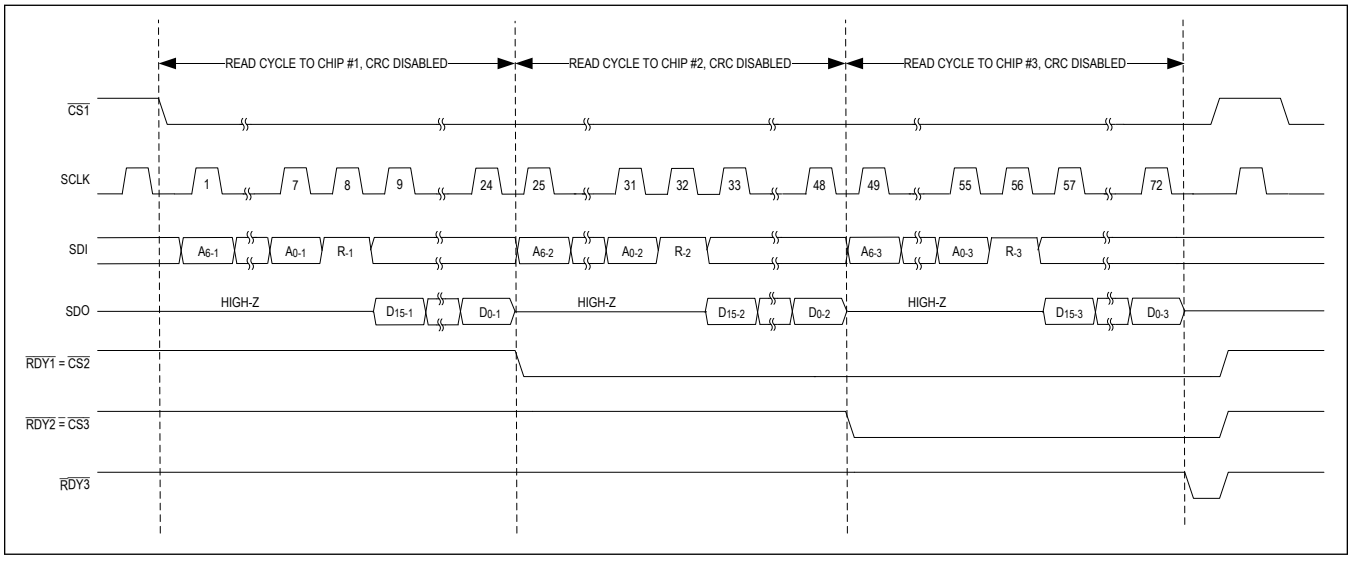


Figure 7. Daisy-Chain SPI Write Diagram

Load DAC ($\overline{LDAC}$) Input

The MAX22007 features an active-low $\overline{LDAC}$ logic input that allows the channels to update asynchronously. $\overline{LDAC}$ should be kept high or connected to V_{DD} when the device is controlled only through the SPI interface. A high-to-low transition of $\overline{LDAC}$ simultaneously updates the channel outputs with data from the Channel x Data registers. If $\overline{LDAC}$ is held low, the contents of the Channel x Data registers are passed through to the DAC immediately, updating the channel outputs.

The LD_CNFG[3:0] bits in the *Configuration* register are used to configure the $\overline{LDAC}$ operation for each channel, independently. When LD_CNFG[x] is set to 1 (transparent mode), writing to the Channel x Data register immediately updates the DAC output value, regardless of the $\overline{LDAC}$ logic level. When LD_CNFG[x] is set to 0, the DAC output is updated at the $\overline{LDAC}$ falling edge with the current content of the Channel x Data register.

Power-On Reset

The low-voltage V_{DD} supply is monitored by power-on reset circuitry. The MAX22007 is held in a reset state until the V_{DD} supply has reached a certain threshold that allows safe operation without loss of data. Once this threshold is exceeded, the SPI interface and low-voltage circuitry is fully functional. The high-voltage supplies (HVDD and HVSS) are also constantly monitored. The loss of the high-voltage supply is indicated by the HVDD_INT bit in the *Status & Interrupts register*. The HVDD_INT bit is set when the voltage difference between HVDD and HVSS is approximately 1.5V.

Software Reset

A software reset can be accomplished by writing to the SW_CLR or SW_RST bit in the *Soft Reset* register. Both bits have a default state of 0 for normal operating condition. Writing a 1 to the SW_RST bit resets all registers except the CRC_EN and REF_SEL bits in the *Configuration* register. Writing a 1 to SW_CLR bit resets only the Channel x Data registers and the DAC latches. Both bits are self-clearing.

Hardware Reset ($\overline{RST}$)

The MAX22007 features an asynchronous active-low $\overline{RST}$ logic input that resets the MAX22007 to power-on reset conditions. Driving $\overline{RST}$ low also aborts any on-going SPI transaction. To allow a new SPI transaction, $\overline{RST}$ must be driven high.

Product Tracking

The MAX22007 includes a 16-bit device tracking number, unique to each device revision manufactured, accessible through the SPI interface. This features enables tracking individual IC revisions. Refer to the *Revision ID* register for details.

Register Map

Registers

ADDRESS	RESET	NAME	MSB							LSB
Revision										
0x00	0xBB45	Revision ID[15:8]	PART_ID[7:0]							
		Revision ID[7:0]	REV_ID[7:0]							
Interrupts										
0x01	0x0000	Status & Interrupts[15:8]	COMP_INT[3:0]				OVC_INT[3:0]			
		Status & Interrupts[7:0]	Reserved[1:0]		THSHDN_INT	THWRNG_INT	HVDD_INT	TMOUT_INT	GPI_INT	CRC_INT
0x02	0x0000	Interrupt Enable[15:8]	COMP_INTEN[3:0]				OVC_INTEN[3:0]			
		Interrupt Enable[7:0]	Reserved[2:0]			THWRNG_INTEN	HVDD_INTEN	TMOUT_INTEN	GPI_INTEN	CRC_INTEN
General Controls										
0x03	0x0001	Configuration[15:8]	LD_CNFG[3:0]				COMP_EDGE_CNFG[1:0]		Reserved	REF_SEL
		Configuration[7:0]	TMOUT_SEL[3:0]				TMOUT_CNFG	TMOUT_EN	OVC_CNFG	CRC_EN
0x04	0x0000	Control[15:8]	LD_CTRL[3:0]				Reserved[3:0]			
		Control[7:0]	Reserved[7:0]							
0x05	0x0000	Channel Mode[15:8]	CHNL_MODE[3:0]				CHNL_PWR[3:0]			
		Channel Mode[7:0]	Reserved[7:0]							
0x06	0x0000	Soft Reset[15:8]	Reserved[2:0]			SW_CLR	Reserved[2:0]			SW_RST
		Soft Reset[7:0]	Reserved[7:0]							
DAC Data										
0x07	0x0000	Channel 0 Data[15:8]	DATA_CH_0[11:4]							
		Channel 0 Data[7:0]	DATA_CH_0[3:0]				Reserved[3:0]			
0x08	0x0000	Channel 1 Data[15:8]	DATA_CH_1[11:4]							
		Channel 1 Data[7:0]	DATA_CH_1[3:0]				Reserved[3:0]			
0x09	0x0000	Channel 2 Data[15:8]	DATA_CH_2[11:4]							

ADDRESS	RESET	NAME	MSB							LSB
		Channel 2 Data[7:0]	DATA_CH_2[3:0]				Reserved[3:0]			
0x0A	0x0000	Channel 3 Data[15:8]	DATA_CH_3[11:4]							
		Channel 3 Data[7:0]	DATA_CH_3[3:0]				Reserved[3:0]			
GPIO Ports										
0x0B	0x0000	GPIO Control[15:8]	GPIO_EN[7:0]							
		GPIO Control[7:0]	GPIO_DIR[7:0]							
0x0C	0x0000	GPIO Data[15:8]	GPO_DATA[7:0]							
		GPIO Data[7:0]	GPI_DATA[7:0]							
0x0D	0x0000	GPI Edge Detection Control[15:8]	GPI_POS_EDGE_INT[7:0]							
		GPI Edge Detection Control[7:0]	GPI_NEG_EDGE_INT[7:0]							
0x0E	0x0000	GPI Edge Detection Status[15:8]	GPI_POS_EDGE_INT_STA[7:0]							
		GPI Edge Detection Status[7:0]	GPI_NEG_EDGE_INT_STA[7:0]							

Register Details

Revision ID (0x0)

BIT	15	14	13	12	11	10	9	8
Field	PART_ID[7:0]							
Reset	0xBB							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	REV_ID[7:0]							
Reset	0x45							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PART_ID	15:8	Part Identification Code: 0xBB
REV_ID	7:0	Revision Identification Code: REV_ID[7:4]: 0x4 REV_ID[3:0]: silicon revision (starting at 0x5)

Status & Interrupts (0x1)

BIT	15	14	13	12	11	10	9	8
Field	COMP_INT[3:0]				OVC_INT[3:0]			
Reset	0x0				0x0			
Access Type	Read Clears All				Read Only			

BIT	7	6	5	4	3	2	1	0
Field	Reserved[1:0]		THSHDN_INT	THWRNG_INT	HVDD_INT	TMOUT_INT	GPI_INT	CRC_INT
Reset	0b00		0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only		Read Clears All	Read Only	Read Only	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
COMP_INT	15:12	Comparator interrupt for output channels. Bit 15 = Channel 3 Bit 14 = Channel 2 Bit 13 = Channel 1 Bit 12 = Channel 0 The event reported by the interrupt depends on the setting of COMP_EDGE_CNFG[1:0], which defines global configuration for all channel comparators: COMP_EDGE_CNFG = 0x1, the interrupt reports a rising edge was detected at the output of the corresponding comparator. The interrupt is cleared on read. COMP_EDGE_CNFG = 0x2, the interrupt reports a falling edge was detected at the output of the corresponding comparator. The interrupt is cleared on read. COMP_EDGE_CNFG = 0x3, the interrupt reports the output level of the corresponding comparator. Reading the interrupt register has no impact on this interrupt.	0: No rising or falling edge detected (COMP_EDGE_CNFG = 0x1 or 0x2) or output level is low (COMP_EDGE_CNFG = 0x3). 1: Rising or falling edge detected (COMP_EDGE_CNFG = 0x1 or 0x2) or output level is high (COMP_EDGE_CNFG = 0x3).

BITFIELD	BITS	DESCRIPTION	DECODE
OVC_INT	11:8	Overcurrent interrupt per output channel. Bit 11 = Channel 3 Bit 10 = Channel 2 Bit 9 = Channel 1 Bit 8 = Channel 0 Asserted when the channel is in output-voltage mode and the output current exceeds 50mA (typical). The clearing behavior of this bit depends on the setting of OVC_CNFG in the Configuration register. OVC_CNFG = 0, automatic mode. OVC_INT is cleared once the overcurrent condition is resolved, and the corresponding output amplifier is powered up. OVC_CNFG = 1, host-controlled mode. The corresponding output channel is powered down. OVC_INT is only cleared when read.	0: AOVM current below 50mA 1: AOVM current above 50mA
Reserved	7:6	Reserved	
THSHDN_INT	5	Thermal shutdown interrupt. Asserted when the die temperature exceeds 165°C (typical). The Channel Mode register field CHNL_PWR[3:0] is reset when this interrupt is asserted. Cleared when read.	0: Internal temperature below 165°C 1: Internal temperature above 165°C
THWRNG_INT	4	Thermal warning interrupt. Asserted when the die temperature exceeds 145°C (typical). Cleared when the device internal temperature falls below 135°C (typical).	0: Internal temperature below 145°C (rising), or 135°C (falling) 1: Internal temperature above 145°C
HVDD_INT	3	Asserted when the high-voltage supply HVDD falls below a preset threshold, indicating that the functionality of the amplifiers is not guaranteed. Cleared when the high-voltage supply exceeds the threshold again.	0: HVDD supply is above preset threshold 1: HVDD supply is below preset threshold
TMOUT_INT	2	SPI time-out interrupt. Asserted when no properly formatted SPI transaction has been detected for a duration exceeding the selected time-out period. A properly formatted transaction is a transaction that has a minimum of 24 bits (if CRC is disabled) or 32 bits (if CRC is enabled). A properly formatted transaction is always accounted for at the end of the transaction. Cleared when read.	0: No SPI time-out detected 1: SPI time-out detected

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_INT	1	Asserted when at least one positive or negative edge was detected at the input of at least one input-configured GPIOs, and the GPI edge detection is enabled in the GPI Edge Detection Control register. Cleared when read.	0: No edge detected on any input-configured GPIO 1: At least one edge detected on at least one input-configured GPIO
CRC_INT	0	Asserted when a CRC error is detected when the CRC mode is enabled. Cleared when read.	0: No CRC error detected 1: At least one CRC error detected

Interrupt Enable (0x2)

BIT	15	14	13	12	11	10	9	8
Field	COMP_INTEN[3:0]				OVC_INTEN[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	Reserved[2:0]			THWRNG_INTEN	HVDD_INTEN	TMOUT_INTEN	GPI_INTEN	CRC_INTEN
Reset	0b000			0b0	0b0	0b0	0b0	0b0
Access Type	Read Only			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
COMP_INTEN	15:12	Comparator interrupt enables for COMP_INT[3:0]. Bit 15 = Channel 3 interrupt enable Bit 14 = Channel 2 interrupt enable Bit 13 = Channel 1 interrupt enable Bit 12 = Channel 0 interrupt enable When set, the $\overline{INT}$ pin is asserted low when the corresponding COMP_INT interrupt bit is asserted.	0: COMP_INT does not assert the $\overline{INT}$ pin 1: COMP_INT asserts the $\overline{INT}$ pin
OVC_INTEN	11:8	Overcurrent interrupt enables for OVC_INT[3:0]. Bit 11 = Channel 3 interrupt enable Bit 10 = Channel 2 interrupt enable Bit 9 = Channel 1 interrupt enable Bit 8 = Channel 0 interrupt enable OVC_INT[3:0] interrupt enable. When set, the $\overline{INT}$ pin is asserted low when the corresponding OVC_INT[3:0] interrupt bit is asserted.	0: OVC_INT does not assert $\overline{INT}$ pin 1: OVC_INT asserts $\overline{INT}$ pin
Reserved	7:5	Reserved	
THWRNG_INTEN	4	THWRNG_INT interrupt enable. When set, the $\overline{INT}$ pin is asserted low when the THWRNG_INT interrupt bit is asserted.	0: THWRNG_INT does not assert the $\overline{INT}$ pin 1: THWRNG_INT asserts the $\overline{INT}$ pin

BITFIELD	BITS	DESCRIPTION	DECODE
HVDD_INTEN	3	HVDD_INT interrupt enable. When set, the $\overline{INT}$ pin is asserted low when the HVDD_INT interrupt bit is asserted.	0: HVDD_INT does not assert the $\overline{INT}$ pin 1: HVDD_INT asserts the $\overline{INT}$ pin
TMOUT_INTEN	2	TMOUT_INT interrupt enable. When set, the $\overline{INT}$ pin is asserted low when the TMOUT_INT interrupt bit is asserted.	0: TMOUT_INT does not assert the $\overline{INT}$ pin 1: TMOUT_INT asserts the $\overline{INT}$ pin
GPI_INTEN	1	GPI_INT interrupt enable. When set, the $\overline{INT}$ pin is asserted low when the GPI_INT interrupt bit is asserted.	0: GPI_INT does not assert the $\overline{INT}$ pin 1: GPI_INT asserts the $\overline{INT}$ pin
CRC_INTEN	0	CRC_INT interrupt enable. When set, the $\overline{INT}$ pin is asserted low when the CRC_INT interrupt bit is asserted.	0: CRC_INT does not assert the $\overline{INT}$ pin 1: CRC_INT asserts the $\overline{INT}$ pin

Configuration (0x03)

BIT	15	14	13	12	11	10	9	8
Field	LD_CNFG[3:0]				COMP_EDGE_CNFG[1:0]		Reserved	REF_SEL
Reset	0x0				0b00		0b0	0b0
Access Type	Write, Read				Write, Read		Read Only	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	TMOUT_SEL[3:0]				TMOUT_CNFG	TMOUT_EN	$\overline{OVC\_CNFG}$	CRC_EN
Reset	0x0				0b0	0b0	0b0	0b1
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LD_CNFG	15:12	DAC latch mode control per output channel. Bit 15 = Channel 3 Bit 14 = Channel 2 Bit 13 = Channel 1 Bit 12 = Channel 0	0: The DAC latch is operational and is controlled by the corresponding LD_CTRL bit in the Control register or the $\overline{LDAC}$ pin. 1: The DAC latch is transparent, and any value written to the Channel x Data register is directly applied to the DAC.
COMP_EDGE_CNFG	11:10	Comparator edge detection configuration for all channel comparators	0b00: Powers down the comparators 0b01: Detects rising edges at the comparator outputs 0b10: Detects falling edges at the comparator outputs 0b11: Shows the comparator outputs
Reserved	9	Reserved	
REF_SEL	8	Voltage reference selection	0: Internal voltage reference 1: External voltage reference

BITFIELD	BITS	DESCRIPTION	DECODE
TMOUT_SEL	7:4	Time-out expiration time selection, for typical values.	0x0: 100ms (default) 0x1: 200ms 0x2: 300ms 0x3: 400ms 0x4: 500ms 0x5: 600ms 0x6: 700ms 0x7: 800ms 0x8: 900ms 0x9: 1.0s 0xA: 1.1s 0xB: 1.2s 0xC: 1.3s 0xD: 1.4s 0xE: 1.5s 0xF: 1.6s
TMOUT_CNFG	3	SPI time-out configuration	0: By default, only TMOUT_INT is asserted in case of a time-out event. 1: TMOUT_INT is asserted in case of a time-out event, and the device is reset, except for the TMOUT_INT interrupt bit, the TMOUT_INTEN bit of the Interrupt Enable register, and the CRC_EN bit and REF_SEL bit of the Configuration register.
TMOUT_EN	2	SPI time-out enable	0: SPI time-out function is disabled 1: SPI time-out function is enabled
OVC_CNFG	1	Overcurrent response control	0: Automatic mode In case of overcurrent detection, the device powers down the corresponding output amplifier, indicated by OVC_INT[x], and powers it up every 8ms for 400µs while the overcurrent condition exists. Once the overcurrent condition is resolved, the output amplifier remains in power-up mode. 1: Host-controlled mode In case of overcurrent detection, the device powers down the corresponding output amplifier, indicated by OVC_INT[x], and the corresponding bit in the CHNL_PWR[3:0] register field is reset. The host is then responsible to rewrite the corresponding bit in the CHNL_PWR[3:0] register field to restart the channel.
CRC_EN	0	When set, enables the CRC verification for incoming and outgoing SPI frames. When CRC is enabled, the SPI frame is 32-bits long. When CRC is disabled, the SPI frame is 24-bits long.	0: CRC disabled 1: CRC enabled (default)

Control (0x4)

BIT	15	14	13	12	11	10	9	8
Field	LD_CTRL[3:0]				Reserved[3:0]			
Reset	0x0				0x0			
Access Type	Write Only Clears All				Read Only			

BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
LD_CTRL	15:12	DAC latch load control. When set, loads the contents of the corresponding channel data register to the DAC output if the corresponding LD_CNFG[3:0] configuration bit is logic low. These bits are self-clearing upon the completion of the SPI transaction. Bit 15 = Channel 3 Bit 14 = Channel 2 Bit 13 = Channel 1 Bit 12 = Channel 0	0: No action 1: Loads the contents of the corresponding channel data register to the DAC output
Reserved	11:8	Reserved	
Reserved	7:0	Reserved	

Channel Mode (0x5)

BIT	15	14	13	12	11	10	9	8
Field	CHNL_MODE[3:0]				CHNL_PWR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CHNL_MODE	15:12	Channel mode selection per channel. Bit 15 = Channel 3 Bit 14 = Channel 2 Bit 13 = Channel 1 Bit 12 = Channel 0	0: Voltage mode 1: Current mode

BITFIELD	BITS	DESCRIPTION	DECODE
CHNL_PWR	11:8	Channel power control per channel. Bit 11 = Channel 3 Bit 10 = Channel 2 Bit 9 = Channel 1 Bit 8 = Channel 0	0: Channel powered off 1: Channel powered on
Reserved	7:0	Reserved	

Soft Reset (0x6)

BIT	15	14	13	12	11	10	9	8
Field	Reserved[2:0]			SW_CLR	Reserved[2:0]			SW_RST
Reset	0b000			0b0	0b000			0b0
Access Type	Read Only			Write Only Clears All	Read Only			Write Only Clears All

BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	15:13	Reserved	
SW_CLR	12	Data register reset control. Resets only the Channel Data registers and DAC latch control bits. This bit is self-clearing upon the completion of the SPI transaction.	0: Normal operation 1: Resets all Channel Data registers and DAC latch control bits
Reserved	11:9	Reserved	
SW_RST	8	Software reset control. Resets all registers except CRC_EN and REF_SEL bits in the Configuration register. This bit is self-clearing upon the completion of the SPI transaction.	0: Normal operation 1: Resets all registers except CRC_EN and REF_SEL bits in the Configuration register
Reserved	7:0	Reserved	

Channel 0 Data (0x07)

BIT	15	14	13	12	11	10	9	8
Field	DATA_CH_0[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	DATA_CH_0[3:0]				Reserved[3:0]			
Reset	0x000				0x0			
Access Type	Write, Read				Read Only			

BITFIELD	BITS	DESCRIPTION
DATA_CH_0	15:4	Channel 0 data
Reserved	3:0	Reserved

Channel 1 Data (0x8)

BIT	15	14	13	12	11	10	9	8
Field	DATA_CH_1[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	DATA_CH_1[3:0]				Reserved[3:0]			
Reset	0x000				0x0			
Access Type	Write, Read				Read Only			

BITFIELD	BITS	DESCRIPTION
DATA_CH_1	15:4	Channel 1 data
Reserved	3:0	Reserved

Channel 2 Data (0x9)

BIT	15	14	13	12	11	10	9	8
Field	DATA_CH_2[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	DATA_CH_2[3:0]				Reserved[3:0]			
Reset	0x000				0x0			
Access Type	Write, Read				Read Only			

BITFIELD	BITS	DESCRIPTION
DATA_CH_2	15:4	Channel 2 data
Reserved	3:0	Reserved

Channel 3 Data (0xA)

BIT	15	14	13	12	11	10	9	8
Field	DATA_CH_3[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	DATA_CH_3[3:0]				Reserved[3:0]			
Reset	0x000				0x0			
Access Type	Write, Read				Read Only			

BITFIELD	BITS	DESCRIPTION
DATA_CH_3	15:4	Channel 3 data
Reserved	3:0	Reserved

GPIO Control (0x0B)

BIT	15	14	13	12	11	10	9	8
Field	GPIO_EN[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	GPIO_DIR[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_EN	15:8	GPIO port enable control. Bit 15 = GPIO 7 Bit 14 = GPIO 6 Bit 13 = GPIO 5 Bit 12 = GPIO 4 Bit 11 = GPIO 3 Bit 10 = GPIO 2 Bit 9 = GPIO 1 Bit 8 = GPIO 0	0: GPIO port disabled 1: GPIO port enabled
GPIO_DIR	7:0	GPIO port direction control. Bit 7 = GPIO 7 Bit 6 = GPIO 6 Bit 5 = GPIO 5 Bit 4 = GPIO 4 Bit 3 = GPIO 3 Bit 2 = GPIO 2 Bit 1 = GPIO 1 Bit 0 = GPIO 0	0: Input mode 1: Output mode

GPIO Data (0xC)

BIT	15	14	13	12	11	10	9	8
Field	GPO_DATA[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	GPI_DATA[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
GPO_DATA	15:8	Data to be driven by output-configured GPIO ports. Bit 15 = GPIO 7 Bit 14 = GPIO 6 Bit 13 = GPIO 5 Bit 12 = GPIO 4 Bit 11 = GPIO 3 Bit 10 = GPIO 2 Bit 9 = GPIO 1 Bit 8 = GPIO 0
GPI_DATA	7:0	Data detected at the input-configured GPIO ports. Bit 7 = GPIO 7 Bit 6 = GPIO 6 Bit 5 = GPIO 5 Bit 4 = GPIO 4 Bit 3 = GPIO 3 Bit 2 = GPIO 2 Bit 1 = GPIO 1 Bit 0 = GPIO 0

GPI Edge Detection Control (0xD)

BIT	15	14	13	12	11	10	9	8
Field	GPI_POS_EDGE_INT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	GPI_NEG_EDGE_INT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_POS_EDGE_INT	15:8	Positive edge detection control. When set, enables the detection of rising edges on the corresponding input-configured GPIO port. Bit 15 = GPIO 7 Bit 14 = GPIO 6 Bit 13 = GPIO 5 Bit 12 = GPIO 4 Bit 11 = GPIO 3 Bit 10 = GPIO 2 Bit 9 = GPIO 1 Bit 8 = GPIO 0	0: Positive edge detection disabled 1: Positive edge detection enabled
GPI_NEG_EDGE_INT	7:0	Negative edge detection control. When set, enables the detection of falling edges on the corresponding input-configured GPIO port. Bit 7 = GPIO 7 Bit 6 = GPIO 6 Bit 5 = GPIO 5 Bit 4 = GPIO 4 Bit 3 = GPIO 3 Bit 2 = GPIO 2 Bit 1 = GPIO 1 Bit 0 = GPIO 0	0: Negative edge detection disabled 1: Negative edge detection enabled

GPI Edge Detection Status (0xE)

BIT	15	14	13	12	11	10	9	8
Field	GPI_POS_EDGE_INT_STA[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BIT	7	6	5	4	3	2	1	0
Field	GPI_NEG_EDGE_INT_STA[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_POS_EDGE_INT_STA	15:8	Positive edge detection status. When asserted, indicates that at least one rising edge was detected on the corresponding input-configured GPIO port. Cleared when read. Bit 15 = GPIO 7 Bit 14 = GPIO 6 Bit 13 = GPIO 5 Bit 12 = GPIO 4 Bit 11 = GPIO 3 Bit 10 = GPIO 2 Bit 9 = GPIO 1 Bit 8 = GPIO 0	0: No positive edge was detected 1: At least one positive edge was detected
GPI_NEG_EDGE_INT_STA	7:0	Negative edge detection status. When asserted, indicates that at least one falling edge was detected on the corresponding input-configured GPIO port. Cleared when read. Bit 7 = GPIO 7 Bit 6 = GPIO 6 Bit 5 = GPIO 5 Bit 4 = GPIO 4 Bit 3 = GPIO 3 Bit 2 = GPIO 2 Bit 1 = GPIO 1 Bit 0 = GPIO 0	0: No negative edge was detected 1: At least one negative edge was detected

Applications Information

Single High-Voltage Supply

The MAX22007 is designed to operate with a single positive high-voltage supply (i.e., HVSS is connected to GND). In this case, the linear output-voltage range starts at 300mV above GND_ and the linear output-current range starts at 1.5mA. If performance to all specifications including an output voltage down to 20mV or output current down to 40µA is required, then a negative high-voltage supply V_{HVSS} of -2V must be applied.

Power-Supply Sequencing

The two power supply pairs of the MAX22007 (V_{DD}/GND and HVDD/HVSS) can be powered up in any sequence. Likewise, the positive and negative high-voltage supplies HVDD and HVSS (if HVSS is chosen not to be at the same potential as GND) can be powered up in any sequence.

Power-Supply Decoupling

To reduce ripple and the chance of introducing signal or data errors, bypass V_{DD} and HVDD with a 1µF low-ESR ceramic capacitor to GND respectively, and place the bypass capacitor as close to the V_{DD} and HVDD pins as possible. If a negative high-voltage supply is required, bypass HVSS with a 1µF low-ESR ceramic capacitor to GND and place the bypass capacitor as close to the HVSS pin as possible.

PCB Layout Recommendations

The PCB designer should follow some critical recommendations in order to get the best performance from the MAX22007.

- Use proper grounding techniques such as a multilayer board with low-inductance ground planes.
- Connect all GND and GND_ pins to the GND plane on the PCB.
- Use ground plane shielding to improve noise immunity.
- Keep analog signal traces away from digital signal traces, especially clock traces.
- Connect the exposed pad on the bottom of the MAX22007 to HVSS.
- Maximize the metal coverage for all layers, especially for top and bottom layer to optimize the heat dissipation.
- Maximize the number of vias under the package for thermal purposes. If possible, fill the via with copper, which further enhances the vertical heat transfer through the PCB.
- Package stress needs to be minimized to ensure the output accuracy.

For a detailed recommended layout, refer to the MAX22007 EV kit data sheet.

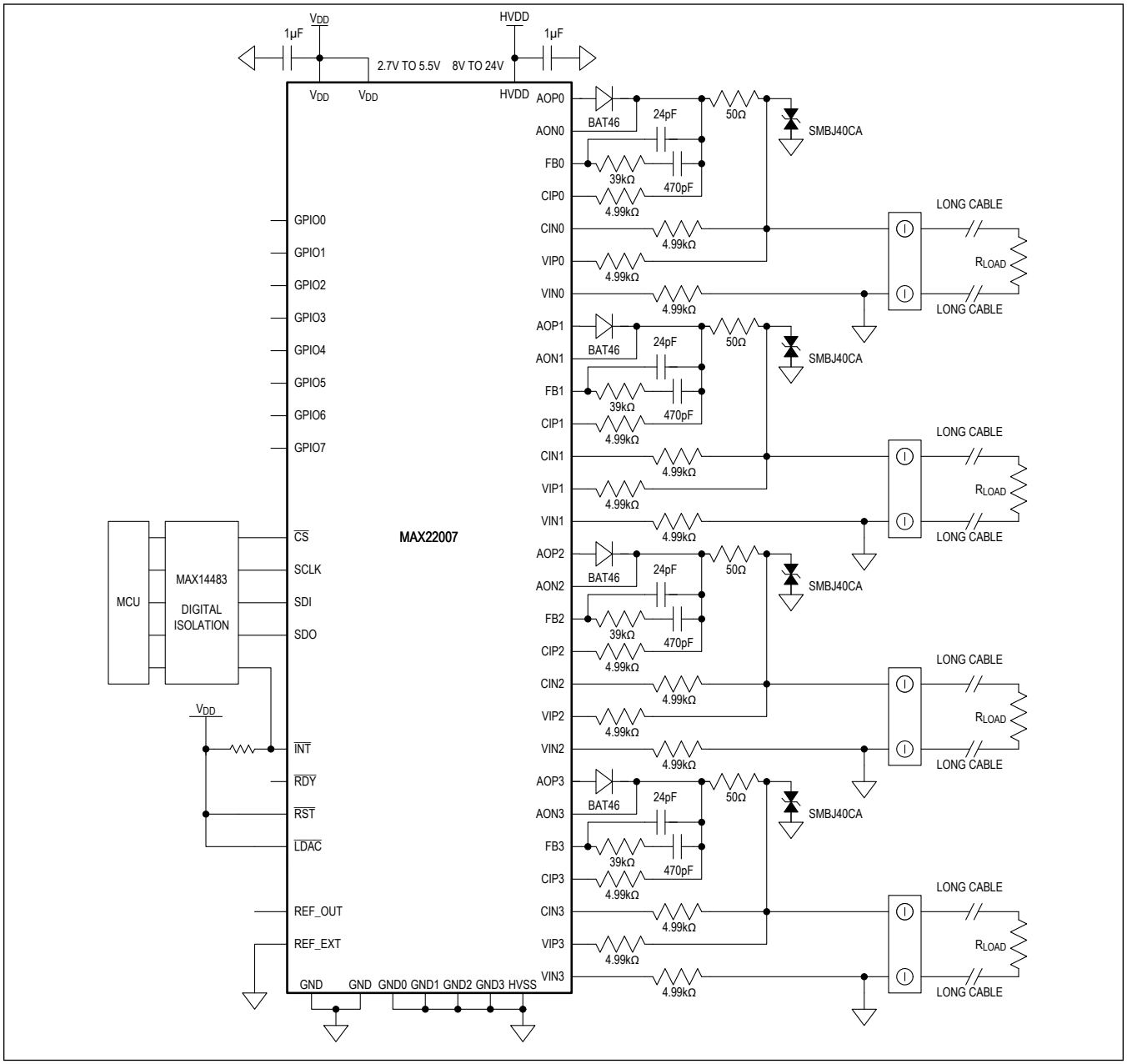
Surge Protection

With external circuitry, the input and output pins are protected against ±1kV/42Ω line-to-line or line-to-ground surge pulses as per IEC 61000-4-5. Place a 40V bidirectional TVS between the outputs and GND, after the AOP_ diode and after the 50Ω current-sense resistor. Place a minimum 4.99kΩ resistor in series with each input pin (CIN_, CIP_, VIN_, and VIP_) at risk.

All other MAX22007 pins are rated for ±2.5kV Human Body Model (HBM) ESD. If surge voltages can couple to the supply rails (HVDD or HVSS), a unidirectional TVS is recommended to be placed on the HVDD or HVSS pins, respectively.

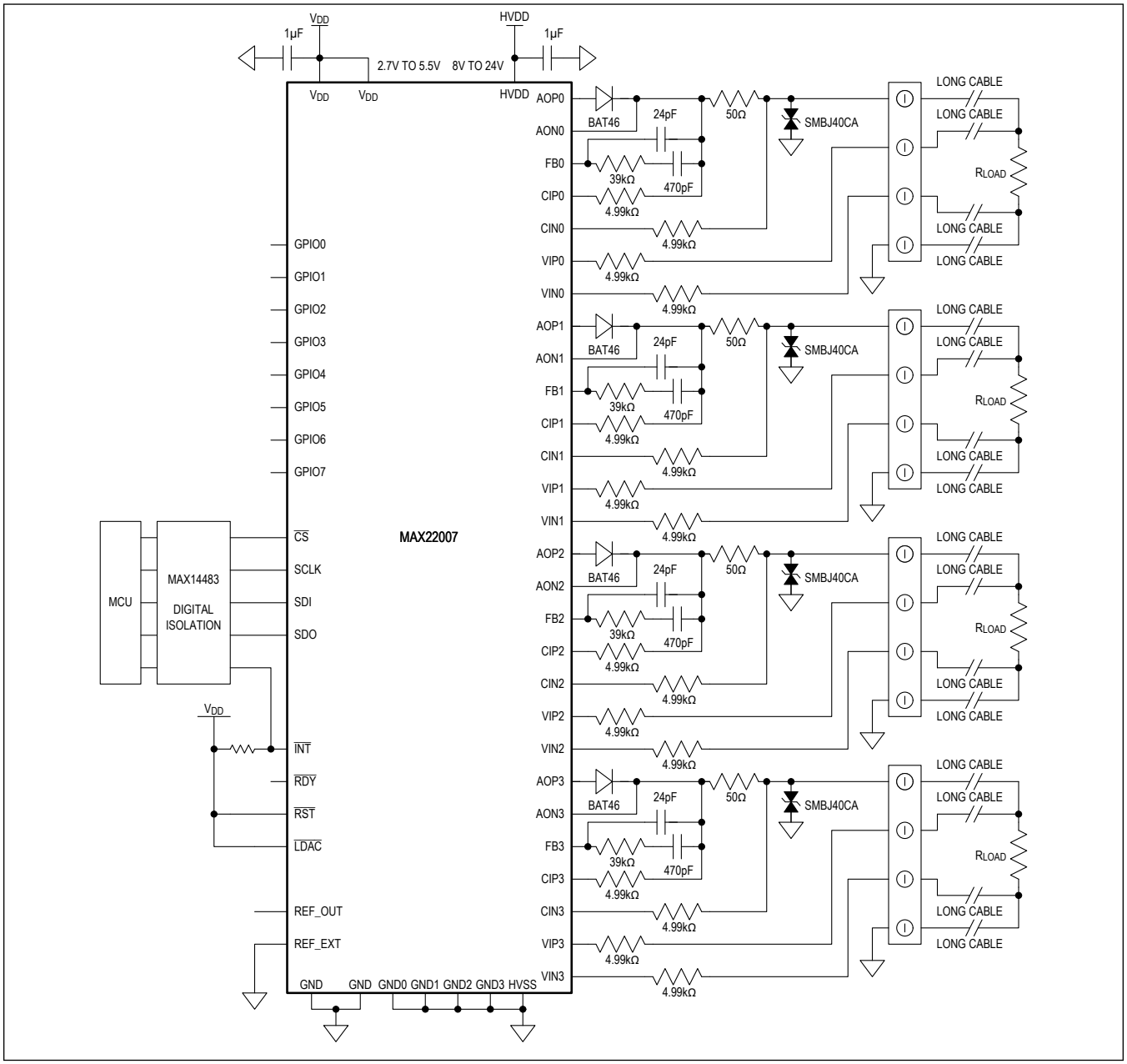
Typical Application Circuits

Two-Wire Application Circuit



Typical Application Circuits (continued)

Four-Wire Application Circuit



Ordering Information

PART	TEMP RANGE	PIN PACKAGE
MAX22007ETN+	-40°C to +85°C	56 TQFN-EP*
MAX22007ETN+T	-40°C to +85°C	56 TQFN-EP*

+ Denotes lead(Pb)-free/RoHS-compliance.

T = Tape-and-reel.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/20	Release for Market Intro	—