MAX20360

PMIC with Ultra-Low I_Q Regulators, Charger, Fuel Gauge, and Haptic Driver for Small Li+ System

General Description

The MAX20360 is a highly integrated and programmable power management solution designed for ultra-low-power wearable applications. It is optimized for size and efficiency to enhance the value of the end product by extending battery life and shrinking the overall solution size. A flexible set of power-optimized voltage regulators, including multiple buck, boost and buck-boost converters, and linear regulators, provides a high level of integration and the ability to create a fully optimized power architecture. The quiescent current of each regulator is ultra-low targeted at extending battery life in always-on applications.

The MAX20360 includes a complete battery management solution with battery seal, charger, power path, and fuel gauge. Both thermal management and input protection are built into the charger. The device also includes a factory programmable button controller with multiple inputs that are customizable to fit specific product UX requirements.

Three integrated LED current sinks are included for indicator or backlighting functions, and an ERM/LRA driver with automatic resonance tracking is capable of providing sophisticated haptic feedback to the user. A low noise, 1.5W buck-boost converter provides a clean way to power LEDs commonly used in optical heart-rate systems. The device is configurable through an I^2C interface that allows for programming various functions and reading the device status, including the ability to read temperature and supply voltages with the integrated ADC. This device is available in a 72-bump, 0.5mm pitch, 4.88mm x 4.19mm, wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

Applications

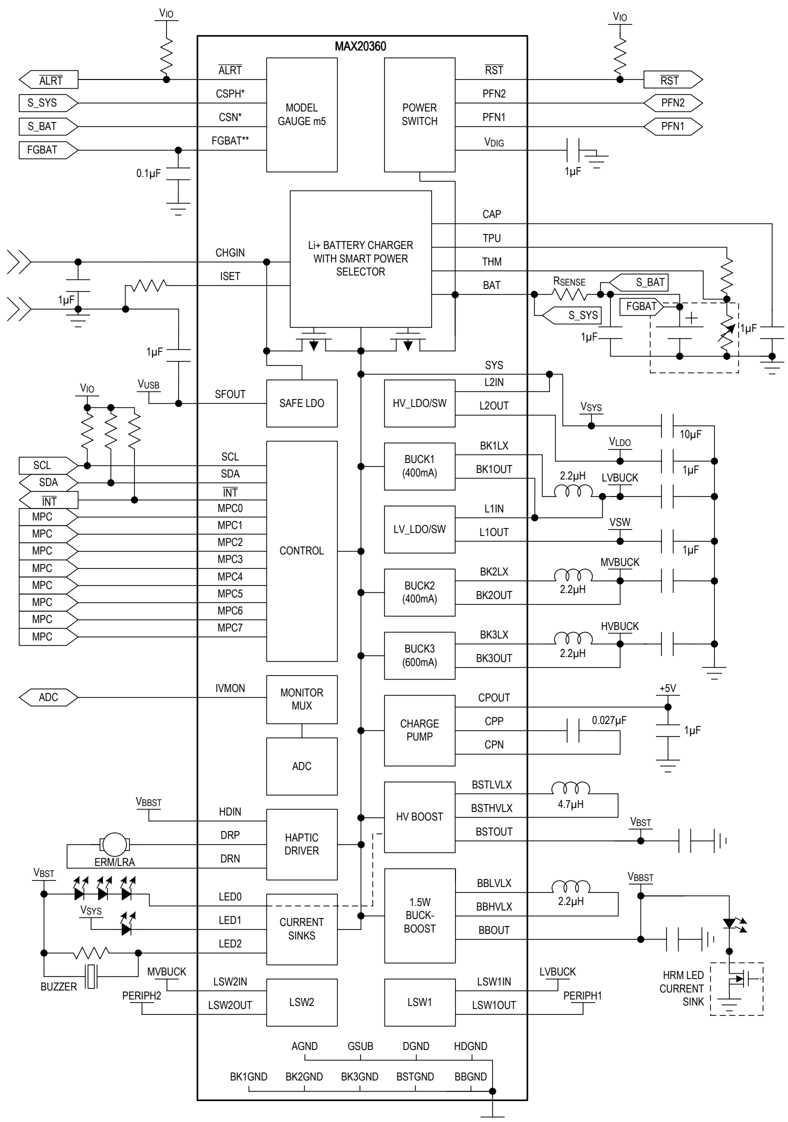
- Wearable Devices
- IoT

Benefits and Features

- Extend Battery-Use Time Between Battery Charging
  - 2 x Micro-I_Q, 400mA Buck Regulators (330nA I_Q typ each)
    - 0.550V to 1.180V in 10mV Steps
    - 0.550V to 2.125V in 25mV Steps
    - 0.550V to 3.700V in 50mV Steps
  - Micro-I_Q, 600mA Buck Regulator (330nA I_Q typ)
    - 0.550V to 1.180V in 10mV Steps
    - 0.550V to 2.125V in 25mV Steps
    - 0.550V to 3.700V in 50mV Steps
  - Micro-I_Q LV LDO/Load Switch (1μA I_Q typ)
    - 1.0V to 2.0V Input Voltage
    - 50mA Output
    - 0.5V to 1.95V Output, 25mV Steps
  - Micro-I_Q LDO/Load Switch (1μA I_Q typ)
    - 1.71V to 5.5V Input Voltage
    - 100mA Output
    - 0.9V to 4V, 100mV Steps
  - Micro-I_Q Buck-Boost Regulator (2μA I_Q typ)
    - 1.5W Output
    - 2.6V to 5V in 50mV Steps
- Easy-to-Implement Li+ Battery Charging
  - Wide Fast Charge Current Range: 5mA to 500mA
  - 28V/-5.5V Tolerant Input
  - Programmable JEITA Current/Voltage Profiles
- Minimize Solution Footprint through High Integration
  - 3.3V or 5.0V Safe Output LDO
    - 15mA When CHGIN Present
  - ERM/LRA Haptic Driver
    - Automatic Braking (LRA Only)
    - Automatic Resonance Tracking (LRA only)
- Supports a Wide Variety of Display Options
  - Micro-I_Q Boost Regulator (2.4μA I_Q typ)
    - 300mW Output
    - 5V to 20V in 250mV Steps
  - 3-Channel Current Sinks
    - 20V Tolerant
    - Programmable from 0.6mA to 30mA
  - Optimize System Control
    - Programmable Push-Button Controller
    - Programmable Supply Sequencing
    - Factory Shelf Mode
    - On-Chip Voltage/Charge Current Monitor Mux and Analog-to-Digital Converter (ADC)

***Ordering Information** appears at end of data sheet.*

Simplified Block Diagram



*KELVIN CONNECT TO RSENSE
**KELVIN CONNECT TO BATTERY CONNECTOR

NOTE: ALL CAPACITANCE LISTED ARE EFFECTIVE CAPACITANCE AFTER DERATING.
FOR SWITCHING REGULATORS, PLEASE REFER TO THE CAPACITANCE SELECTION SECTION IN THE DETAILED DESCRIPTION FOR THE CORRESPONDING REGULATOR.

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Absolute Maximum Ratings

(All voltages referenced to GSUB, unless otherwise noted) ....
CHGIN .... -6.0V to +30.0V
SYS, BAT, SDA, SCL, TPU, IVMON, RST, INT, PFN_, HDIN, L2IN, LSW_IN, BBOUT, FGBAT .... -0.3V to +6.0V
THM.................................... -0.3V to min(V_{FGBAT} + 0.3V, +6.0V)
ALRT .... -0.3V to +17.0V
CAP, SFOUT .... -0.3V to min(|V_{CHGIN}| + 0.3V, +6.0V)
L1IN, VDIG .... -0.3V to +2.2V
MPC_, BK_LX, BK_OUT, BBLVLX, BSTLVLX, CPN.......-0.3V to (V_{SYS} + 0.3V)
DRP, DRN .... -0.3V to min(V_{HDIN} + 0.3V, +6.0V)
BBHVLX .... -0.3V to min(V_{BBOUT} + 0.3V, +6.0V)
ISET................... -0.3V to min(V_{BAT} + 0.3V, V_{SYS} + 0.3V, +6.0V)
L_OUT .... -0.3V to (V_{L_IN} +0.3V)
LSW_OUT .... -0.3V to (V_{LSW_IN} + 0.3V)
CPP .... (V_{CPN} - 0.3V) to (V_{CPN} + 6.0V)
CPOUT .... (V_{CPP} - 0.3V) to min(V_{CPP} + 6.0V, +12.0V)
BSTHVLX, BSTOUT, LED_ .... -0.3V to +22.0V
BK_GND, BSTGND, BBGND, HDGND, AGND, DGND .. -0.3V to +0.3V
CSN, CSPH .... -0.3V to (V_{FGBAT} + 0.3V)
Continuous Current into BK_OUT, BK_LX, BBLVLX, BBHVLX, BBOUT, BSTLVLX, BSTHVLX, BSTOUT........................±660mA
Continuous Current into L_IN, L_OUT............................±250mA
Continuous Current into SW_IN, SW_OUT ....±140mA
Continuous Current into BAT, SYS, CHGIN ....±1000mA
Continuous Current into DRP, DRN, HDIN......................±600mA
Continuous Current into Any Other Terminal...................±100mA
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 32.53mW/°C above +70°C.) 2602mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Soldering Temperature (reflow) .... +260ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

72 WLP

Package Code	W724A4+1
Outline Number	21-100373
Land Pattern Number	Refer to *Application Note 1891*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	30.74°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL SUPPLY CURRENT						
CHGIN Input Current	I_{CHGIN}	V_{CHGIN} = 5V, ON mode, Charger disabled, THM monitoring disabled, SFOUT disabled, LDO2 disabled, all other rails disabled		0.81		mA

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BAT Input Current	I_{BAT}	V_{CHGIN} = 0V, SEAL mode, LDO2 disabled		0.25		μA
		V_{CHGIN} = 0V, OFF mode, LDO2 enabled, L2IN connected to BAT, Fuel Gauge contribution not included		1.50		
		V_{CHGIN} = 0V, Battery Recovery (BR) mode, LDO2 disabled, Fuel Gauge contribution not included		1.35		
		V_{CHGIN} = 0V, ON mode, LDO2 disabled, all other rails disabled, Fuel Gauge contribution not included		1.50		
		V_{CHGIN} = 0V, ON mode, LDO2 disabled, Buck1 enabled, all other rails disabled, Fuel Gauge contribution not included		1.87		
		V_{CHGIN} = 0V, ON mode, LDO2 disabled, Buck1 enabled, Buck2 enabled, all other rails disabled, Fuel Gauge contribution not included		2.19		
		V_{CHGIN} = 0V, ON mode, LDO2 disabled, Buck1 enabled, Buck2 enabled, Buck3 enabled, all other rails disabled, Fuel Gauge contribution not included		2.69		
INTERNAL SUPPLIES, UVLOS, AND BAT OCP						
V_{CCINT} OTP OK Threshold / Startup Voltage	$V_{CCINT\_OTP\_OK}$	V_{CCINT} rising (Note 2)		2.92	3.25	V
		V_{CCINT} falling (Note 2)	2.60	2.90		
V_{DIG} OTP OK Threshold	$V_{DIG\_OTP\_OK}$	V_{DIG} rising		1.52	1.62	V
		V_{DIG} falling	1.41	1.51		
V_{CCINT} UVLO Threshold (POR)	V_{CCINT_UVLO}	V_{CCINT} rising (Note 2)	2.20	2.45	2.75	V
		V_{CCINT} falling (Note 2)	2.15	2.40	2.70	
V_{CCINT} UVLO Threshold (POR) Hysteresis	$V_{CCINT\_UVLO\_H}$	(Note 2)		50		mV
Internal VDIG Regulator	V_{DIG}		1.71	1.80	1.89	V
V_{DIG} UVLO Threshold	V_{DIG_UVLO}	V_{DIG} rising	1.59		1.73	V
		V_{DIG} falling	1.51		1.61	
V_{DIG} UVLO Threshold Hysteresis	$V_{DIG\_UVLO\_H}$			100		mV
Internal CAP Regulator	V_{CAP}	V_{CHGIN} = 4.3V to 28.0V	3.75	4.10	4.55	V
CAP Detect Threshold	V_{CAP_DET}	V_{CHGIN} = V_{CAP} rising	3.15	3.40	3.60	V
		V_{CHGIN} = V_{CAP} falling	2.60	2.80	3.00	

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CAP Detect Threshold Hysteresis	$V_{CAP\_DET\_H}$				600		mV
CHGIN Detect Threshold	V_{CHGIN_DET}	V_{CHGIN} rising		4.00	4.15	4.30	V
		V_{CHGIN} falling		3.20	3.30	3.40	
CHGIN Detect Threshold Hysteresis	$V_{CHGIN\_DET\_H}$				850		mV
CHGIN Detection Debounce Time	t_{CHGIN_DET}	CHGIN insertion			108		ms
		CHGIN detachment			100		
SYS UVLO Threshold	V_{SYS_UVLO}	Device Specific (see Table 8)	V_{SYS} rising, VSysUvlo = 00	2.65	2.75	2.85	V
			V_{SYS} falling, VSysUvlo = 00	2.60	2.70	2.80	
			V_{SYS} falling, VSysUvlo = 01	2.80	2.90	3.00	
			V_{SYS} falling, VSysUvlo = 10	2.90	3.00	3.10	
			V_{SYS} falling, VSysUvlo = 11	3.10	3.20	3.30	
SYS UVLO Threshold Hysteresis	$V_{SYS\_UVLO\_H}$				50		mV
SYS UVLO Falling Debounce Time	$t_{SYS\_UVLO\_FD}$	V_{SYS} falling			20		µs
BAT OCP Threshold Accuracy	$I_{BAT\_OCP\_ACC}$	I_{SYS} rising, threshold from 200mA to 400mA in 200mA steps, device specific (see IBatOc in Table 8)		-50		+50	%
		I_{SYS} rising, threshold from 600mA to 1.6A in 200mA steps, device specific (see IBatOc in Table 8)		-40		+40	
BAT OCP Threshold Hysteresis	$I_{BAT\_OCP\_H}$				7		%
BAT OCP Rising Debounce Time	$t_{BAT\_OCP\_RD}$	I_{SYS} rising			50		ms
OVP AND INPUT CURRENT LIMITER							
CHGIN Overvoltage Threshold	V_{CHGIN_OV}	V_{CHGIN} rising		7.2	7.5	7.8	V
CHGIN Overvoltage Threshold Hysteresis	$V_{CHGIN\_OV\_H}$				200		mV
CHGIN-SYS Valid Trip Point	$V_{CHGIN\_SYS\_TP}$	V_{CHGIN} - V_{SYS} rising		30	145	290	mV
CHGIN-SYS Valid Trip Point Hysteresis	$V_{CHGIN\_SYS\_TP\_H}$				275		mV

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Overcurrent Max Limit	I_{LIM_MAX}	Device Specific (see Table 8)	t < t_{ILIM_BLANK}, ILimMax = 0	400	450	500	mA
			t < t_{ILIM_BLANK}, ILimMax = 1	800	1000	1250	
Input Current Limit	I_{LIM}	ILimCntl = 000			50		mA
		ILimCntl = 001			90		
		ILimCntl = 010			150		
		ILimCntl = 011			200		
		ILimCntl = 100			300		
		ILimCntl = 101			400		
		ILimCntl = 110		400	450	500	
		ILimCntl = 111		900	1000	1100	
Input Current-Limit Blanking Time	t_{ILIM_BLANK}	ILimBlank = 00			0.0		ms
		ILimBlank = 01			0.5		
		ILimBlank = 10			1.0		
		ILimBlank = 11			10.0		
SYS Regulation Voltage	V_{SYS_REG}			V_{BAT_REG} + 0.14	V_{BAT_REG} + 0.20	V_{BAT_REG} + 0.26	V
SYS Regulation-Voltage Dropout	$V_{CHGIN\_SYS\_REG}$				40		mV
CHGIN to SYS On Resistance	R_{CHGIN_SYS}				0.37	0.66	Ω
Input Current Soft-Start Time	t_{ILIM_SFT}				1		ms
Thermal Shutdown Temperature	T_{CHG_SHDN}	Device Specific (see Table 8)	TShdn = 000		50		°C
			TShdn = 001		60		
			TShdn = 010		70		
			TShdn = 011		80		
			TShdn = 100		90		
			TShdn = 101		100		
			TShdn = 110		110		
			TShdn = 111		120		
CHGIN Boot Retry Timeout	$t_{CHG\_RETRY\_TMO}$	ChgAlwTry = 1, Device Specific (see Table 8)			0.5		s
BATTERY CHARGER							
BAT to SYS On Resistance	R_{BAT_SYS}	V_{BAT} = 4.2V, I_{BAT} = 300mA			80	140	mΩ

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Thermal Regulation Temperature	T_{CHG_LIM}				T_{CHG_SHDN} - 3		°C
BAT to SYS Switch On Threshold	$V_{BAT\_SYS\_ON}$	V_{SYS} falling, measured as V_{BAT} - V_{SYS}		10	19	35	mV
BAT to SYS Switch Off Threshold	$V_{BAT\_SYS\_OFF}$	V_{SYS} rising, measured as V_{BAT} - V_{SYS}		-3	-1	0	mV
SYS to BAT Charge Current Reduction Threshold	$V_{SYS\_BAT\_REG}$	Measured as V_{SYS} - V_{BAT}, SysMinVlt = 000, V_{BAT} > 3.6V			100		mV
Minimum SYS Voltage	V_{SYS_LIM}	V_{BAT} < 3.4V	SysMinVlt = 000		3.6		V
			SysMinVlt = 001		3.7		
			SysMinVlt = 010		3.8		
			SysMinVlt = 011		3.9		
			SysMinVlt = 100		4.0		
			SysMinVlt = 101		4.1		
			SysMinVlt = 110		4.2		
			SysMinVlt = 111		4.3		
Charger Current Soft-Start Time	t_{ICHG_SFT}				1		ms
Precharge Current	I_{PCHG}	IPChg = 00			0.05 x I_{FCHG}		mA
		IPChg = 01		0.09 x I_{FCHG}	0.10 x I_{FCHG}	0.11 x I_{FCHG}	
		IPChg = 10			0.20 x I_{FCHG}		
		IPChg = 11			0.30 x I_{FCHG}		
Precharge Threshold	V_{BAT_PCHG}	V_{BAT} rising	VPChg = 000		2.10		V
			VPChg = 001		2.25		
			VPChg = 010		2.40		
			VPChg = 011		2.55		
			VPChg = 100		2.70		
			VPChg = 101		2.85		
			VPChg = 110		3.00		
			VPChg = 111		3.15		
Precharge Threshold Hysteresis	$V_{BAT\_PCHG\_H}$				90		mV

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Step-Charge Threshold	V_{BAT_STPCHG}	V_{BAT} rising	ChgStepRise = 0000		3.80		V
			ChgStepRise = 0001		3.85		
			ChgStepRise = 0010		3.90		
			ChgStepRise = 0011		3.95		
			ChgStepRise = 0100		4.00		
			ChgStepRise = 0101		4.05		
			ChgStepRise = 0110		4.10		
			ChgStepRise = 0111		4.15		
			ChgStepRise = 1000		4.20		
			ChgStepRise = 1001		4.25		
			ChgStepRise = 1010		4.30		
			ChgStepRise = 1011		4.35		
			ChgStepRise = 1100		4.40		
			ChgStepRise = 1101		4.45		
			ChgStepRise = 1110		4.50		
			ChgStepRise = 1111		4.55		
Step-Charge Threshold Hysteresis	$V_{BAT\_STPCHG\_H}$	ChgStepHys = 000			100		mV
		ChgStepHys = 001			200		
		ChgStepHys = 010			300		
		ChgStepHys = 011			400		
		ChgStepHys = 100			500		
		ChgStepHys = 101			600		

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fast-Charge Current Reduction Due to Step Charge	I_{FCHG_STPCHG}	ChgIStep = 000		0.2 x I_{FCHG}		mA
		ChgIStep = 001		0.3 x I_{FCHG}		
		ChgIStep = 010		0.4 x I_{FCHG}		
		ChgIStep = 011		0.5 x I_{FCHG}		
		ChgIStep = 100		0.6 x I_{FCHG}		
		ChgIStep = 101		0.7 x I_{FCHG}		
		ChgIStep = 110		0.8 x I_{FCHG}		
		ChgIStep = 111		I_{FCHG}		
ISET Current Gain Factor	K_{ISET}			2000		A/A
ISET Regulation Voltage	V_{ISET}			1		V
BAT Fast-Charge Current Set Range	I_{FCHG}	R_{ISET} = 400kΩ		5		mA
		R_{ISET} = 40kΩ	45	50	55	
		R_{ISET} = 4kΩ		500		

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Battery-Regulation Voltage	V_{BAT_REG}	ChgBatReg = 0000			4.0500		V
		ChgBatReg = 0001			4.1000		
		ChgBatReg = 0010			4.1500		
		ChgBatReg = 0011	T_A = 25°C	4.1853	4.2000	4.2147	
			T_A = -5°C to +50°C	4.1769	4.2000	4.2231	
				4.1622	4.2000	4.2378	
		ChgBatReg = 0100			4.2500		
		ChgBatReg = 0101			4.3000		
		ChgBatReg = 0110			4.3500		
		ChgBatReg = 0111	T_A = 25°C	4.3846	4.4000	4.4154	
			T_A = -5°C to +50°C	4.3758	4.4000	4.4242	
				4.3604	4.4000	4.4396	
		ChgBatReg = 1000	T_A = 25°C	4.4344	4.4500	4.4656	
			T_A = -5°C to +50°C	4.4255	4.4500	4.4745	
				4.4099	4.4500	4.4901	
		ChgBatReg = 1001			4.5000		
		ChgBatReg = 1010			4.5500		
		ChgBatReg = 1011			4.6000		
Battery-Recharge Threshold	V_{BAT_RECHG}	ChgBatReChg = 00			70		mV
		ChgBatReChg = 01			120		
		ChgBatReChg = 10			170		
		ChgBatReChg = 11			220		
Maximum Precharge Time	t_{PCHG}	PChgTmr = 00			30		min
		PChgTmr = 01			60		
		PChgTmr = 10			120		
		PChgTmr = 11			240		
Maximum Fast-Charge Time	t_{FCHG}	FChgTmr = 00			75		min
		FChgTmr = 01			150		
		FChgTmr = 10			300		
		FChgTmr = 11			600		

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge Done Qualification	I_{CHG_DONE}	IChgDone = 00		0.050 x I_{FCHG}		mA
		IChgDone = 01	0.085 x I_{FCHG}	0.100 x I_{FCHG}	0.115 x I_{FCHG}	
		IChgDone = 10		0.200 x I_{FCHG}		
		IChgDone = 11		0.300 x I_{FCHG}		
Maximum Maintain Charge Time	t_{MTCHG}	MtChgTmr = 00		0		min
		MtChgTmr = 01		15		
		MtChgTmr = 10		30		
		MtChgTmr = 11		60		
Timer Accuracy	t_{CHG_ACC}		-10		+10	%
Fast-Charge Timer Extend Current Threshold	I_{FCHG_TEXT}	See Figure 32		50		%I_{FCHG}
Fast-Charge Timer Suspend Current Threshold	I_{FCHG_TSUS}	See Figure 32		20		%I_{FCHG}
Battery Regulation Voltage Reduction Due to Temperature	$V_{BAT\_REG\_JTA}$	ChgCool/Room/WarmBatReg = 00		V_{BAT_REG} - 0.15		V
		ChgCool/Room/WarmBatReg = 01		V_{BAT_REG} - 0.1		
		ChgCool/Room/WarmBatReg = 10		V_{BAT_REG} - 0.05		
		ChgCool/Room/WarmBatReg = 11		V_{BAT_REG}		

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fast-Charge Current Reduction Due to Temperature	I_{FCHG_JTA}	ChgCool/Room/WarmIFChg = 000		0.20 x I_{FCHG}		mA
		ChgCool/Room/WarmIFChg = 001		0.30 x I_{FCHG}		
		ChgCool/Room/WarmIFChg = 010		0.40 x I_{FCHG}		
		ChgCool/Room/WarmIFChg = 011		0.50 x I_{FCHG}		
		ChgCool/Room/WarmIFChg = 100		0.60 x I_{FCHG}		
		ChgCool/Room/WarmIFChg = 101		0.70 x I_{FCHG}		
		ChgCool/Room/WarmIFChg = 110		0.80 x I_{FCHG}		
		ChgCool/Room/WarmIFChg = 111		I_{FCHG}		
BAT UVLO Threshold	V_{BAT_UVLO}	V_{BAT} rising, valid only when CHGIN is present, when V_{BAT} < V_{BAT_UVLO} the BAT to SYS switch opens and BAT is connected to SYS through a diode	1.95	2.05	2.15	V
BAT UVLO Threshold Hysteresis	$V_{BAT\_UVLO\_H}$			50		mV
BAT Pulldown Resistance	R_{BAT_PD}	BatPD = 1		15		kΩ
HARVESTER INTERACTION						
Harvester Interaction Comparator Quiescent Current	$I_{HARV\_CMP\_Q}$	V_{BAT} = 3.7V		0.25		μA
Harvester Interaction Ideal BAT to SYS Diode Quiescent Current	$I_{HARV\_BAT\_SYS\_DIO\_Q}$	V_{BAT} = 4.2V, I_{SYS} = 0μA		0.65		μA
		V_{BAT} = 4.2V, I_{SYS} = 10mA		12		
Harvester Interaction SYS to BAT Diode Drop in POR / SEAL Mode	$V_{HARV\_SYS\_BAT\_DIO\_PORSEAL}$	POR condition, V_{BAT} = 2.1V, I_{SYS} = -20mA		0.6		V

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Harvester Interaction Battery Charging Stop Threshold	$V_{HARV\_BAT\_REG}$	V_{BAT} rising, T_A = -18°C,+80°C	HrvBatReg = 0000	3.9710	4.0500	4.0723	V
			HrvBatReg = 0001	4.0200	4.1000	4.1226	
			HrvBatReg = 0010	4.0691	4.1500	4.1728	
			HrvBatReg = 0011	4.1181	4.2000	4.2231	
			HrvBatReg = 0100	4.1671	4.2500	4.2734	
			HrvBatReg = 0101	4.2161	4.3000	4.3237	
			HrvBatReg = 0110	4.2652	4.3500	4.3739	
			HrvBatReg = 0111	4.3142	4.4000	4.4242	
			HrvBatReg = 1000	4.3632	4.4500	4.4745	
			HrvBatReg = 1001	4.4122	4.5000	4.5248	
			HrvBatReg = 1010	4.4613	4.5500	4.5750	
			HrvBatReg = 1011	4.5103	4.6000	4.6253	
Harvester Interaction Battery Charging Restart Threshold	$V_{HARV\_BAT\_RECHG}$	V_{BAT} falling	HrvBatReChg = 00		$V_{HARV\_BAT\_REG}$ - 0.07		V
			HrvBatReChg = 01		$V_{HARV\_BAT\_REG}$ - 0.12		
			HrvBatReChg = 10		$V_{HARV\_BAT\_REG}$ - 0.17		
			HrvBatReChg = 11		$V_{HARV\_BAT\_REG}$ - 0.22		
Harvester Interaction Battery Charging Stop Threshold Reduction Due to Temperature	$V_{HARV\_BAT\_REG\_JTA}$	HrvCool/Room/WarmBatReg = 00			$V_{HARV\_BAT\_REG}$ - 0.15		V
		HrvCool/Room/WarmBatReg = 01			$V_{HARV\_BAT\_REG}$ - 0.10		
		HrvCool/Room/WarmBatReg = 10			$V_{HARV\_BAT\_REG}$ - 0.05		
		HrvCool/Room/WarmBatReg = 11			$V_{HARV\_BAT\_REG}$		
Harvester Interaction Ideal BAT-to-SYS Diode Regulation	$V_{HARV\_BAT\_SYS\_DIO\_REG}$	V_{BAT} = 4.2V, I_{SYS} = 100mA, measured as V_{BAT} - V_{SYS}			28		mV

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Harvester Interaction Ideal BAT-to-SYS Diode Load Transient	$V_{HARV\_BAT\_SYS\_DIO\_LOADTRAN}$	V_{BAT} = 4.2V, I_{SYS} = from -20mA to 1A in 1µs, measured as V_{BAT} - V_{SYS}			165		mV
Harvester Interaction Ideal BAT-to-SYS Diode Release Delay	$t_{HARV\_BAT\_SYS\_DIO\_REL}$	V_{BAT} = 4.2V, I_{SYS} = from 1A to -1mA in 1µs, measured as the time from when I_{BAT} goes negative to when it rises above -50µA			110		µs
SFOUT LDO							
SFOUT LDO Voltage	V_{SFOUT}	SFOUTVSet = 0 (5V), V_{CHGIN} = 6V, I_{SFOUT} = 0mA		4.85	5.00	5.15	V
		SFOUTVSet = 0 (5V), V_{CHGIN} = 5V, I_{SFOUT} = 15mA			4.90		
		SFOUTVSet = 1 (3.3V), V_{CHGIN} = 5V, I_{SFOUT} = 0mA		3.15	3.30	3.45	
		SFOUTVSet = 1 (3.3V), V_{CHGIN} = 5V, I_{SFOUT} = 15mA			3.29		
SFOUT OVP Voltage	V_{SFOUT_OV}	SFOUT LDO is turned off if V_{CHGIN} is above V_{CHGIN_OV} threshold			V_{CHGIN_OV}		V
SFOUT Thermal Limit	T_{SFOUT_LIM}				150		°C
THERMISTOR MONITOR							
THM Monitoring Quiescent Current	I_{THM_Q}	VDIG to TPU switch closed, THM measurement running			190		µA
Harvester Interaction THM Hot Threshold	$V_{HRV\_THM\_HOT}$	Device Specific (see JEITASet and HrvEn in Table 8)	V_{THM} falling, JEITASet = 0, HrvEn = 1 and Harvester Actively Charging	12.51	14.51	16.51	$\%V_{DIG}$
			V_{THM} falling, JEITASet = 1, HrvEn = 1 and Harvester Actively Charging	21.53	23.53	25.53	
THM Hot Threshold	V_{THM_HOT}	Device Specific (see JEITASet in Table 8)	V_{THM} falling, JEITASet = 0, No Harvester mode	21.53	23.53	25.53	$\%V_{DIG}$
			V_{THM} falling, JEITASet = 1, No Harvester mode	30.94	32.94	34.94	
THM Warm Threshold	V_{THM_WARM}	Device Specific (see JEITASet in Table 8)	V_{THM} falling, JEITASet = 0	30.94	32.94	34.94	$\%V_{DIG}$
			V_{THM} falling, JEITASet = 1	48.20	50.20	52.20	
THM Cool Threshold	V_{THM_COOL}	V_{THM} rising		62.31	64.31	66.31	$\%V_{DIG}$

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
THM Cold Threshold	V_{THM_COLD}	V_{THM} rising, No Harvester mode		71.73	73.73	75.73	%V_{DIG}
Harvester THM Cold Threshold	$V_{HRV\_THM\_COLD}$	Device Specific (see HrvEn in Table 8)	V_{THM} rising, HrvEn = 1 and Harvester Actively Charging	79.57	81.57	83.57	%V_{DIG}
THM Disable Threshold	V_{THM_DIS}	V_{THM} rising		90.94	92.94	94.94	%V_{DIG}
THM Threshold Hysteresis	V_{THM_H}				60		mV
THM Input Leakage	I_{THM_LK}	V_{THM} = 0V to 5.5V, Fuel Gauge contribution not included		-1		+1	μA
TPU Input Leakage	I_{TPU_LK}	VDIG to TPU switch disabled, V_{TPU} = 0V to 5.5V		-1		+1	μA
V_{DIG}-to-TPU Switch Resistance	R_{VDIG_TPU}	3mA through the switch			3	10	Ω
IVMON MULTIPLEXER							
IVMON Multiplexer Output Ratio	$V_{IVMON\_DIV\_RT}$	No load on IVMON pin. Inputs: Charger Current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, SFOUT, BBOUT	IVMONRatioConfig = 00		100.0		%
			IVMONRatioConfig = 01		50.0		
			IVMONRatioConfig = 10		33.3		
			IVMONRatioConfig = 11		25.0		
IVMON Multiplexer Output Impedance	R_{IVMON_DIV}	10μA load on IVMON pin. Inputs Charger Current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, SFOUT, BBOUT	IVMONRatioConfig = 00		5.5		kΩ
		1μA load on IVMON pin. Inputs Charger Current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, SFOUT, BBOUT	IVMONRatioConfig = 01		31.0		
			IVMONRatioConfig = 10		28.0		
			IVMONRatioConfig = 11		24.0		
IVMON Input Leakage	I_{IVMON_LK}	IVMON multiplexer disabled, pulldown resistance disabled, V_{IVMON} = 0V to 5.5V		-1		+1	μA

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IVMON Multiplexer Off-State Pulldown Resistance	R_{IVMON_OFF}	IVMON multiplexer disabled, pulldown resistance enabled		59.0		kΩ
SAR ADC						
ADC Quiescent Current	I_{ADC_Q}	Conversion running		930		µA
ADC HDIN Divider Resistance	$R_{ADC\_HDIN\_DIV}$	HDIN conversion running		2.20		MΩ
ADC IVMON Divider Resistance	$R_{ADC\_IVMON\_DIV}$	IVMON conversion running		2.20		MΩ
ADC CHGIN Divider Resistance	$R_{ADC\_CHGIN\_DIV}$	CHGIN conversion running		1.10		MΩ
ADC CPOUT Divider Resistance	$R_{ADC\_CPOUT\_DIV}$	CPOUT conversion running		0.82		MΩ
ADC BSTOUT Divider Resistance	$R_{ADC\_BSTOUT\_DIV}$	BSTOUT conversion running		0.89		MΩ
ADC HDIN Least Significant Bit	$V_{ADC\_HDIN\_LSB}$			21.57		mV
ADC IVMON Least Significant Bit	$V_{ADC\_IVMON\_LSB}$			21.57		mV
ADC CHGIN Least Significant Bit	$V_{ADC\_CHGIN\_LSB}$			32.35		mV
ADC CPOUT Least Significant Bit	$V_{ADC\_CPOUT\_LSB}$			32.35		mV
ADC BSTOUT Least Significant Bit	$V_{ADC\_BSTOUT\_LSB}$			82.35		mV
ADC HDIN Absolute Sensing Worst-Case Accuracy	$V_{ADC\_HDIN\_ACC}$	V_{HDIN} = 2.6V	-65		+65	mV
		V_{HDIN} = 5.5V	-123		+123	
ADC IVMON Absolute Sensing Worst-Case Accuracy	$V_{ADC\_IVMON\_ACC}$	V_{IVMON} = 1.0V	-34		+34	mV
		V_{IVMON} = 5.5V	-123		+123	
ADC CHGIN Absolute Sensing Worst-Case Accuracy	$V_{ADC\_CHGIN\_ACC}$	V_{CHGIN} = 3.0V	-79		+79	mV
		V_{CHGIN} = 8.0V	-178		+178	
ADC CPOUT Absolute Sensing Worst-Case Accuracy	$V_{ADC\_CPOUT\_ACC}$	V_{CPOUT} = 5.0V	-118		+118	mV
		V_{CPOUT} = 6.6V	-150		+150	
ADC BSTOUT Absolute Sensing Worst-Case Accuracy	$V_{ADC\_BSTOUT\_ACC}$	V_{BSTOUT} = 3.0V	-115		+115	mV
		V_{BSTOUT} = 21.0V	-465		+465	
ADC Conversion Time	t_{ADC_CONV}	1.1ms (typ) additional delay prior to each 1st conversion		82		µs

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HAPTIC DRIVER						
Input Voltage	V_{HDIN}		2.6		5.5	V
Quiescent Current	I_{HD_Q}	V_{DRP} / V_{DRN} = 0V to V_{HDIN}		1.25		mA
HDIN UVLO Threshold	V_{HDIN_UVLO}	V_{HDIN} rising	2.65	2.75	2.85	V
		V_{HDIN} falling	2.60	2.70	2.80	
HDIN UVLO Threshold Hysteresis	$V_{HDIN\_UVLO\_H}$			50		mV
H-Bridge PWM Output Frequency	$f_{HD\_PWM\_OUT}$		22.5	25.0	27.5	kHz
H-Bridge PWM Output Duty-Cycle Resolution	$D_{HD\_PWM\_OUT}$	7 bits		V_{HDIN} / 128		%V_{HDIN}
H-Bridge Output-Impedance in Off State	R_{HD_OFF}	HptOffImp = 1		15		kΩ
		HptOffImp = 0		$R_{HD\_ON\_LS}$		Ω
H-Bridge Output Leakage in High-Z State	I_{HD_LK}	During back EMF detection, V_{DRP} / V_{DRN} = 0V to V_{HDIN}	-1		+1	µA
H-Bridge On Resistance	$R_{HD\_ON\_HS}$	High-side pMOS switch on, 300mA load	0.04	0.18	0.50	Ω
	$R_{HD\_ON\_LS}$	Low-side nMOS switch on, 300mA load	0.04	0.18	0.50	
H-Bridge Overcurrent-Protection Threshold	I_{HD_OCP}	Rising current through high-side or low-side switch	600	1000	1500	mA
H-Bridge Overcurrent-Protection Threshold Hysteresis	$I_{HD\_OCP\_H}$			130		mA
H-Bridge Thermal-Shutdown Temperature Threshold	T_{HD_SHDN}	Rising temperature		150		°C
H-Bridge Thermal-Shutdown Temperature Threshold Hysteresis	$T_{HD\_SHDN\_H}$			25		°C
PPWM Mode Input Frequency	$f_{HD\_PPWM\_IN}$		10		250	kHz
LRA Resonance Frequency Tracking Range	f_{HD_LRA}	See the *Haptic Driver* section	max(200 k/ IniGss[11:0],100)		min(800 k/ IniGss[11:0],1000)	Hz
Startup Latency	t_{HD_START}	Time from enabling to vibration response		6.5	7.5	ms
BUCK1&2						
Input-Voltage Range	V_{IN}	Input voltage = V_{SYS}	2.7		5.5	V

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Voltage Range	V_{BK_OUT}	10mV step resolution	0.55		1.18	V
		25mV step resolution	0.55		2.125	
		50mV step resolution	0.55		3.7	
Quiescent-Supply Current	I_{Q_BK}	I_{BK_OUT} = 0, V_{SYS} = 3.7V, V_{BK_OUT} = 1.2V, Buck_VStep = 25mV, Buck_FPWM = 0		0.35	0.70	µA
	$I_{Q\_BK\_PWM}$	I_{BK_OUT} = 0, V_{SYS} = 3.7V, V_{BK_OUT} = 1.2V, Buck_FPWM = 1, L = 2.2µH, Buck_ISet = 175mA		2		mA
Shutdown Supply Current with Active Discharge Enabled	I_{SD_BK}	Buck disabled, Buck_ActDsc = 1		60		µA
Output Average Voltage Accuracy	ACC_BK	Buck_IntegDis = 0, CCM operation, V_{BK_OUT} ≤ 3.4V	-2.5		+2.5	%
Peak-to-Peak Voltage Ripple	V_{RPP_BK}	$C_{BK\_OUT\_EFF}$ ≥ 4µF, I_{BK_OUT} = 1mA, L = 2.2µH, Buck_Iset = 150mA, V_{OUT} = 1.2V, V_{SYS} = 3.7V		10		mV
Nominal Peak Current Set Range	I_{PSET_BK}	25mA step resolution	0		375	mA
Load Transient Response	$V_{LOAD\_TRANS\_BK}$	10µA to 300mA at 1A/µs, C_{BK_EFF} = 9µF, V_{BK_OUT} = 1.2V		70		mV
Load Regulation Error	$V_{LOAD\_REG\_BK\_}$	Buck_IAdptDis = 0, Buck_IntegDis = 0 I_{BK_OUT} = 500mA		-0.5		%
Line Regulation Error	$V_{LINE\_REG\_BK\_}$	V_{BK_OUT} = 1.2V, V_{SYS} from 2.7V to 5.5V, I_{BK_OUT} = 200mA, C_{BK_OUT} > 9µF		±5		mV
Maximum Operative Output Current	I_{BK_MAX}	Load regulation error = -5%, Buck_IntegDis = 0	400			mA
Valley Current Limit During Short-Circuit to GND	I_{SHRT_BK}	V_{BK_OUT} = 0V		1		A
Valley Current Limit During Startup	$I_{VLY\_BK\_STUP}$	During startup before PGOOD = 1 condition is achieved		250		mA
BKLX Leakage Current	I_{LK_BKLX}	Buck disabled	-1		+1	µA
Active Discharge Current	I_{ACTD_BK}	V_{BK_OUT} = 0.7V	8	16	28	mA
Passive Discharge Resistance	R_{PSV_BK}		6	10	14	kΩ
Full Turn-On Time	t_{ON_BK}	Time from enable to PGOOD and full current capability. No load. 1 Murata GRM155R60J226ME11 22µF output capacitor		10		ms

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Efficiency	EFFIC_BK	Buck_VSet = 1.2V, I_{BK_OUT} = 10mA, Inductor: Murata DFE201610E-2R2M		86		%
BKLX Rising/Falling Slew Rate	SLW_BK	Buck_LowEMI = 0		3		V/ns
	SLW_BK_L	Buck_LowEMI = 1		0.6		
Thermal Shutdown Threshold	T_{SHDN_BK}			140		°C
BUCK3						
Input-Voltage Range	V_{IN}	Input voltage = V_{SYS}	2.7		5.5	V
Output-Voltage Range	V_{BK3OUT}	10mV step resolution	0.55		1.18	V
		25mV step resolution	0.55		2.125	
		50mV step resolution	0.55		3.7	
Quiescent-Supply Current	I_{Q_BK3}	I_{BK3OUT} = 0, V_{SYS} = 3.7V, V_{BK3OUT} = 3.3V, Buck3FPWM = 0		0.5	0.8	µA
	$I_{Q\_BK3\_PWM}$	I_{BK3OUT} = 0, V_{SYS} = 3.7V, V_{BK3OUT} = 3.3V, Buck3FPWM = 1, L = 2.2µH, Buck3ISet = 175mA		1.5		mA
Shutdown Supply Current with Active Discharge Enabled	I_{SD_BK3}	Buck3 disabled, Buck3ActDsc = 1		60		µA
Output Average-Voltage Accuracy	ACC_BK3	Buck3IntegDis = 0, CCM operation, V_{BK3OUT} ≤ 3.4V	-2.5		+2.5	%
Peak-to-Peak Voltage Ripple	V_{RPP_BK3}	C_{BK3OUT_EFF} ≥ 4µF, I_{BK3OUT} = 1mA; L = 2.2µH; Buck3Iset = 150mA, V_{OUT} = 1.2V, V_{SYS} = 3.7V		10		mV
Nominal Peak Current Set Range	I_{PSET_BK3}	25mA step resolution	0		375	mA
Load Transient Response	$V_{LOAD\_TRANS\_BK3}$	10µA to 300mA at 1A/µs, C_{BK3EFF} = 9µF, V_{BK3OUT} = 1.2V		70		mV
Load Regulation Error	$V_{LOAD\_REG\_BK3}$	Buck3IAdptDis = 0, Buck3IntegDis = 0, I_{BK3OUT} = 500mA		-0.5		%
Line Regulation Error	$V_{LINE\_REG\_BK3}$	V_{BK3OUT} = 3.3V, V_{SYS} from 5.5V to 3.4V, I_{BK3OUT} = 300mA, C_{BK3OUT} > 4µF, LDO mode assistant enabled		±100		mV
Maximum Operative Output Current	I_{BK3_MAX}	Load regulation error = -5%, Buck3IntegDis = 0	600			mA
Valley Current Limit During Short-Circuit to GND	I_{SHRT_BK3}	V_{BK3OUT} = 0V		1.8		A
Valley Current Limit During Startup	$I_{VLY\_BK3\_STUP}$	During startup before PGOOD = 1 condition is achieved		250		mA
BK3LX Leakage Current	I_{LK_BK3LX}	Buck3 disabled			1	µA

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Discharge Current	I_{ACTD_BK3}	V_{BK3OUT} = 0.7V	8	16	28	mA
Passive Discharge Resistance	R_{PSV_BK3}		6	10	14	kΩ
Full Turn-On Time	t_{ON_BK3}	Time from enable to PGOOD and full current capability. No load. 1 Murata GRM155R60J226ME11 22µF output capacitor		10		ms
Efficiency	EFFIC_BK3	Buck3VSet = 3.3V, I_{BK3OUT} = 250mA, Inductor: Murata DFE201610E-2R2M		95		%
BK3LX Rising/Falling Slew Rate	SLW_BK3	Buck3LowEMI = 0		3		V/ns
	SLW_BK3_L	Buck3LowEMI = 1		0.6		
Thermal Shutdown Threshold	T_{SHDN_BK3}			140		°C
Supply vs. BOUT Dropout threshold	$V_{IN\_BOUT\_DROPOUT\_TH\_F}$	Supply falling, Buck3VSet = 3.3V	250	330	400	mV
LDO1 (TYPICAL VALUES ARE AT V_{L1IN}=1.2V, V_{L1OUT}=1V)						
Input Voltage	V_{IN_LDO1}	LDO mode	1		2	V
		Switch mode	0.7		2	
Quiescent-Supply Current	I_{Q_LDO1}	LDO enabled, I_{L1OUT} = 0		1.0	2.2	µA
		LDO enabled, I_{L1OUT} = 0, switch mode		0.35	0.90	
		LDO enabled, I_{L1OUT} = 0, LDO1_MPC0CNT = 1, MPC0 high		0.7	1.5	
Quiescent-Supply Current in Dropout	$I_{Q\_LDO1\_D}$	I_{L1OUT} = 0, V_{L1IN} = 1.2V, LDO1VSet = 0x1D (1.225V)		2.4	4.2	µA
Output Leakage	I_{LK_L1OUT}	V_{L1OUT} = GND, LDO1 disabled		0.015	2.5	µA
Shutdown Supply Current with Active Discharge Enabled	I_{SD_LDO1}	LDO1 disabled, LDO1ActDsc = 1		50		µA
Maximum Output Current	I_{L1OUT_MAX}		50			mA
Output-Voltage Range	V_{L1OUT}	25mV step resolution	0.50		1.95	V
Output-Voltage Accuracy	ACC_LDO1	(V_{L1OUT} + 0.2V) ≤ V_{L1IN} ≤ 2V, I_{L1OUT} = 1mA	-3.25		+3.25	%
Dropout Voltage	V_{DROP_LDO1}	V_{L1IN} = 1V, I_{L1OUT} = 50mA, LDO1VSet = 1V			70	mV
Line-Regulation Error	$V_{LINEREG\_LDO1}$	V_{L1IN} = (V_{L1OUT} + 0.2V) to 2V	-0.4		+0.4	%/V
Load-Regulation Error	$V_{LOADREG\_LDO1}$	I_{L1OUT} = 100µA to 50mA		0.003	0.013	%/mA

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Line Transient	$V_{LINETRAN\_LDO1}$	V_{L1IN} = +1V to +2V, 200ns rise time		±45		mV
		V_{L1IN} = +1V to +2V, 1µs rise time		±25		
Load Transient	$V_{LOADTRAN\_LDO1}$	I_{L1OUT} = 0 to 10mA, 200ns rise time		80		mV
		I_{L1OUT} = 0mA to 50mA, 200ns rise time		130		
Passive-Discharge Resistance	R_{PD_LDO1}		5	10	15	kΩ
Active-Discharge Current	I_{AD_LDO1}		7	25	55	mA
Switch Mode Resistance	R_{ON_LDO1}	V_{L1IN} = 1V, I_{L1OUT} = 50mA			1.1	Ω
	$R_{ON\_LDO1\_0p7}$	V_{L1IN} = 0.7V, I_{L1OUT} = 1mA			2.7	
Turn-On Time	t_{ON_LDO1}	I_{L1OUT} = 0, time from 10%–90% of final value		0.38		ms
	$t_{ON\_LDO1\_SW}$	I_{L1OUT} = 0, time from 10%–90% of final value, switch mode		0.065		
	t_{ON_LDO1}	I_{L1OUT} = 0mA, LDO1_MPC0CNT = 1, time from MPC0 rising to 90% of L1OUT final value, C_{L1OUT} = 10nF		580		ns
Short-Circuit Current Limit	I_{SHRT_LDO1}	V_{L1IN} = 1.2V, V_{L1OUT} = GND		400	1000	mA
		V_{L1IN} = 1.2V, V_{L1OUT} = GND, switch mode		305	1000	
Thermal-Shutdown Temperature	T_{SHDN_LDO1}			150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_LDO1\_H}$			10		°C
L1IN UVLO	V_{UVLO_LDO1}	V_{L1IN} falling	0.53	0.77		V
		V_{L1IN} rising		0.78	1.00	
Output Noise	V_{NOISE_LDO1}	10Hz to 100kHz, V_{L1IN} = 2V, V_{L1OUT} = 1.8V		120		$µV_{RMS}$
		10Hz to 100kHz, V_{L1IN} = 2V, V_{L1OUT} = 1.0V		95		
		10Hz to 100kHz, V_{L1IN} = 2V, V_{L1OUT} = 0.5V		70		
LDO2 (ALWAYS ON LDO, TYPICAL VALUES ARE AT V_{L2IN} = +3.7V, V_{L2OUT} = +3V)						
Input Voltage	V_{IN_LDO2}	LDO mode	1.71		5.5	V
		Switch mode	1.2		5.5	
Quiescent-Supply Current	I_{Q_LDO2}	LDO enabled, I_{L2OUT} = 0µA		1.0	1.9	µA
	IQ_LDO2_SW	LDO enabled, I_{L2OUT} = 0µA, switch mode		0.35	0.9	

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent-Supply Current in Dropout	$I_{Q\_LDO2\_D}$	I_{L2OUT} = 0µA, V_{L2IN} = 2.9V, LDO2VSet = 0x15 (+3V)			1.9	3.7	µA
Shutdown-Supply Current with Active Discharge Enabled	I_{SD_LDO2}	LDO2 disabled, LDO2ActDSC = 1			55		µA
Maximum Output Current	I_{L2OUT_MAX}	V_{L2IN} > 1.8V		100			mA
		V_{L2IN} ≤ 1.8V		50			
Maximum Output Current when Supplied from V_{CCINT}	$I_{L2OUT\_MAX\_VCCINT}$	V_{BAT} > 3.2V, V_{L2OUT} = 1.8V, LDO2Supply = internal (see Table 8)		100			µA
Internal-Supply Switch	R_{ON_L2IN}	LDO2Supply = internal (see Table 8), switch between V_{CCINT} and L2IN		4.5	7.3	11	kΩ
Output-Voltage Range	V_{L2OUT}	100mV step resolution		0.9		4.0	V
Output-Voltage Accuracy	ACCLDO2	V_{L2IN} = (V_{L2OUT} + 0.5V) or higher, I_{L2OUT} = 1mA		-2.7		+2.7	%
Dropout Voltage	V_{DROP_LDO2}	V_{L2IN} = 3.0V, LDO2VSet = 3.1V, I_{L2OUT} = 100mA				100	mV
		V_{L2IN} = 1.85V, LDO2VSet = 1.9V, I_{L2OUT} = 100mA				130	
Line-Regulation Error	$V_{LINEREG\_LDO2}$	V_{L2IN} = (V_{L2OUT} + 0.5V) to 5.5V, V_{L2IN} ≥ 1.8V		-0.4		+0.4	%/V
Load-Regulation Error	$V_{LOADREG\_LDO2}$	+1.8V ≤ V_{L2IN} ≤ +5.5V, I_{L2OUT} = 100µA to 100mA			0.002	0.007	%/mA
Line Transient	$V_{LINETRAN\_LDO2}$	V_{L2IN} = 4V to 5V, 200ns rise time			±35		mV
		V_{L2IN} = 4V to 5V, 1µs rise time			±25		
Load Transient	$V_{LOADTRAN\_LDO2}$	200ns rise time	I_{L2OUT} = 0mA to 10mA		100		mV
			I_{L2OUT} = 0mA to 100mA		200		
Passive Discharge Resistance	R_{PD_LDO2}			5	10	15	kΩ
Active Discharge Current	I_{AD_LDO2}	V_{L2IN} = 3.7V		8	22	40	mA
Switch-Mode Resistance	R_{ON_LDO2}	I_{L2OUT} = 100mA, switch mode	V_{L2IN} = 2.7V		0.4	0.7	Ω
	$R_{ON\_LDO2\_1p8}$		V_{L2IN} = 1.8V, I_{L2OUT} = 100mA, switch mode		0.65	1	
	$R_{ON\_LDO2\_sw}$	I_{L2OUT} = 5mA, switch mode	V_{L2IN} = 1.2V		1.5	2.3	

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-On Time	t_{ON_LDO2}	I_{L2OUT} = 0mA, time from 10% to 90% of final value			1.5		ms
			Switch mode		0.26		
Short-Circuit Current Limit	I_{SHRT_LDO2}	V_{L2OUT} = GND	V_{L2IN} = 5.5V	225	460	650	mA
	$I_{SHRT\_LDO2\_SW}$		V_{L2IN} = 2.7V, switch mode	210	350	540	
Thermal-Shutdown Temperature	T_{SHDN_LDO2}				150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_LDO2\_H}$				20		°C
L2IN UVLO	V_{UVLO_LDO2}	V_{L2IN} falling		1.05	1.35		V
		V_{L2IN} rising			1.36	1.69	
Output Noise	V_{NOISE_LDO2}	10Hz to 100kHz, V_{L2IN} = 5V, V_{L2OUT} = 3.3V			150		$µV_{RMS}$
		10Hz to 100kHz, V_{L2IN} = 5V, V_{L2OUT} = 2.5V			125		
		10Hz to 100kHz, V_{L2IN} = 5V, V_{L2OUT} = 1.2V			90		
		10Hz to 100kHz, V_{L2IN} = 5V, V_{L2OUT} = 0.8V			80		
Ouput Leakage	I_{LK_L2OUT}	V_{L2OUT} = GND, LDO2 disabled		-1		+1	µA
BUCK-BOOST							
Input Voltage	V_{BBIN}	Input voltage = V_{SYS}		2.7		5.5	V
Output Voltage Set Range	V_{BBOUT}	50mV step resolution, do not exceed the valid voltage range		2.6		5.5	V
Quiescent Supply Current	I_{Q_BB}	I_{BBOUT} = 0, V_{BBOUT} = 5V			2	4	µA
Shutdown Supply Current with Active Discharge Enabled	I_{SD_BB}	Buck-boost disabled, BBstActDsc = 1			60		µA
Maximum Output Operative Power	P_{MAX_BBOUT}	BBstIAdptDis = 0, V_{BBIN} ≥ 3.2V, V_{BBOUT} ≥ 3.2V, 7.5% load regulation (Note 3)		1.5			W
Load-Regulation Error	LOAD_REG_ERR	BBstIAdptDis = 0, BBstVSet > 3.3V, P_{OUT} = 1.5W			-3.5		%
Average Output-Voltage Accuracy	ACC_BBOUT	I_{BBOUT} = 1mA, C_{BBOUT_EFF} ≥ 5µF		-3		3	%
Maximum Output Current During Startup	$I_{LOAD\_MAX\_STUP}$	V_{BBIN} > 3V, BBstIAdptDis = 0		85			mA
Startup Time	t_{STUP}	I_{LOAD} < $I_{LOAD\_MAX\_STUP}$, time from V_{BBOUT} = 0V to final value			13		ms

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Supply Current During Startup	I_{BBIN_STUP}	V_{BBIN} = 3.6V, V_{BBOUT} = 5V, C_{BBOUT_EFF} = 10µF, I_{BBOUT} = 0		10		mA
Output UVLO Threshold	V_{BBOUT_UVLO}	Falling edge (50mV hysteresis)		1.85	2.46	V
HVLX Leakage Current	I_{LK_BBHVLX}		-1		+1	µA
LVLX Leakage Current	I_{LK_BBLVLX}		-1		+1	µA
Passive Discharge Resistance	R_{PSV_BB}		5	10	17	kΩ
Active Discharge Current	I_{ACTD_BB}	V_{BBOUT} = 2.5V	5	20	50	mA
BBOUT Pulldown Current	$I_{PD\_BB\_E}$	BBst Enabled; BBstVSet = 4V; V_{BBOUT} = 4.1V		300		nA
Thermal Shutdown Temp	T_{SHDN_BB}			150		°C
HV BOOST						
Input-Voltage Range	V_{BSTIN}	Input voltage = V_{SYS}	2.7		5.5	V
Output-Voltage Range	V_{BSTOUT}	250mV step resolution	5		20	V
Output-Voltage UVLO	V_{BSTOUT_UVLO}	V_{BSTOUT} - V_{SYS} falling	-2.7	-2.2	-1.6	V
Quiescent-Supply Current	I_{Q_BST}	I_{BSTOUT} = 0, V_{SYS} = 3.7V, BstVSet = 5V, T_A = 25°C		2.4	9	µA
		I_{BSTOUT} = 0, V_{SYS} = 3.7V, BstVSet = 5V			106	
Output-Average Voltage Accuracy	ACC_BST	I_{BSTOUT} = 1mA, V_{HVOUT} < 13V	-4		+2	%
Peak-to-Peak Voltage Ripple	V_{RPP_BST}	BstISet = 350mA, BstVSet = 12V, C_{BSTOUT_EFF} = 10µF, L_{BSTOUT} = 4.7µH, I_{BSTOUT} = 1mA		5		mV
Peak Current-Set Range	I_{PSET_BST}	25mA step resolution	100		475	mA
DC Load Regulation Error	$V_{LOAD\_REG\_BST}$	BstVSet = 12V, I_{BSTOUT} = 25mA, BstISet = 300mA, BstIAdptEn = 1		0.3		%
DC Line Regulation Error	$V_{LINE\_REG\_BST}$	BstVSet = 6.5V, V_{SYS} from 2.7V to 5.5V		4		mV
BSTOUT Pulldown Resistance	R_{BSTOUT}	-3% Load Regulation Error		10		MΩ
True Shutdown PMOS On-Resistance	R_{ON_TS}	I_{BSTOUT} = 100mA		0.15	0.22	Ω
Boost Freewheeling NMOS On-Resistance	$R_{ONBST\_FRWHL\_N}$	I_{BSTOUT} = 100mA		0.45	0.7	Ω
Boost NMOS On-Resistance	R_{ONBST_N}	BstFETScale = 0, I_{BSTOUT} = 100mA		0.55	0.9	Ω
	R_{ONBST_NFS}	BstFETScale = 1, I_{BSTOUT} = 100mA		1.1	1.8	

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Schottky Diode Forward Voltage	$V_{BE\_SCHOTTKY}$	I_{BSTOUT} = 100mA, $V_{BSTHVLX}$ - V_{BSTOUT}	0.2	0.4	0.6	V
Freewheeling On-Resistance	R_{ONBST_FRWHL}	I_{BSTOUT} = 100mA		50	80	Ω
Minimum t_{ON}	$t_{ON\_BST\_MIN}$			65		ns
Max Switching Frequency	FREQ_BST_MX	V_{BSTOUT} regulation error = -150mV, BstISet = 100mA, BstIAdptEn = 0	1.7	3.5	5.5	MHz
Max Peak Current Setting Extra Budget with BstIAdptEn = 1	ΔI_{P_MAX}	BstIAdptEn = 1, V_{BSTOUT} regulation error = -200mV	150	250	450	mA
Short-Circuit Current Limit Difference vs. Peak Current Setting	ΔI_{BST_SHRT}	BstIAdptEn = 0	130	200	250	mA
BSTHVLX Leakage	$I_{LK\_BSTHVLX}$	Boost disabled			1	µA
BSTLVLX Leakage	$I_{LK\_BSTLVLX}$	Boost disabled			1	µA
Passive Discharge Resistance	R_{BSTPSV}			10		kΩ
Linear BSTOUT Precharge Current	$I_{L\_BSTOUT\_PRCH}$	V_{BSTOUT} from 0V to V_{SYS} - 0.4V	5	12.5	20	mA
Switching Precharge Inductor Current	$I_{SW\_BSTOUT\_PRCH}$	V_{BSTOUT} from V_{SYS} - 0.4V to final regulation voltage		13		mA
Full Turn-On Time	$t_{ON\_BST\_MIN}$	Time from enable to full current capability		100		ms
Efficiency	EFFIC_12	BstVSet = 12V, I_{BSTOUT} = 20mA, BstISet = 300mA, Inductor = Murata DFE201610E-4R7M		85		%
	EFFIC_15	BstVSet = 15V, I_{BSTOUT} = 2mA, BstISet = 300mA, Inductor = Murata DFE201610E-4R7M		83		
	EFFIC_5	BstVSet = 5V, I_{BSTOUT} = 10µA, BstISet = 150mA, Inductor = Murata DFE201610E-4R7M		76		
	EFFIC_6P5	BstVSet = 6.5V, I_{BSTOUT} = 10µA, BstISet = 150mA, Inductor = Murata DFE201610E-4R7M		73		
BHVLX Rising/Falling Slew Rate	SLW_BSTHVLX			2		V/ns
Thermal Shutdown Threshold	T_{SHDN_BST}			140		°C
CHARGE PUMP						
Input Voltage	V_{CPIN}	Input voltage = V_{SYS}	2.7		5.5	V

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent-Supply Current	$I_{Q\_CP\_5V}$	I_{CPOUT} = 0μA, CPVSet = 5V		2	3.5	μA
	$I_{Q\_CP\_6.6V}$	I_{CPOUT} = 0μA, CPVSet = 6.6V		2.2	4.3	
CPOUT Output Voltage	V_{CPOUT}	CPVSet = 0, I_{CPOUT} = 10μA, V_{SYS} > 3.3V		6.6		V
		CPVSet = 1, I_{CPOUT} = 10μA		5		
Output Accuracy	ACC_CP	I_{CPOUT} < 120μA, V_{SYS} > 3.3V	-3		+3	V
Maximum Operative Output Current	I_{CPOUT_MAX}	V_{SYS} > 3.3V, -5% load regulation error	250			μA
Efficiency	EFF_CP	CPVSet = 6.6V, I_{OUT} = 10μA, V_{SYS} = 3.7V		79		%
Max Charge-Pump Frequency	FREQ_CP		89	100	114	kHz
Passive-Discharge Resistance	R_{PSV_CP}			10		kΩ
LOAD SWITCHES 1 AND 2 (TYPICAL VALUES ARE AT V_{LSW_IN} = 1.2V)						
Input Voltage	V_{SW_IN}		0.65		5.50	V
Quiescent-Supply Current	$I_{Q\_SW\_}$	Load switch on, voltage protection enabled		0.80	1.20	μA
		Load switch on, voltage protection disabled		0.26	0.45	
On-Resistance	$R_{SW\_}$	V_{SYS} = 3V, V_{SW_IN} = 1.2V, I_{SW_OUT} = 50mA		0.5	0.85	Ω
Startup Current	I_{SW_START}	V_{LSW_IN} = 1.2V, V_{LSW_OUT} = 0V initially		50	108	mA
Voltage Protection Threshold	V_{SW_PROT}	Rising		130	260	mV
		Falling	10	120		
Turn-On Time	$t_{ON\_SW\_}$	V_{LSW_IN} = 1.2V, 1μF output capacitance, 10% to 90% out		15		μs
Startup Time-Out Time	t_{STUP_LSW}			5		ms
Startup Retry Time	$t_{RETRY\_LSW\_}$			5		ms
Passive Discharge Resistance	$R_{PSV\_LSW\_}$			10		kΩ
Active Discharge Current	$I_{ACTD\_LSW\_}$			20		mA
Output Leakage	$I_{LK\_LSW\_}$	LSW_OUT = GND, load switch disabled			1	μA
LED CURRENT SINKS						
Maximum Input Voltage	$V_{IN\_LED\_MAX}$				20	V
Quiscent Current	I_{Q_LED}	All LEDs on, V_{SYS} = 3.7V		245	370	μA

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Sink Setting Range	I_{LED_RNG}	LEDIStep = 0.6mA steps	0.6		15	mA
		LEDIStep = 1mA steps	1		25	
		LEDIStep = 1.2mA steps	1.2		30	
LED Current Accuracy	ACC_LED	$I_{LED\_}$ = 13mA, T_A = +25°C, $V_{LED\_}$ = +0.7V to +20V	-2		+2	%
		$I_{LED\_}$ = 13mA, $V_{LED\_}$ = +0.7V to +20V	-5		+5	
		$I_{LED\_}$ = 0.6mA to 30mA, T_A = +25°C, $V_{LED\_}$ = +0.7V to +20V	-5		+5	
		$I_{LED\_}$ = 0.6mA to 30mA, $V_{LED\_}$ = +0.7V to +20V	-6		+6	
LED Dropout Voltage	V_{LED_DROP}	I_{LED_SET} = 5mA, $I_{LED\_}$ = 0.9 x 5mA		110	160	mV
		I_{LED_SET} = 25mA, $I_{LED\_}$ = 0.9 x 25mA		145	215	
		I_{LED_SET} = 30mA, $I_{LED\_}$ = 0.9 x 30mA		175	270	
Leakage in Shutdown	I_{LK_LED}	$V_{LED\_}$ = +20V			0.1	µA
Open-LED Detection Threshold	V_{LED_DET}	LED_ enabled, LEDIStep = 0.6mA steps, falling edge	61	92	140	mV
VBSTOUT Loop Max Voltage	LED_LOOP_VMAX	5V < BstVSet < 15V, LED_BoostLoop = 1, VLED0 = GND		V_{BSTOUT} + 5		V
VLED0 Loop Regulation Voltage	VLED0_LOOP_REG	LED_BoostLoop = 1, LED0_REFSEL = 00	190	200	210	mV
		LED_BoostLoop = 1, LED0_REFSEL = 01	290	300	310	
		LED_BoostLoop = 1, LED0_REFSEL = 10	385	400	415	
		LED_BoostLoop = 1, LED0_REFSEL = 11	485	500	515	
FUEL GAUGE (REFER TO MAX17260 FOR DETAILS) / POWER SUPPLY						
FGBAT UVLO Threshold	V_{FGBAT_UVLO}	V_{FGBAT} rising, V_{CHGIN} present		2.25	2.28	V
		V_{FGBAT} falling, V_{CHGIN} present	2.16	2.19		
Shutdown Supply Current	I_{DD0}			0.5		µA
Hibernate Supply Current	I_{DD1}	Average current		5.5		µA
Active Supply Current	I_{DD2}	Average current not including thermistor measurement current		12.5		µA
Startup Voltage	$V_{FGBATSU}$				3.05	V
FUEL GAUGE (REFER TO MAX17260 FOR DETAILS) / ANALOG-TO-DIGITAL CONVERSION						
FGBAT Measurement Error	V_{GERR}	T_A = +25°C	-7.5		+7.5	mV
		-40°C ≤ T_A ≤ +85°C	-20		20	

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FGBAT Measurement Resolution	V_{LSB}			78.125		μV
FGBAT Measurement Range	V_{FS}		2.3		4.9	V
Current-Measurement Offset Error	I_{OERR}	Long-term average without load current		±1.5		μV
Current-Measurement Error	I_{GERR}		-1		+1	% of Reading
Current-Measurement Resolution	I_{LSB}			1.5625		μV
Current-Measurement Range	I_{FS}			±51.2		mV
Internal Temperature-Measurement Error	TI_{GERR}	-40°C ≤ T_A ≤ +85°C		±1		°C
Internal Temperature-Measurement Resolution	TI_{LSB}			0.00391		°C
FUEL GAUGE (REFER TO MAX17260 FOR DETAILS) / INPUT/OUTPUT						
External Thermal Resistance	R_{EXT10}	Config.R100 = 0		10		kΩ
	R_{EXT100}	Config.R100 = 1		100		
Output Drive Low, $\overline{ALRT}$, SDA	V_{OL}	I_{OL} = 4mA, V_{BATT} = 2.3V			0.4	V
Input Logic High, $\overline{ALRT}$, SCL, SDA	V_{IH}		1.5			V
Input Logic Low, $\overline{ALRT}$, SCL, SDA	V_{IL}				0.5	V
Battery-Detach Detection Threshold	V_{DET}	Measured as a fraction of V_{FGBAT} on THM rising	91.0	96.2	99.0	%
Battery-Detach Detection Threshold Hysteresis	$V_{DET-HYS}$	Measured as a fraction of V_{FGBAT} on THM falling		1.6		%
Battery-Detach Comparator Delay	t_{OFF}	THM step from 70% to 100% of V_{FGBAT} (Alrtp = 0, EnAIN = 1, FTHRM = 1)			100	μs
FUEL GAUGE (REFER TO MAX17260 FOR DETAILS) / LEAKAGE						
Leakage Current, CSN, CSPH, $\overline{ALRT}$	I_{LEAK}	$V_{\overline{ALRT}}$ < 15V	-1		+1	μA
FUEL GAUGE (REFER TO MAX17260 FOR DETAILS) / TIMING						
Time-Base Accuracy	t_{ERR}	T_A = +25°C	-1		+1	%
TH Precharge Time	t_{PRE}		8.48			ms

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL						
SDA, SCL, MPC_, PFN_, RST, INT Input-Leakage Current	I_{LK_IO}	Input pullup/pulldown resistances disabled, V_{IO} = 0V to 5.5V	-1		+1	μA
SDA, SCL, MPC_ Input-Logic High	V_{IO_IH}		1.4			V
SDA, SCL, MPC_ Input-Logic Low	V_{IO_IL}				0.4	V
PFN_ Input-Logic High	$V_{PFN\_IH\_C}$	OFF/SEAL mode		0.7 x V_{CCINT}		V
PFN_ Input-Logic Low	$V_{PFN\_IL\_C}$	OFF/SEAL mode		0.3 x V_{CCINT}		V
PFN_ Input-Logic High	$V_{PFN\_IH\_T}$	ON mode	1.4			V
PFN_ Input-Logic Low	$V_{PFN\_IL\_T}$	ON mode			0.4	V
MPC_, PFN_ Input-Pullup Resistance	R_{IO_PU}	Pullup resistance to V_{CCINT} (Note 2)		170		kΩ
MPC_, PFN_ Input-Pulldown Resistance	R_{IO_PD}			170		kΩ
MPC_ Output Logic-High	V_{IO_OH}	I_{OH} = 1mA, MPC_ configured as push-pull output, pullup voltage is V_{BK1OUT}	V_{BK1OUT} - 0.4			V
SDA, MPC_, PFN_, RST, INT Output Logic Low	V_{IO_OL}	I_{OL} = 4mA			0.4	V
MPC6 Harvester Disable Pullup Resistor	$R_{MPC6\_HARV\_DIS\_RPU}$	Harvester interaction enabled, pull-up resistor to V_{CCINT} (Note 2)		4		kΩ
SCL Clock Frequency	f_{SCL}	(Note 4)	0		400	kHz
Bus Free-Time Between STOP and START Condition	t_{BUF}		1.3			μs
Hold Time for a Repeated START Condition	t_{HD_STA}		0.6			μs
Setup Time for a Repeated START Condition	t_{SU_STA}		0.6			μs
Low Period of SCL Clock	t_{LOW}	(Note 5)	1.3			μs
High Period of SCL Clock	t_{HIGH}		0.6			μs
Data-Hold Time	t_{HD_DAT}	(Notes 6, 7)	0		0.9	μs
Data-Setup Time	t_{SU_DAT}		100			ns

Electrical Characteristics (continued)

(V_{BAT} = V_{FGBAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 8)	50			ns
SPI						
SCLK Frequency	f_{SCLK}				10	MHz
$\overline{CS}$ Setup Time	t_{CS}		10			ns
$\overline{CS}$ Hold Time	t_{CH}		100			ns
$\overline{CS}$ Pulse-Width High	t_{IDLE}			60		ns
DIN Setup Time	t_{DS}		10			ns
DIN Hold Time	t_{DH}		20			ns
SCLK Pulse-Width Low	t_{LOW_SPI}		20			ns
SCLK Pulse-Width High	t_{HIGH_SPI}		20			ns

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: V_{CCINT} is an internal supply generated from either BAT or CAP. Its voltage is determined by the following:
IF: [(V_{CHGIN} > V_{CHGIN_DET} AND V_{CAP} > V_{CAP_DET}) OR V_{CAP} > (V_{BAT} + $V_{THSWOVER}$)]
THEN: V_{CCINT} = V_{CAP}
ELSE: V_{CCINT} = V_{BAT}
where $V_{THSWOVER}$ = 0mV–300mV

Note 3: Guaranteed by design, not production tested.

Note 4: Timing must be fast enough to prevent the Fuel Gauge from entering shutdown mode due to bus low for a period greater than the shutdown timer setting.

Note 5: The SCL waveform must meet the minimum clock low time plus the rise/fall times.

Note 6: The maximum t_{HD_DAT} has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

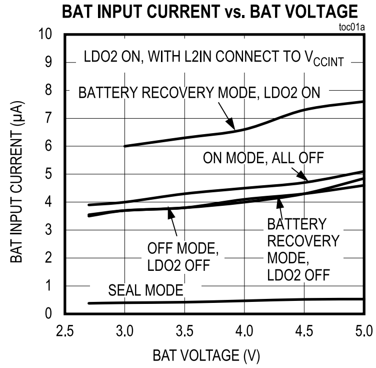
Note 7: This device internally provides a hold time of at least 100ns for the SDA signal (refer to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 8: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

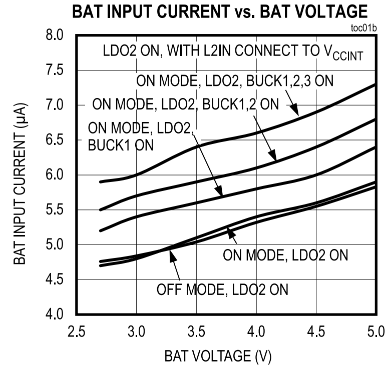
Typical Operating Characteristics

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25ºC, unless otherwise noted.)

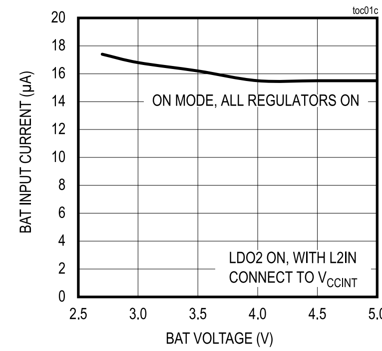
BAT INPUT CURRENT vs. BAT VOLTAGE



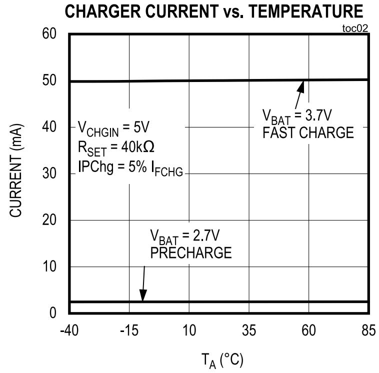
BAT INPUT CURRENT vs. BAT VOLTAGE



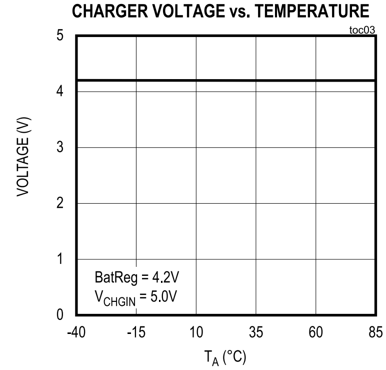
BAT INPUT CURRENT vs. BAT VOLTAGE



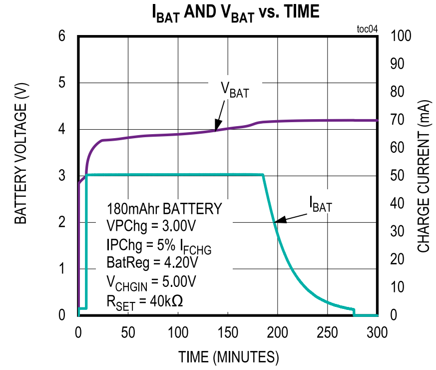
CHARGER CURRENT vs. TEMPERATURE



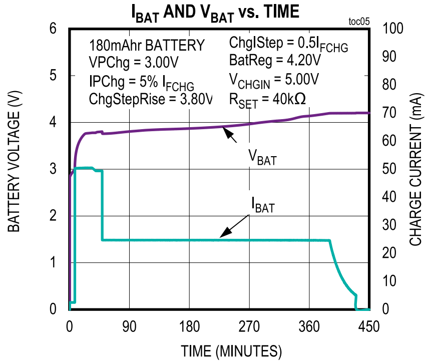
CHARGER VOLTAGE vs. TEMPERATURE



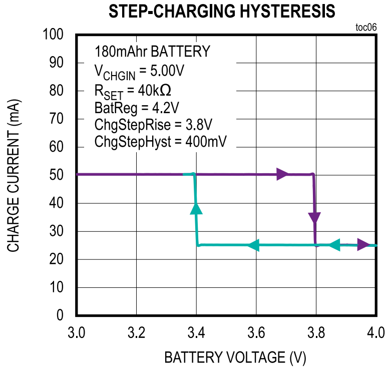
CHARGER PROFILE
I_{BAT} AND V_{BAT} vs. TIME



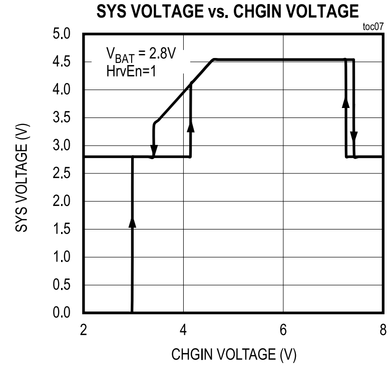
STEP-CHARGING CHARGER PROFILE
I_{BAT} AND V_{BAT} vs. TIME



STEP-CHARGING HYSTERESIS



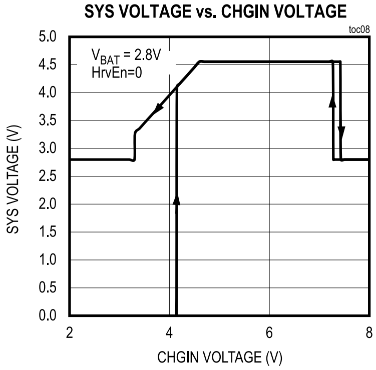
SYS VOLTAGE vs. CHGIN VOLTAGE



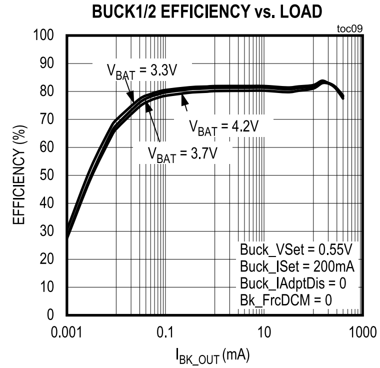
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH, T_A = +25°C, unless otherwise noted.)

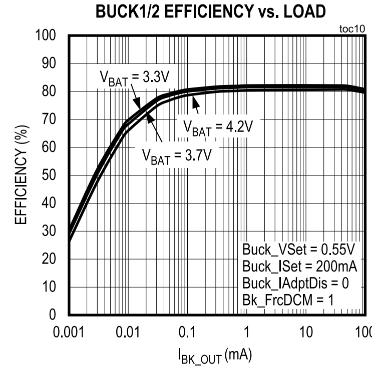
SYS VOLTAGE vs. CHGIN VOLTAGE



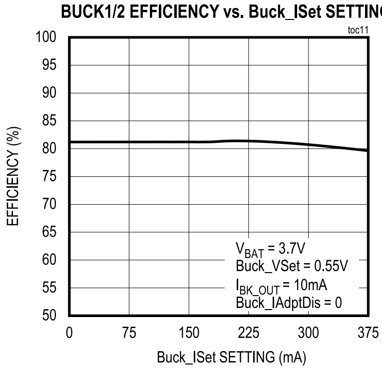
BUCK1/2 EFFICIENCY vs. LOAD



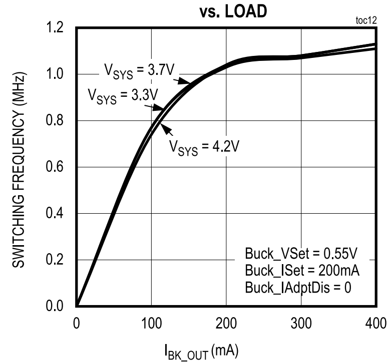
BUCK1/2 EFFICIENCY vs. LOAD



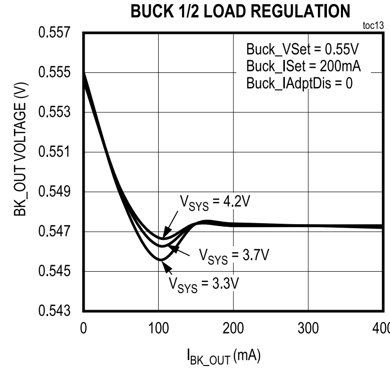
BUCK1/2 EFFICIENCY vs. Buck_ISet SETTING



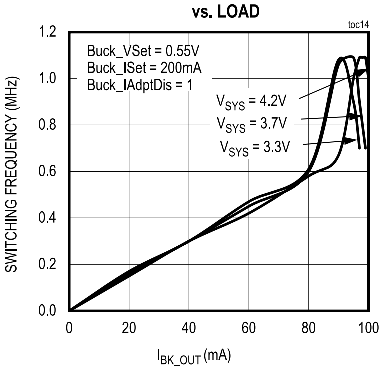
BUCK 1/2 SWITCHING FREQUENCY vs. LOAD



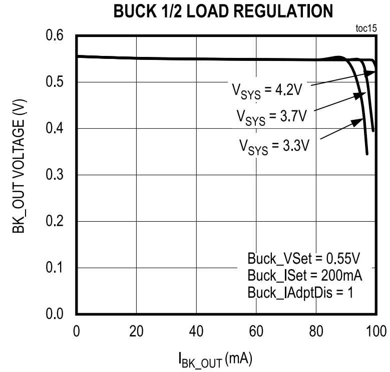
BUCK 1/2 LOAD REGULATION



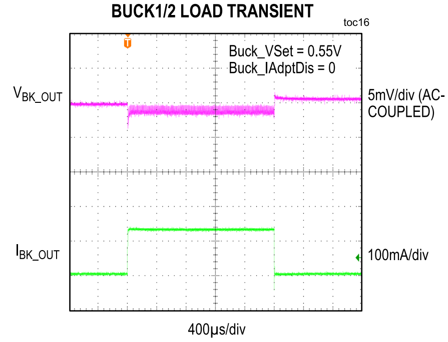
BUCK 1/2 SWITCHING FREQUENCY vs. LOAD



BUCK 1/2 LOAD REGULATION



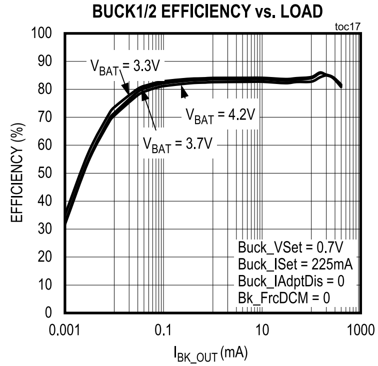
BUCK1/2 LOAD TRANSIENT



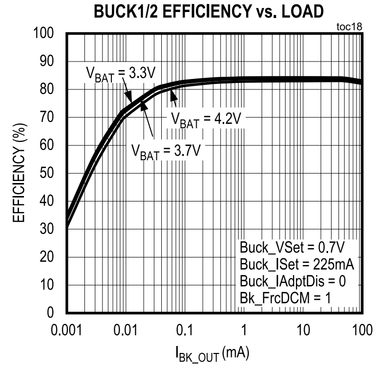
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

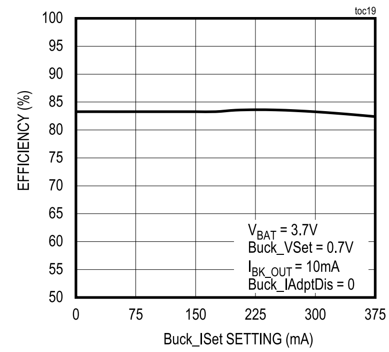
BUCK1/2 EFFICIENCY vs. LOAD



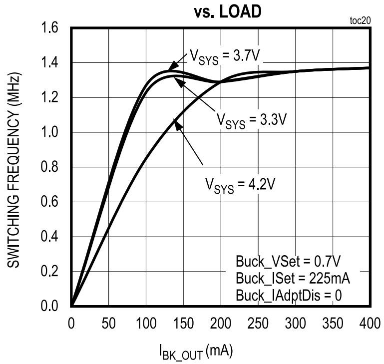
BUCK1/2 EFFICIENCY vs. LOAD



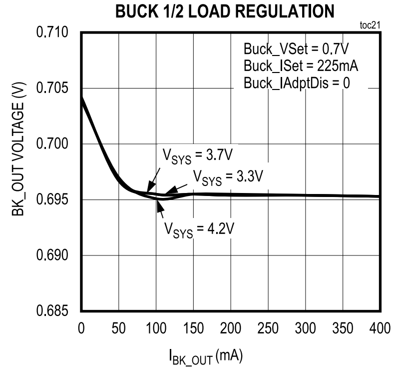
BUCK1/2 EFFICIENCY vs. Buck_ISet SETTING



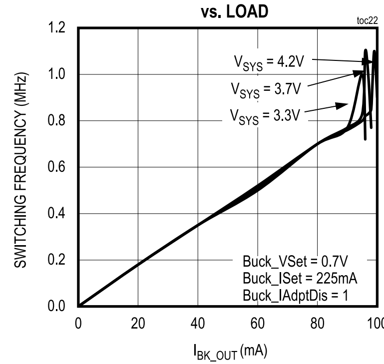
BUCK 1/2 SWITCHING FREQUENCY vs. LOAD



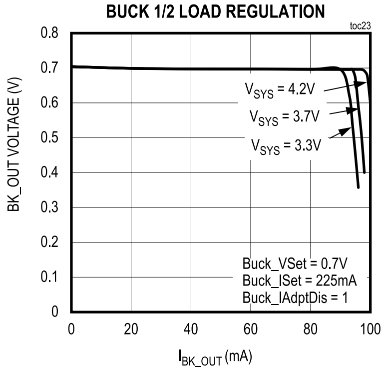
BUCK 1/2 LOAD REGULATION



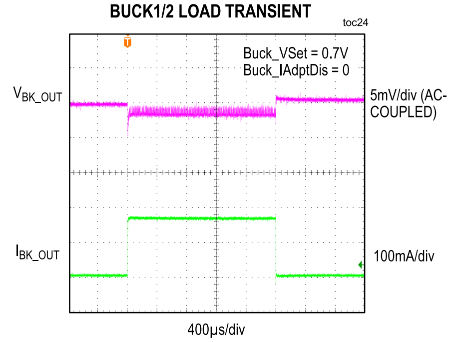
BUCK 1/2 SWITCHING FREQUENCY vs. LOAD



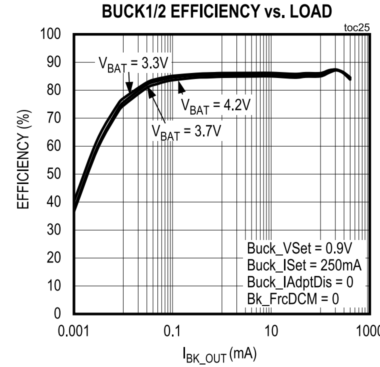
BUCK 1/2 LOAD REGULATION



BUCK1/2 LOAD TRANSIENT

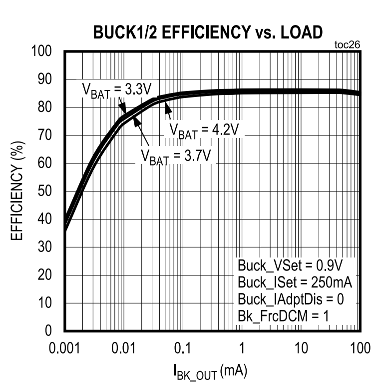


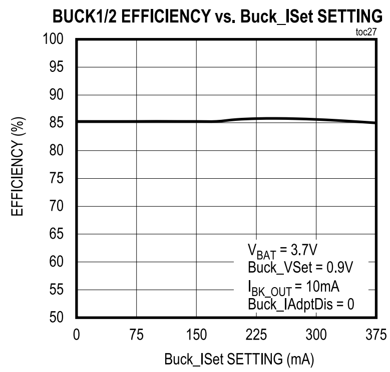
BUCK1/2 EFFICIENCY vs. LOAD

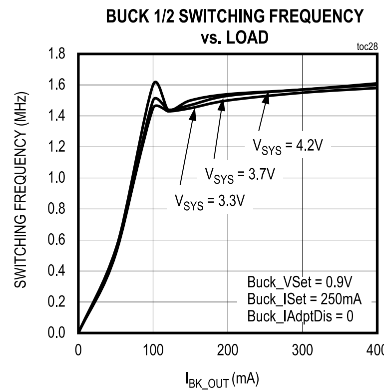


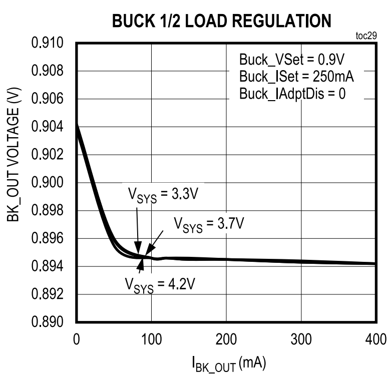
Typical Operating Characteristics (continued)

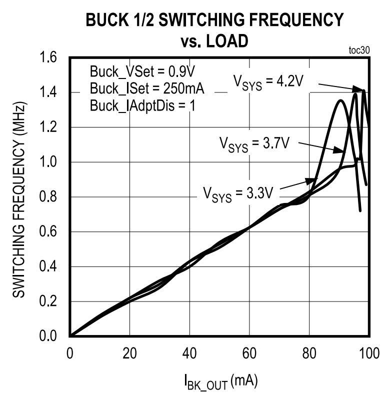
(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

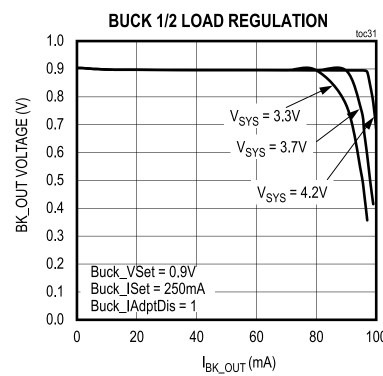


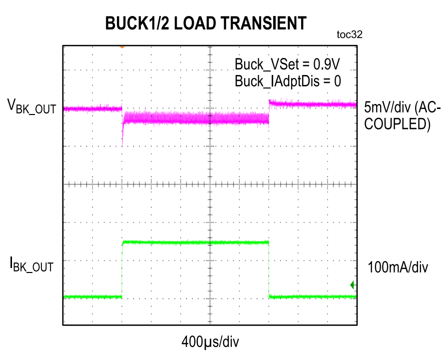


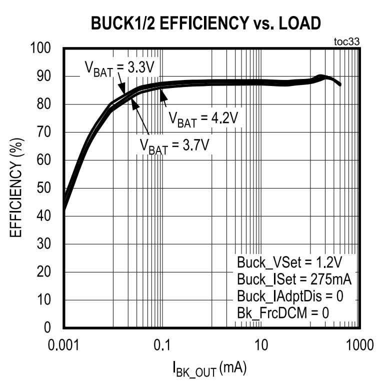


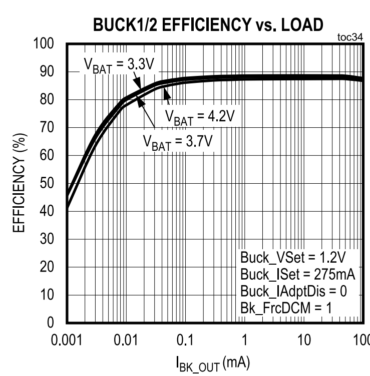






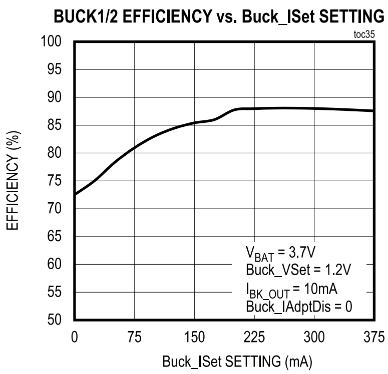


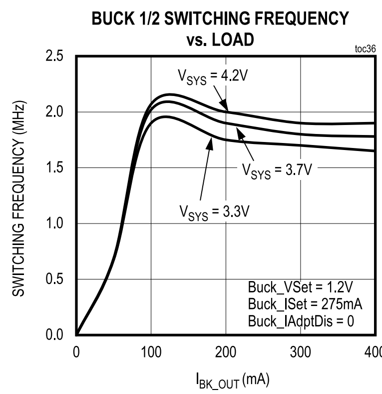


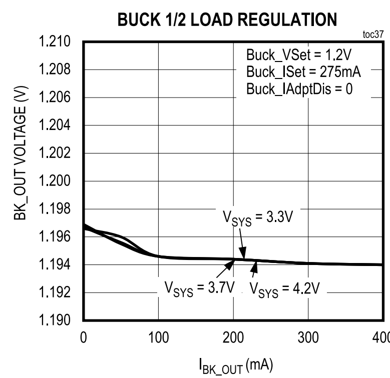


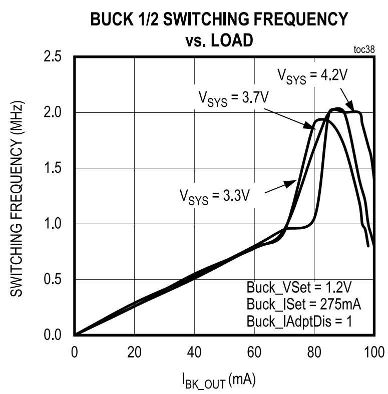
Typical Operating Characteristics (continued)

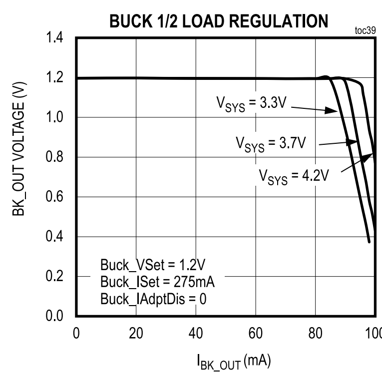
(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH, T_A = +25ºC, unless otherwise noted.)

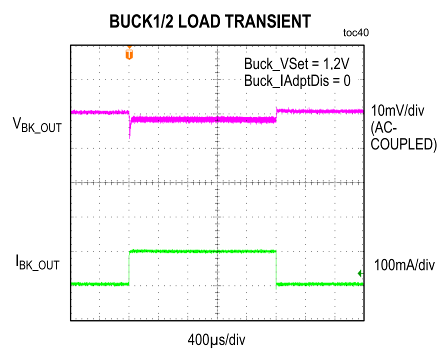


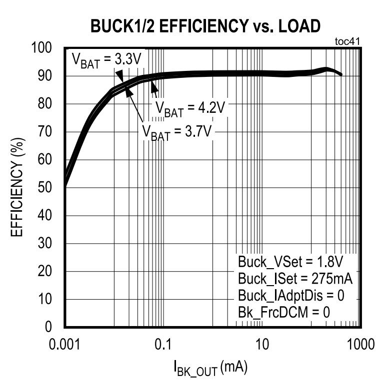


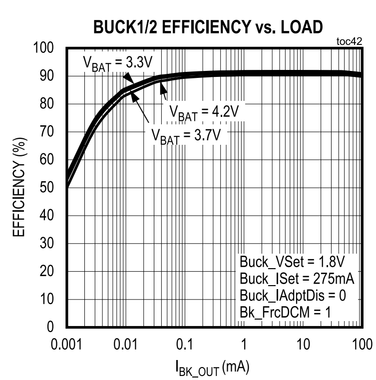


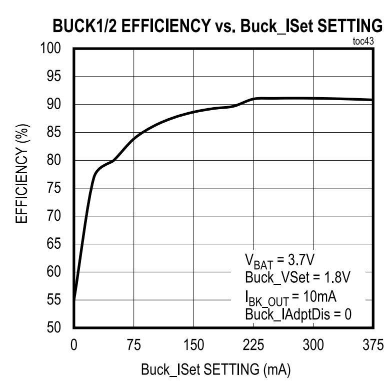








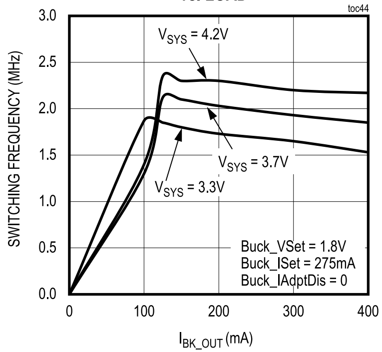




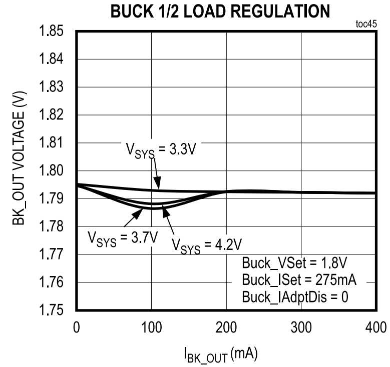
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

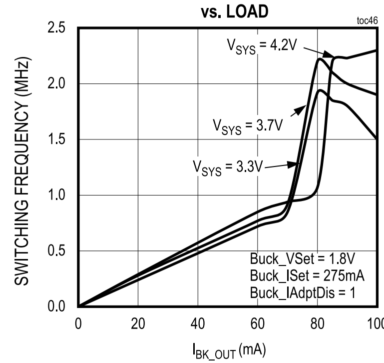
BUCK 1/2 SWITCHING FREQUENCY vs. LOAD



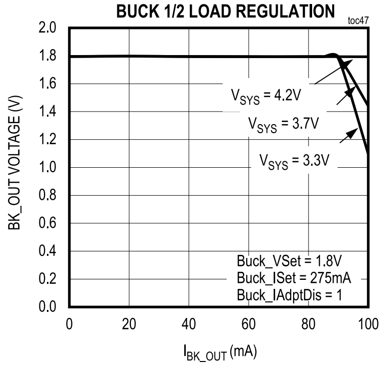
BUCK 1/2 LOAD REGULATION



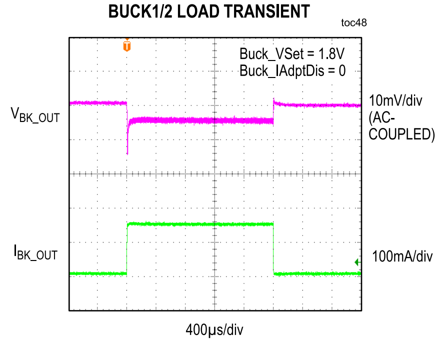
BUCK 1/2 SWITCHING FREQUENCY vs. LOAD



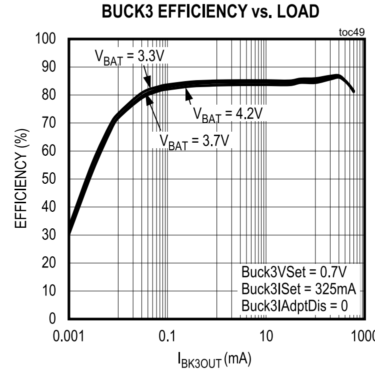
BUCK 1/2 LOAD REGULATION



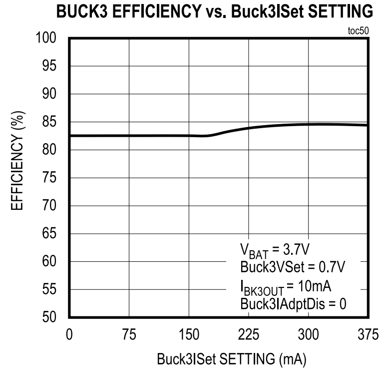
BUCK1/2 LOAD TRANSIENT



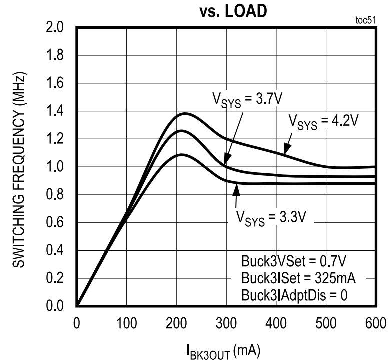
BUCK3 EFFICIENCY vs. LOAD



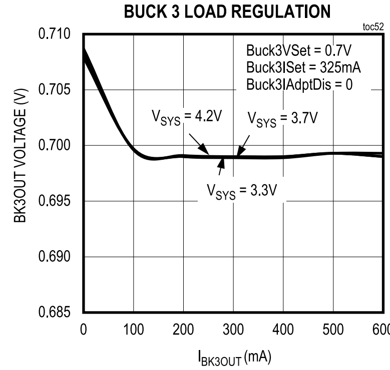
BUCK3 EFFICIENCY vs. Buck3ISet SETTING



BUCK 3 SWITCHING FREQUENCY vs. LOAD

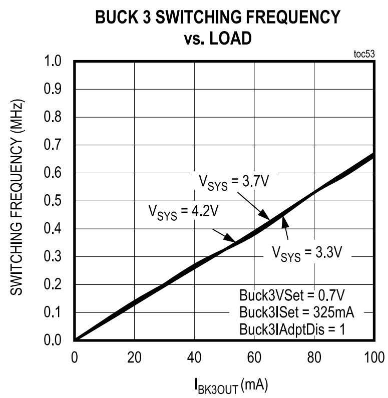


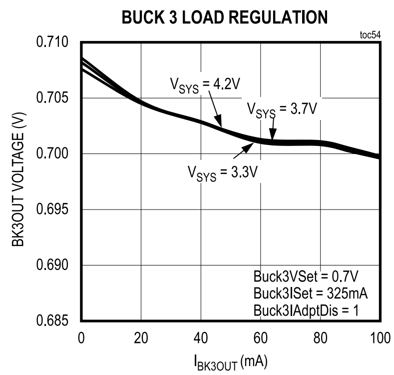
BUCK 3 LOAD REGULATION

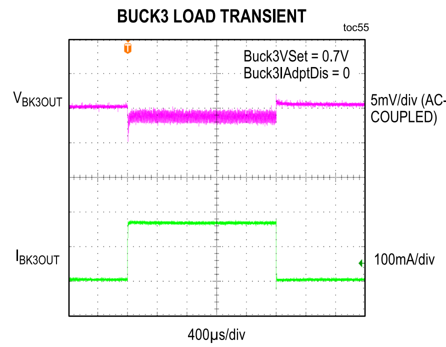


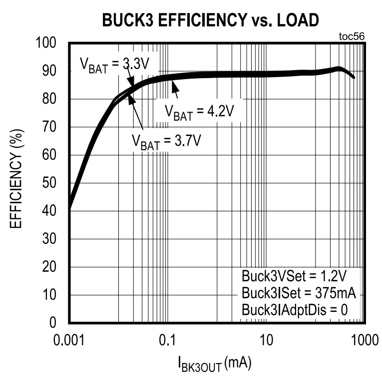
Typical Operating Characteristics (continued)

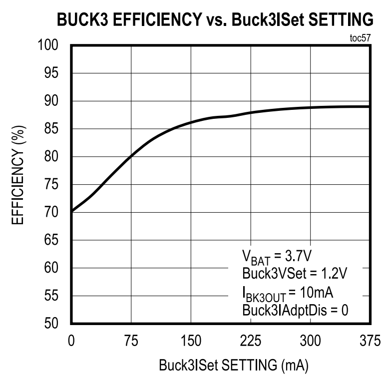
(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

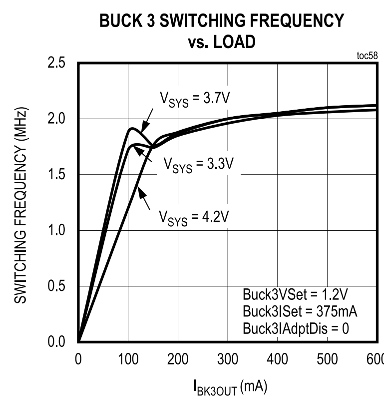


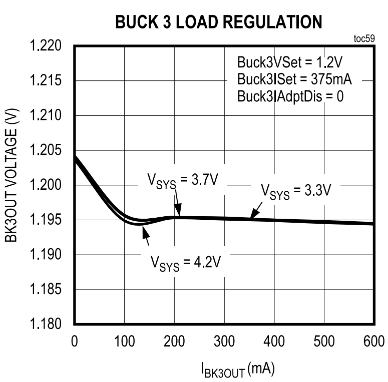


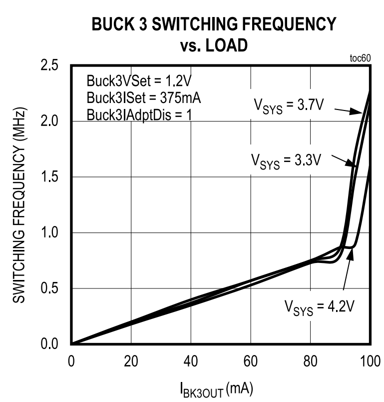


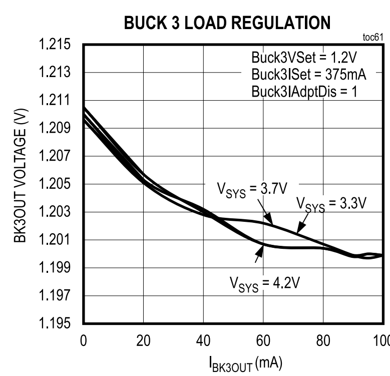






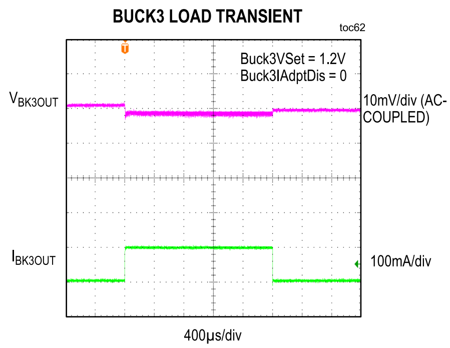


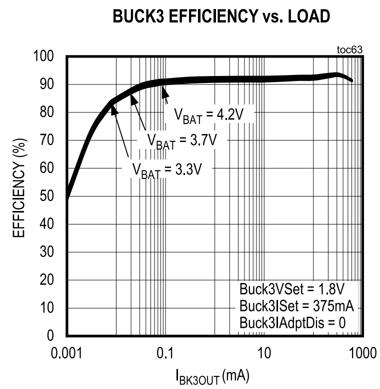


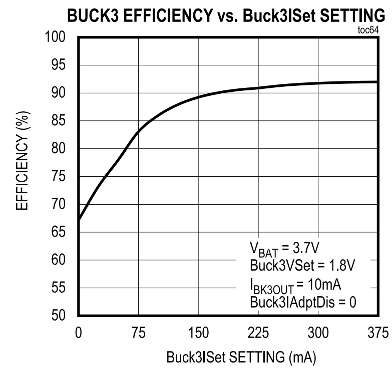


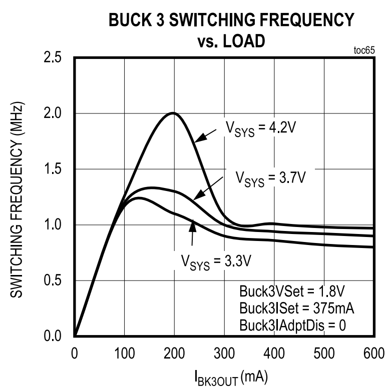
Typical Operating Characteristics (continued)

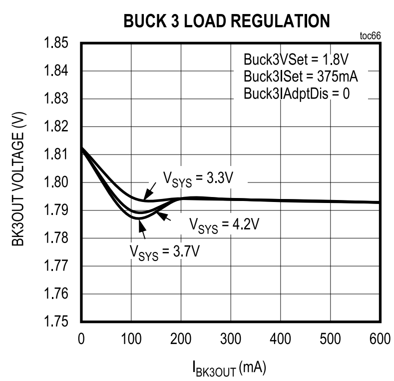
(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

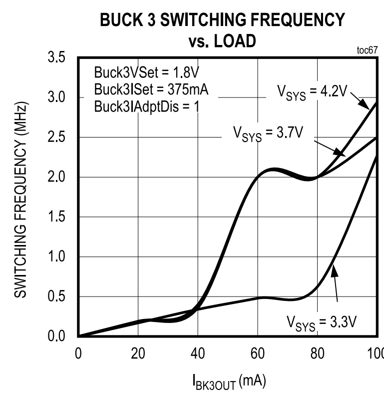


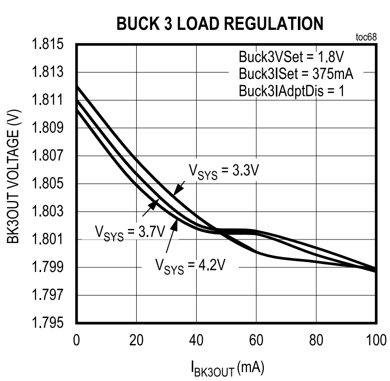


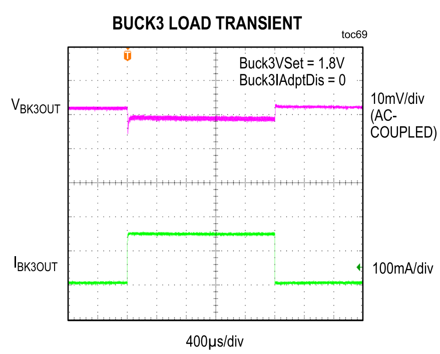


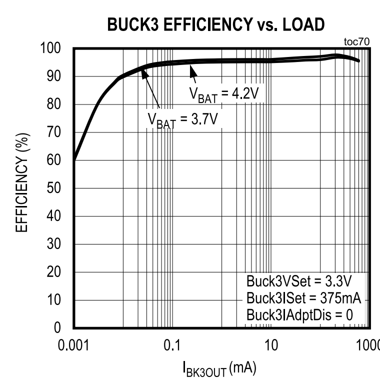








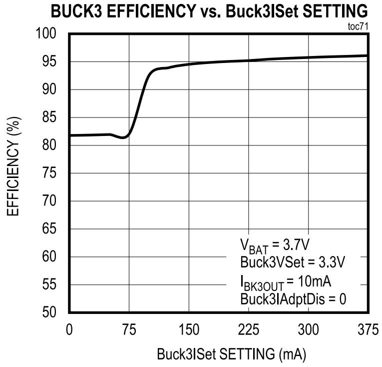




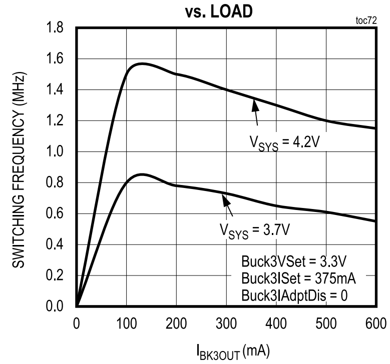
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

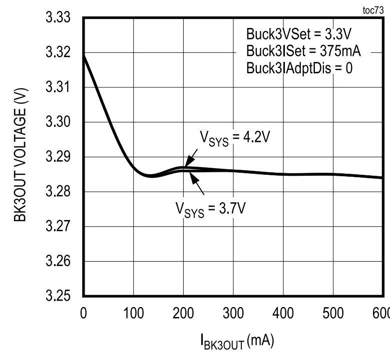
BUCK3 EFFICIENCY vs. Buck3ISet SETTING



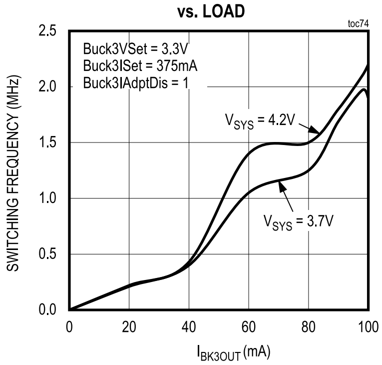
BUCK 3 SWITCHING FREQUENCY vs. LOAD



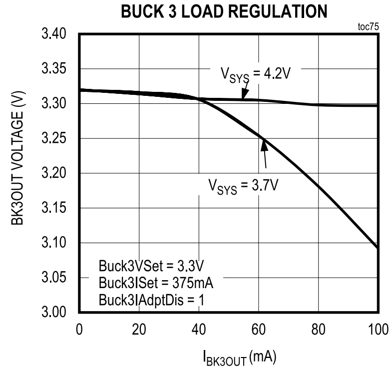
BUCK 3 LOAD REGULATION



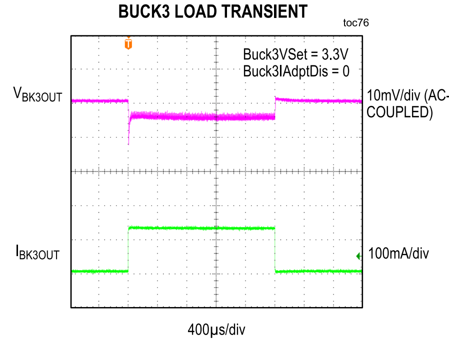
BUCK 3 SWITCHING FREQUENCY vs. LOAD



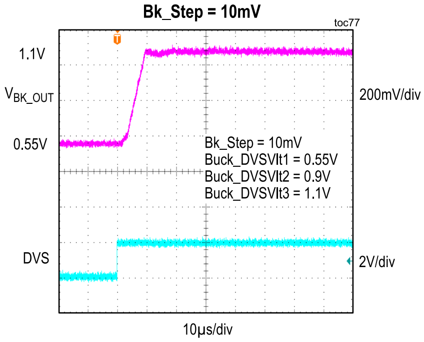
BUCK 3 LOAD REGULATION



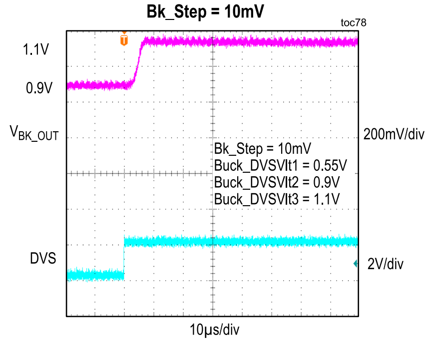
BUCK3 LOAD TRANSIENT



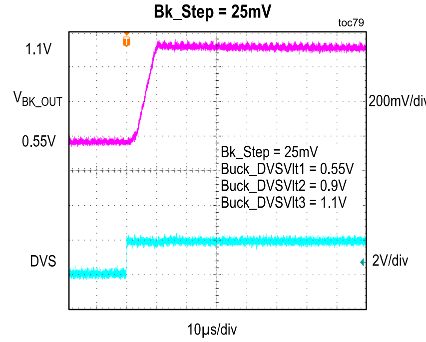
BUCK DVS MODE 1 TRANSITION
Bk_Step = 10mV



BUCK DVS MODE 1 TRANSITION
Bk_Step = 10mV

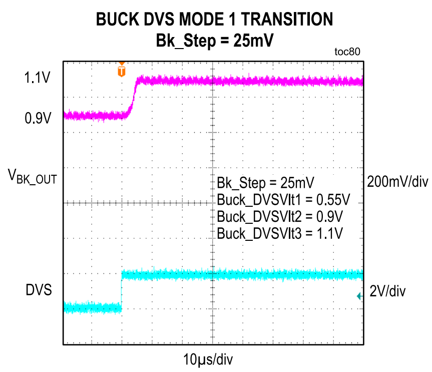


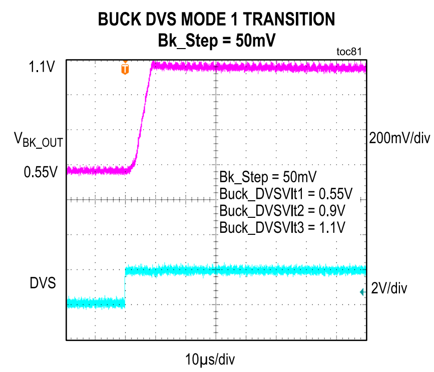
BUCK DVS MODE 1 TRANSITION
Bk_Step = 25mV

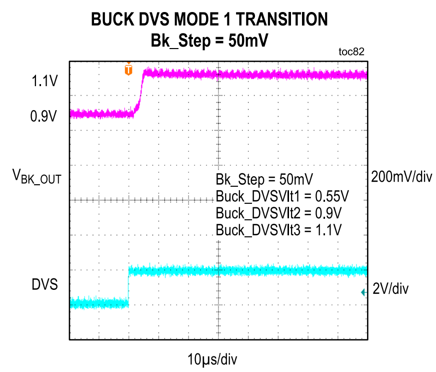


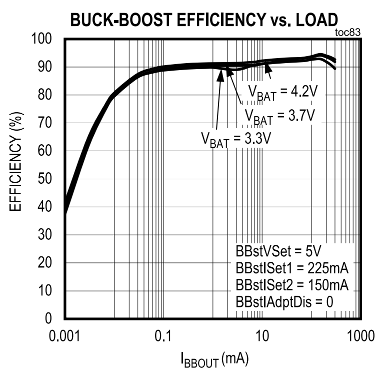
Typical Operating Characteristics (continued)

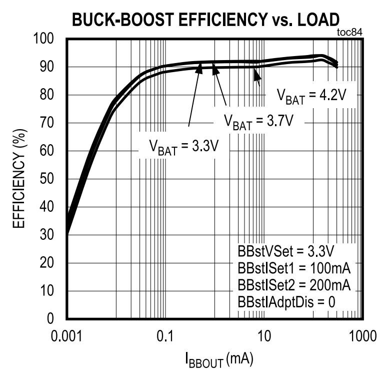
(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

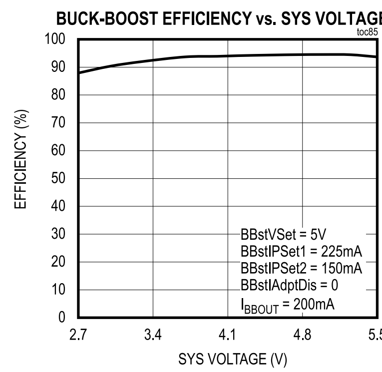


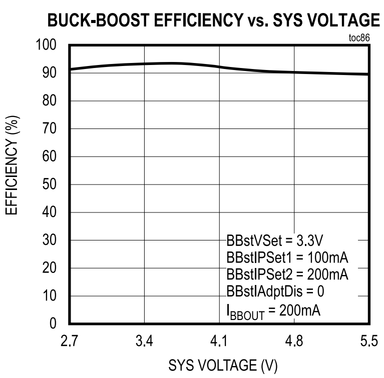


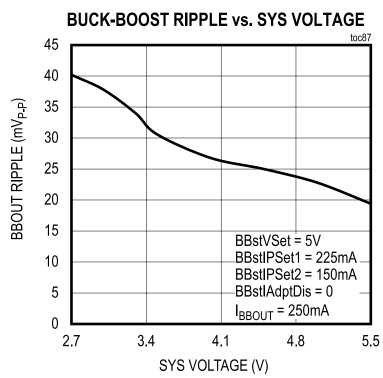


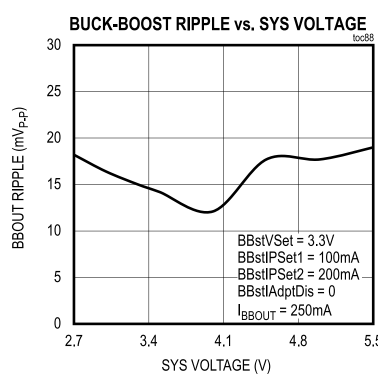








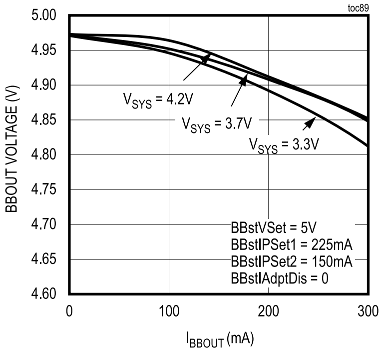




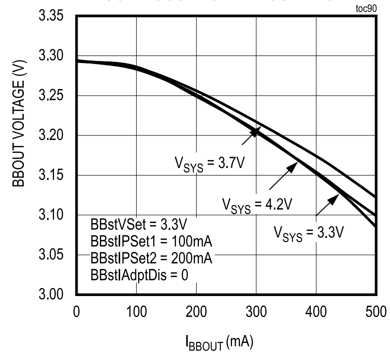
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1μF, C_{VDIG_EFF} = 1μF, C_{CAP_EFF} = 1μF, C_{SYS_EFF} = 10μF, C_{BAT_EFF} = 1μF, $C_{BK\_OUT\_EFF}$ = 10μF, C_{L_IN} = 1μF, $C_{L\_OUT\_EFF}$ = 1μF, C_{BBOUT_EFF} = 8.8μF, C_{BSTOUT_EFF} = 10μF, L_{BK_OUT} = 2.2μH, L_{BBOUT} = 2.2μH, L_{BSTOUT} = 4.7μH, T_A = +25°C, unless otherwise noted.)

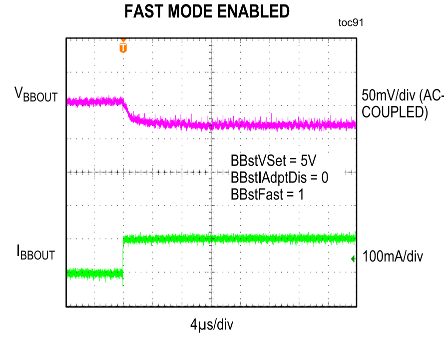
BUCK-BOOST LOAD REGULATION



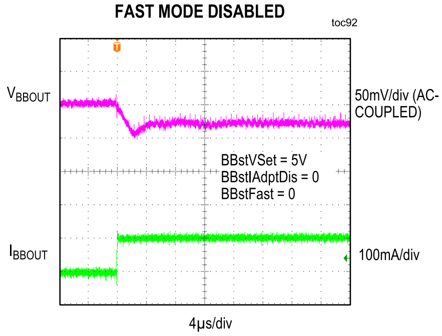
BUCK-BOOST LOAD REGULATION



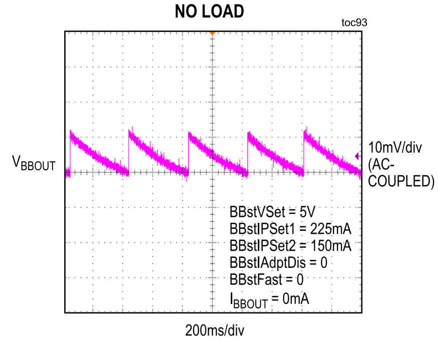
BUCK-BOOST LOAD TRANSIENT FAST MODE ENABLED



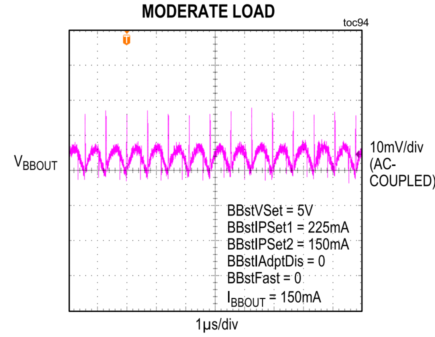
BUCK-BOOST LOAD TRANSIENT FAST MODE DISABLED



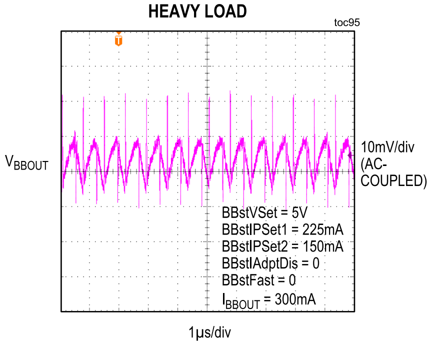
BUCK-BOOST RIPPLE NO LOAD



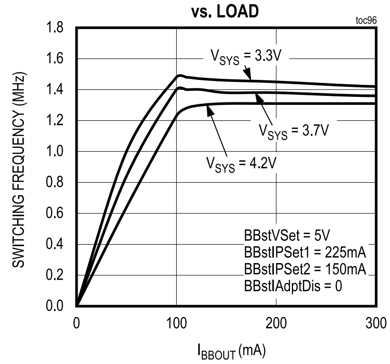
BUCK-BOOST RIPPLE MODERATE LOAD



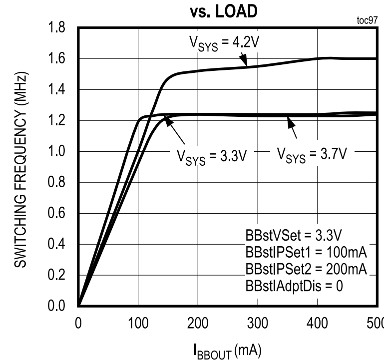
BUCK-BOOST RIPPLE HEAVY LOAD



BUCK-BOOST SWITCHING FREQUENCY vs. LOAD



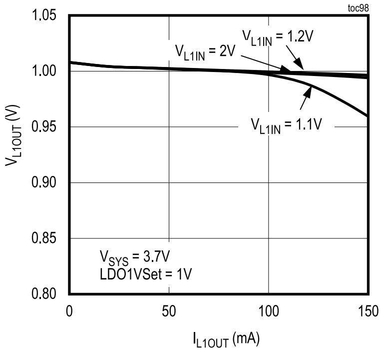
BUCK-BOOST SWITCHING FREQUENCY vs. LOAD



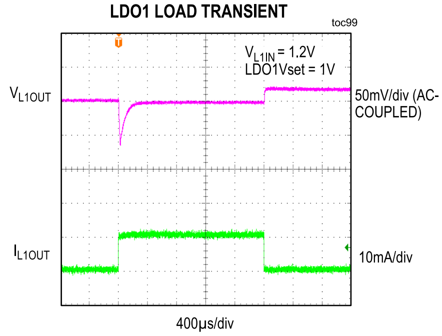
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

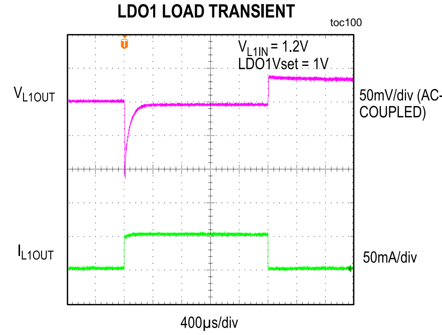
LDO1 LOAD REGULATION



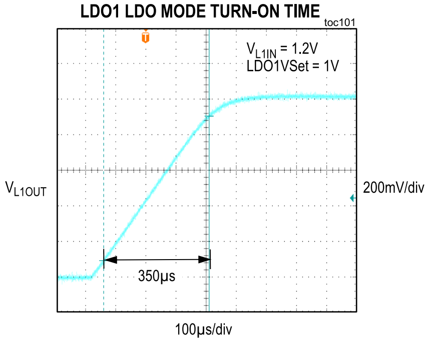
LDO1 LOAD TRANSIENT



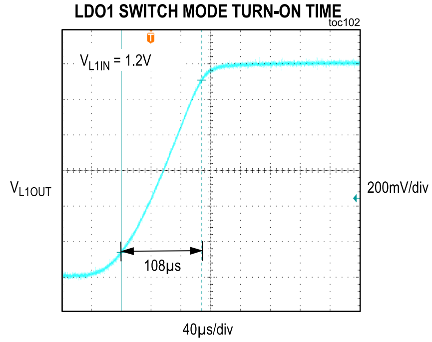
LDO1 LOAD TRANSIENT



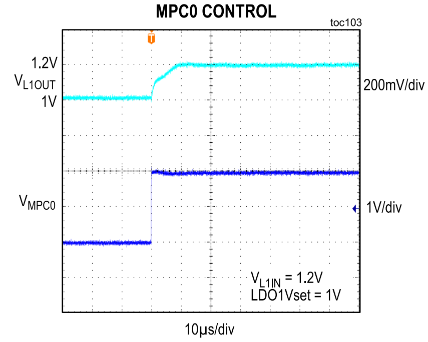
LDO1 LDO MODE TURN-ON TIME



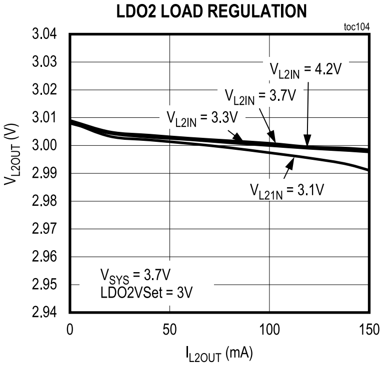
LDO1 SWITCH MODE TURN-ON TIME



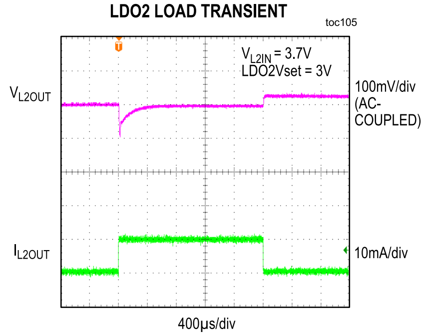
LDO1 LDO MODE TO SWITCH MODE MPC0 CONTROL



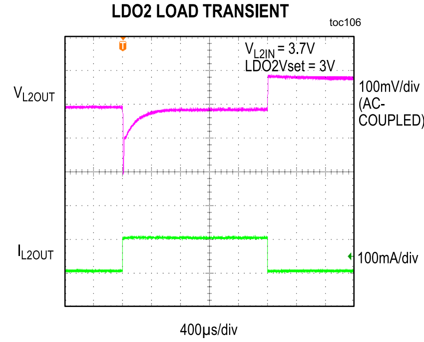
LDO2 LOAD REGULATION



LDO2 LOAD TRANSIENT



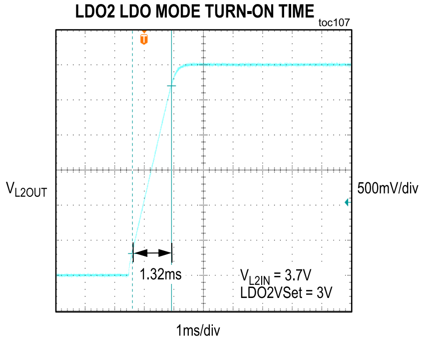
LDO2 LOAD TRANSIENT



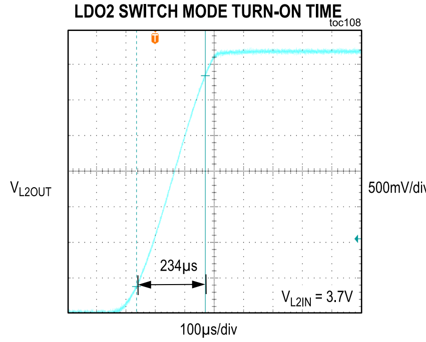
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

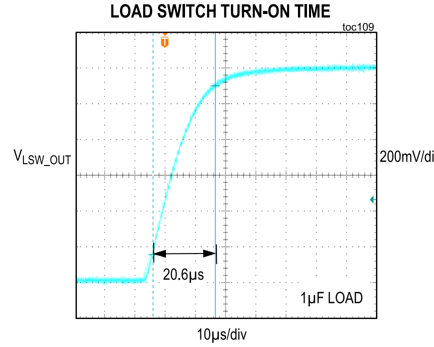
LDO2 LDO MODE TURN-ON TIME



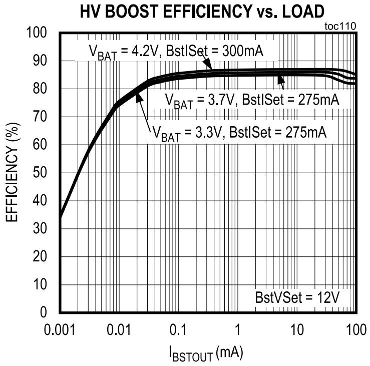
LDO2 SWITCH MODE TURN-ON TIME



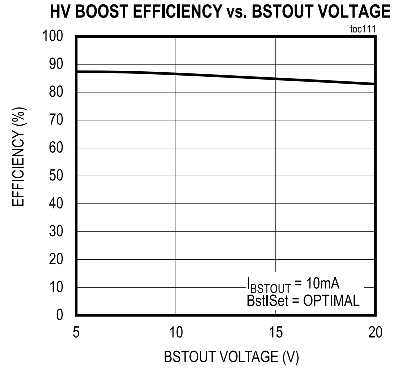
LOAD SWITCH TURN-ON TIME



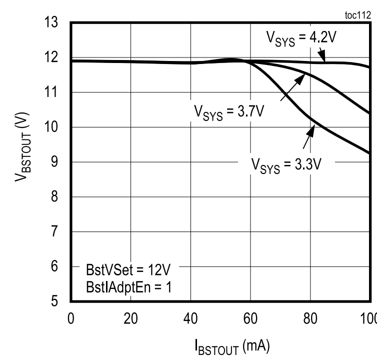
HV BOOST EFFICIENCY vs. LOAD



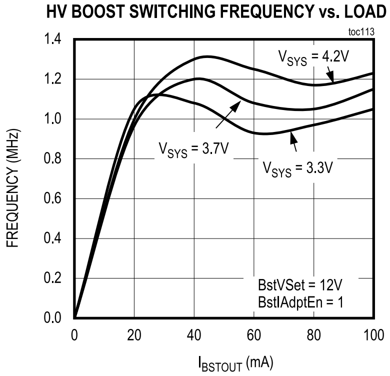
HV BOOST EFFICIENCY vs. BSTOUT VOLTAGE



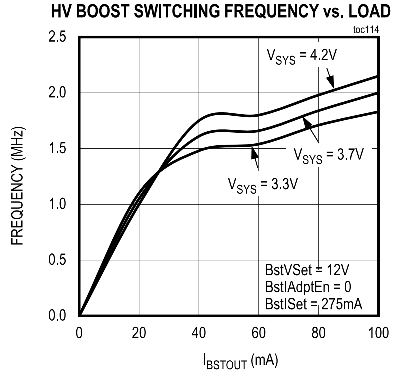
HV BOOST LOAD REGULATION



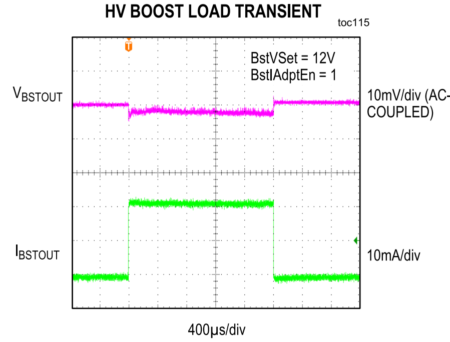
HV BOOST SWITCHING FREQUENCY vs. LOAD



HV BOOST SWITCHING FREQUENCY vs. LOAD



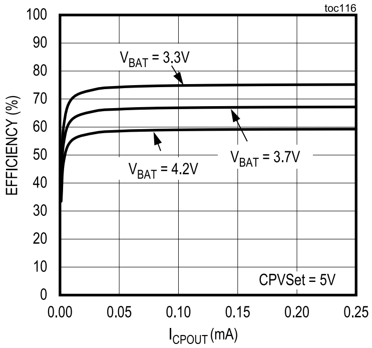
HV BOOST LOAD TRANSIENT



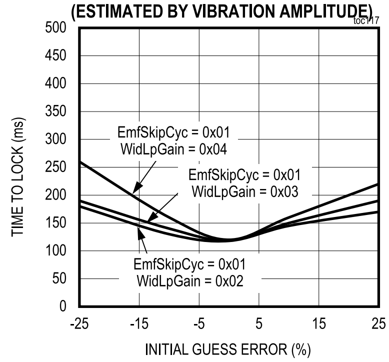
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

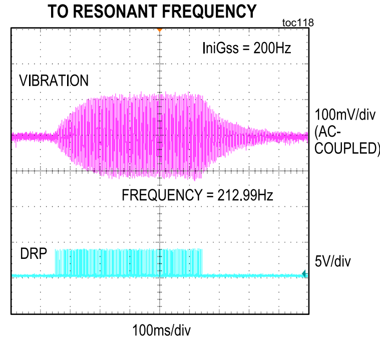
CHARGE PUMP EFFICIENCY vs. LOAD



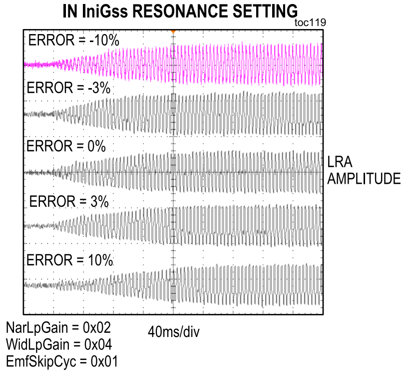
TIME TO RESONANCE LOCK vs. INITIAL GUESS ERROR (ESTIMATED BY VIBRATION AMPLITUDE)



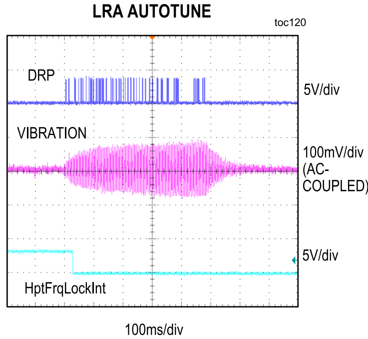
HAPTIC DRIVER LRA AUTOTUNE IniGss CLOSE TO RESONANT FREQUENCY



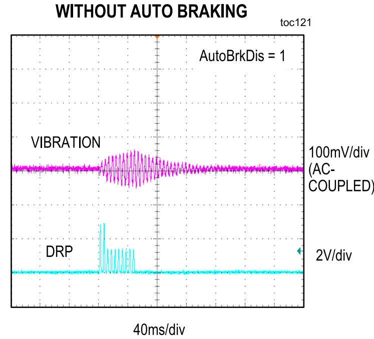
HAPTIC DRIVER LRA AUTOTUNE ERROR IN IniGss RESONANCE SETTING



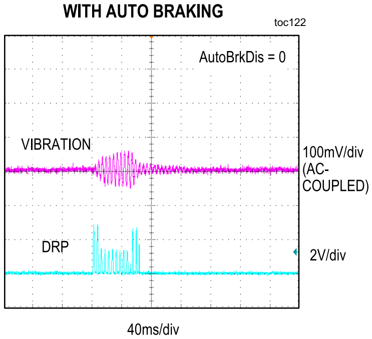
HAPTIC DRIVER LRA AUTOTUNE



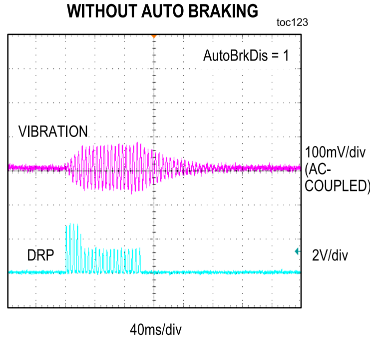
HAPTIC DRIVER 50ms LRA DRIVE WITHOUT AUTO BRAKING



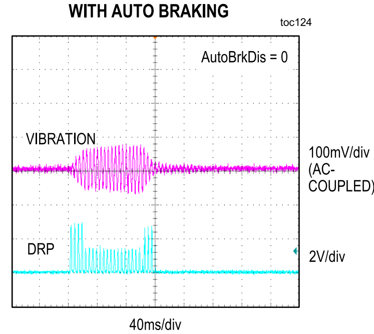
HAPTIC DRIVER 50ms LRA DRIVE WITH AUTO BRAKING



HAPTIC DRIVER 100ms LRA DRIVE WITHOUT AUTO BRAKING



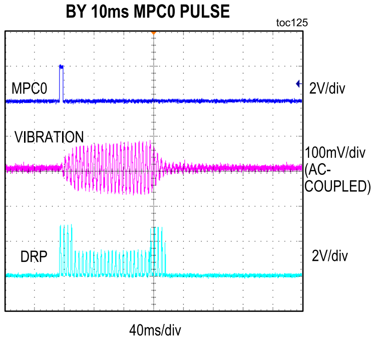
HAPTIC DRIVER 100ms LRA DRIVE WITH AUTO BRAKING



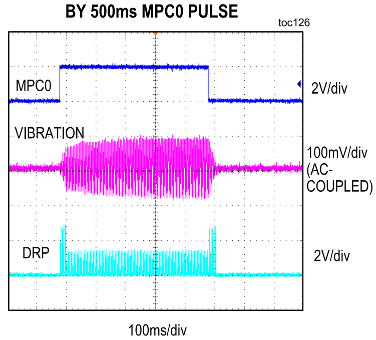
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

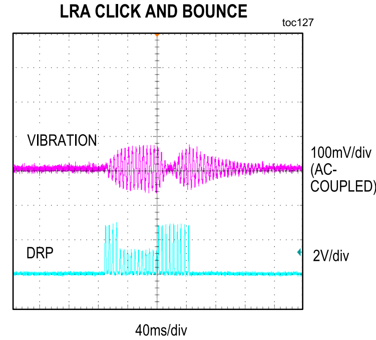
HAPTIC DRIVER
100ms LRA DRIVE TRIGGERED
BY 10ms MPC0 PULSE



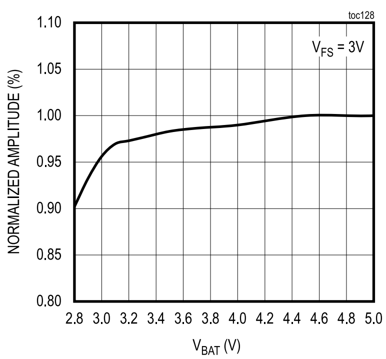
HAPTIC DRIVER
100ms LRA DRIVE EXTENDED
BY 500ms MPC0 PULSE



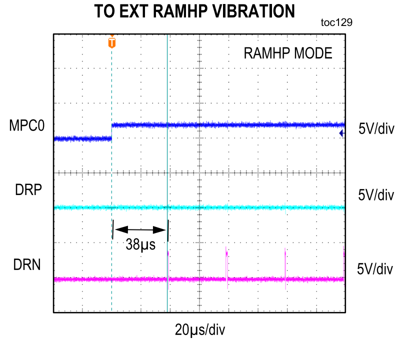
HAPTIC DRIVER
LRA CLICK AND BOUNCE



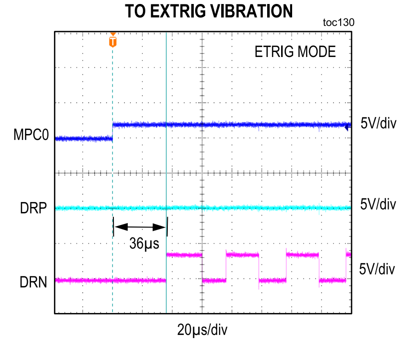
HAPTIC DRIVER LRA AMPLITUDE vs. V_{BAT}



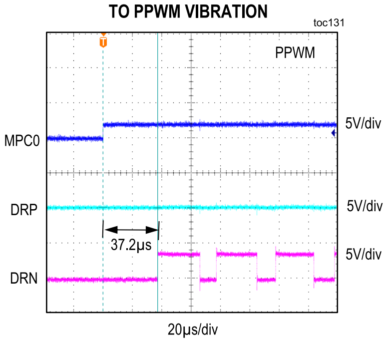
HAPTIC DRIVER
TIME FROM MPC0 ASSERTION
TO EXT RAMHP VIBRATION



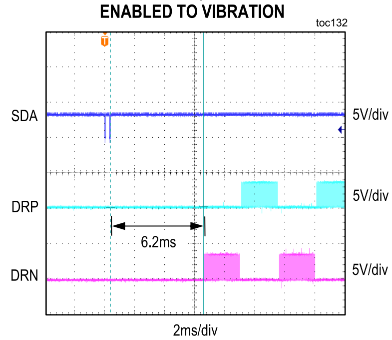
HAPTIC DRIVER
TIME FROM MPC0 ASSERTION
TO EXTRIG VIBRATION



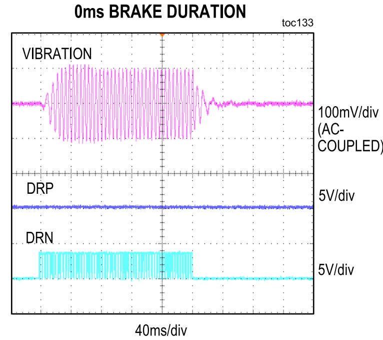
HAPTIC DRIVER
TIME FROM MPC0 ASSERTION
TO PPWM VIBRATION



HAPTIC DRIVER
TIME FROM HptDrvClkEn
ENABLED TO VIBRATION



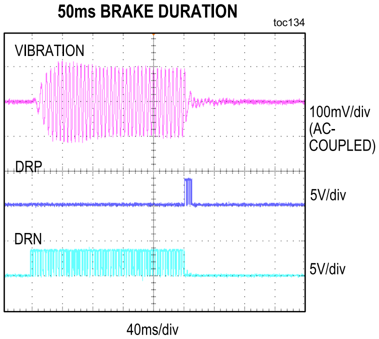
HAPTIC DRIVER
200ms ERM DRIVE
0ms BRAKE DURATION



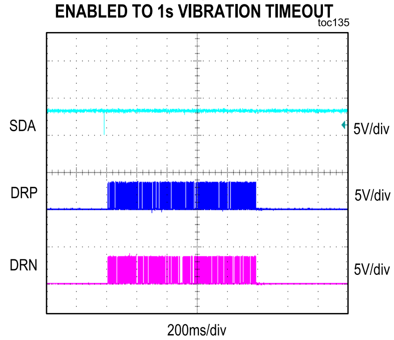
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, C_{BSTOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, L_{BSTOUT} = 4.7µH, T_A = +25°C, unless otherwise noted.)

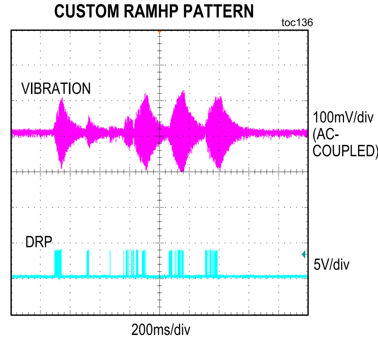
HAPTIC DRIVER
200ms ERM DRIVE
50ms BRAKE DURATION



HAPTIC DRIVER
TIME FROM HptDrvClkEn
ENABLED TO 1s VIBRATION TIMEOUT

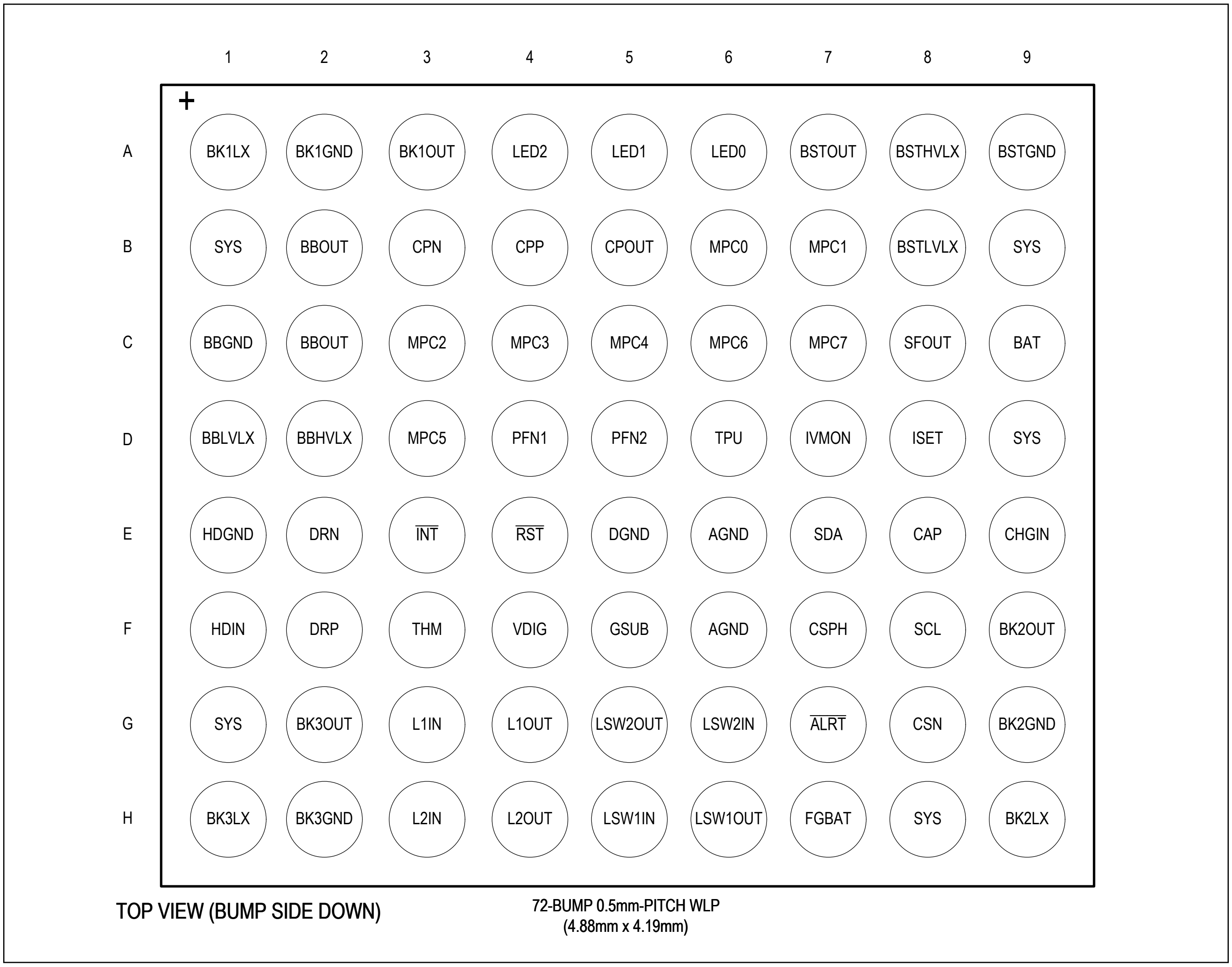


CUSTOM RAMHP PATTERN



Pin Configuration

MAX20360



Pin Description

PIN	NAME	FUNCTION
A1	BK1LX	Buck 1 Regulator Switch. Connect a 1μH or 2.2μH inductor to BK1OUT.
A2	BK1GND	Buck 1 Ground. All ground bumps must be connected on the PCB using a low-impedance trace, or on the GND plane.
A3	BK1OUT	Buck 1 Regulator Output. Bypass with effective capacitance to GND. Refer to the *Buck Output Capacitor Selection* section.
A4	LED2	Current Sink Output 2
A5	LED1	Current Sink Output 1
A6	LED0	Current Sink Output 0

Pin Description (continued)

PIN	NAME	FUNCTION
A7	BSTOUT	Boost Regulator Output. Bypass with effective capacitance to GND. Refer to the *Boost Regulator Section* section.
A8	BSTHVLX	Boost Regulator Switch. Connect through a 2.2μH or 4.7μH inductor to BSTLVLX.
A9	BSTGND	Boost Ground. All ground bumps must be connected on the PCB using a low-impedance trace, or on the GND plane.
B1, B9, D9, G1, H8	SYS	System Load Connection. All SYS bumps must be connected on the PCB using a low-impedance trace or SYS plane. Bypass the common node with a minimum 10μF real capacitance (after derating) to GND.
B2, C2	BBOUT	Buck-Boost Regulator Output. Bypass with effective capacitance to GND. Refer to the *Buck-Boost Output Capacitor Selection* section.
B3	CPN	Charge Pump Capacitor Negative Terminal. Connect 22nF (min), 33nF (max) capacitor to CPP.
B4	CPP	Charge Pump Capacitor Positive Terminal. Connect 22nF (min), 33nF (max) capacitor to CPN.
B5	CPOUT	Charge Pump Output. Bypass with 1μF capacitor to GND.
B6	MPC0	Multipurpose Control I/O 0. LDO3 direct control option.
B7	MPC1	Multipurpose Control I/O 1. FAST control option for buck-boost.
B8	BSTLVLX	Boost Regulator Switch. Connect through a 3.3μH or 4.7μH inductor to BSTHVLX.
C1	BBGND	Buck-Boost Ground. All ground bumps must be connected on the PCB using a low-impedance trace, or on the GND plane.
C3	MPC2	Multipurpose Control I/O 2
C4	MPC3	Multipurpose Control I/O 3
C5	MPC4	Multipurpose Control I/O 4
C6	MPC6	Multipurpose Control I/O 6
C7	MPC7	Multipurpose Control I/O 7
C8	SFOUT	Safe Out LDO. Bypass with 1μF real capacitor (after derating) to GND.
C9	BAT	Battery Connection. Connect to a positive battery terminal. Bypass with a minimum 1μF real capacitor (after derating) to GND.
D1	BBLVLX	Buck-Boost Regulator Switch LV Side. Connect through 2.2μH inductor to BBHVLX.
D2	BBHVLX	Buck-Boost Regulator Switch HV Side. Connect through 2.2μH inductor to BBLVLX.
D3	MPC5	Multipurpose Control I/O 5
D4	PFN1	Configurable Power Mode Control Pin (e.g., $\overline{\text{KIN}}$)
D5	PFN2	Configurable Power Mode Control Pin (e.g., $\overline{\text{KOUT}}$)
D6	TPU	Battery Temperature Thermistor Measurement Pullup. Internally connected to VDIG during battery temperature thermistor measurement. Do not exceed 2mA load on TPU.
D7	IVMON	Voltages and Charging Current Monitor Multiplexer Output.
D8	ISET	External Resistor Connection for Battery Charge Current Level Setting. Do not connect any capacitance on this pin. Maximum allowed capacitance: C_{ISET} < (5μs / R_{ISET}) pF.
E1	HDGND	Haptic Driver Ground. All ground bumps must be connected on the PCB using a low-impedance trace, or on the GND plane.
E2	DRN	Haptic Driver Negative Output
E3	$\overline{\text{INT}}$	Interrupt Open-Drain Output. Active-low.
E4	$\overline{\text{RST}}$	Reset Open-Drain Output. Active-low.

Pin Description (continued)

PIN	NAME	FUNCTION
E5	DGND	Digital Ground. All ground bumps must be connected on the PCB using a low-impedance trace, or on the GND plane.
E6, F6	AGND	Analog Ground. All ground bumps must be connected on the PCB using a low-impedance trace, or on the GND plane.
E7	SDA	I^2C Serial Data Input/Open-Drain Output
E8	CAP	Internal Reference Supply. Bypass with 1µF real capacitor (after derating) to GND.
E9	CHGIN	+28V/-5.5V Protected Charger Input. Bypass with 1µF real capacitance (after derating) to GND.
F1	HDIN	Haptic Driver H-Bridge Supply. Connect using a low-impedance trace to SYS for normal operation or to BBOUT when a higher drive voltage is required. Bypass with a local capacitor to GND if the trace up to SYS or BBOUT bypass capacitors is longer than 10mm.
F2	DRP	Haptic Driver Positive Output
F3	THM	Battery Temperature Thermistor Measurement Connection
F4	VDIG	Internal Reference Supply. Bypass with 1µF real capacitor (after derating) to GND.
F5	GSUB	Substrate Connection. All ground bumps must be connected on the PCB using a low-impedance trace, or on the GND plane.
F7	CSPH	Fuel Gauge Sense Resistor Positive Sense Point. Kelvin connect to the system side of the sense resistor.
F8	SCL	I^2C Serial Clock Input
F9	BK2OUT	Buck 2 Regulator Output. Bypass with effective capacitance to GND. Refer to the *Buck Output Capacitor Selection* section.
G2	BK3OUT	Buck 3 Regulator Output. Bypass with effective capacitance to GND. Refer to the *Buck Output Capacitor Selection* section.
G3	L1IN	LDO 1 Input. Bypass with 1µF capacitor to GND.
G4	L1OUT	LDO 1 Output. Bypass with 1µF real capacitor (after derating) to GND.
G5	LSW2OUT	Load Switch 2 Output
G6	LSW2IN	Load Switch 2 Input
G7	$\overline{ALRT}$	Alert Output. The $\overline{ALRT}$ pin is an open-drain active-low output that provides fuel-gauge alerts. Connect to GND if not used.
G8	CSN	Fuel Gauge Resistor Sense Point. Kelvin connect to the cell-side of the sense resistor.
G9	BK2GND	Buck 2 Ground. All ground bumps must be connected on the PCB using a low-impedance trace, or on the GND plane.
H1	BK3LX	Buck 3 Regulator Switch. Connect a 2.2µH inductor to BK3OUT.
H2	BK3GND	Buck 3 Ground. All ground bumps must be connected on the PCB using a low-impedance trace, or on the GND plane.
H3	L2IN	LDO 2 Input. Bypass with 1µF capacitor to GND.
H4	L2OUT	LDO 2 Output. Bypass with 1µF real capacitor (after derating) to GND.
H5	LSW1IN	Load Switch 1 Input
H6	LSW1OUT	Load Switch 1 Output
H7	FGBAT	Fuel Gauge Power Supply and Battery Voltage Sense Input. Connect to the positive terminal of a battery cell. Bypass with a 0.1µF real capacitor (after derating) to GND.
H9	BK2LX	Buck 2 Regulator Switch. Connect a 1µH or 2.2µH inductor to BK2OUT.

Detailed Description

The MAX20360 is a highly integrated and programmable power management solution designed for ultra-low-power wearable applications. It is optimized for size and efficiency to enhance the value of the end product by extending battery life and shrinking the overall solution size. A flexible set of power-optimized voltage regulators, including multiple buck, boost and buck-boost converters, and linear regulators, provides a high level of integration and the ability to create a fully optimized power architecture. The quiescent current of each regulator is ultra-low targeted at extending battery life in always-on applications.

The MAX20360 includes a complete battery management solution with battery seal, charger, power path, and fuel gauge. Both thermal management and input protection are built into the charger. The device also includes a factory programmable button controller with multiple inputs that are customizable to fit specific product UX requirements.

Three integrated LED current sinks are included for indicator or backlighting functions, and an ERM/LRA driver with automatic resonance tracking is capable of providing sophisticated haptic feedback to the user. A low noise, 1.5W buck-boost converter provides a clean way to power LEDs commonly used in optical heart-rate systems. The device is configurable through an I^2C interface that allows for programming various functions and reading device status, including the ability to read temperature and supply voltages with the integrated ADC.

Power Regulation

The MAX20360 features three high-efficiency, low-quiescent current buck regulators (see the *Buck Regulators* section), a buck-boost regulator (see the *Buck-Boost Regulator* section), two low-quiescent current, low-dropout linear regulators (LDOs) (see the *LDOs* section), a low-quiescent current charge pump (see the *Charge Pump* section), a low-quiescent current, high voltage boost (see the *Boost Regulator* section), and two dedicated load switches (see the *Load Switches* section). Excellent light-load efficiency allows the switching regulators to run continuously without significant energy cost. The buck, buck-boost, and boost regulators can operate in a fixed peak current mode for low-current applications or an adaptive peak-current mode to improve load regulation, extend the high-efficiency range, and minimize capacitor size when more current is required.

Dynamic Voltage Scaling

All of MAX20360 regulators feature dynamic voltage scaling (DVS) to scale the output voltage without disabling the converter. The regulator output voltages are set by direct I^2C writes to the corresponding VSet register. In addition to I^2C DVS, the buck and buck-boost regulators feature two additional control methods for applications where timing is critical: GPIO DVS and SPI DVS. Note that the output-voltage slew rate remains the same in all DVS modes.

Buck DVS transitions maximize the output-voltage slew rate while controlling inrush current for devices that require fast voltage transitions. The other regulators minimize inrush current by limiting the output-voltage slew rate. A typical DVS transition on a buck regulator has a rise time of 10μs. (Note S_DVS_HC)

DVS Mode 0 (I^2C DVS Mode)

DVS Mode 0 configures the regulator outputs to be controlled by I^2C. If Buck_DVSCfg or BBstDVSCfg = 00000 (see these bits: *Buck1DVSCfg*, *Buck2DVSCfg*, *Buck3DVSCfg*, *BBstDVSCfg*), the output voltage of that regulator is controlled by I^2C writes to the Buck_VSet or BBstVSet bitfield (see these bits: *Buck1VSet*, *Buck2VSet*, *Buck3VSet*, *BBstVset*). Note that a regulator in I^2C DVS mode must be unlocked before modifying the output voltage. Regulators are unlocked by setting their lock mask bit to 0 in LockMsk (see bit: *LockMsk*) and writing the unlock password 0x55 to the LockUnlock register (see register: *LockUnlock*).

DVS Mode 1 (GPIO DVS Mode)

In DVS Mode 1, two MPC inputs select the regulator output from four programmed values. To configure a regulator output for GPIO mode, set the corresponding Buck_DVSCfg or BBstDVSCfg bits (see bits: *Buck1DVSCfg*, *Buck2DVSCfg*, *Buck3DVSCfg*, *BBstDVSCfg*) to any value between 00001 and 11100. Each code selects a different pair of MPC_ pins to control the regulator. See the DVS Cfg register descriptions (refer to bits: *Buck1DVSCfg*, *Buck2DVSCfg*, *Buck3DVSCfg*, *BBstDVSCfg*) for details on which MPC inputs are used for a code. In each case, the first MPC listed controls the lower bit and the second MPC controls the higher bit.

The four xxxDVSVlt_ bitfields (see bits: Buck1DVSVlt0, Buck1DVSVlt1, Buck1DVSVlt2, Buck1DVSVlt3, Buck2DvsVlt0, Buck2DvsVlt1, Buck2DvsVlt2, Buck2DvsVlt3, Buck3DvsVlt0, Buck3DvsVlt1, Buck3DvsVlt2, Buck3DvsVlt3, BBstDvsVlt0, BBstDvsVlt1, BBstDvsVlt2, BBstDvsVlt3) are loaded with the corresponding regulator's factory default voltage when the MAX20360 first powers on. After the startup process, each 6-bit output voltage level can be programmed using the I^2C for each converter in the Buck_DVSVlt_ and BBstDVSVlt_ bitfields. As the MPC inputs change, the regulator output adjusts to the newly selected level as illustrated in Figure 1. Voltage levels are selected as shown in Table 1.

Table 1. DVS Mode 1 Voltage Selection

GPIO1	GPIO0	DVS VOLTAGE
0	0	Vlt0
0	1	Vlt1
1	0	Vlt2
1	1	Vlt3

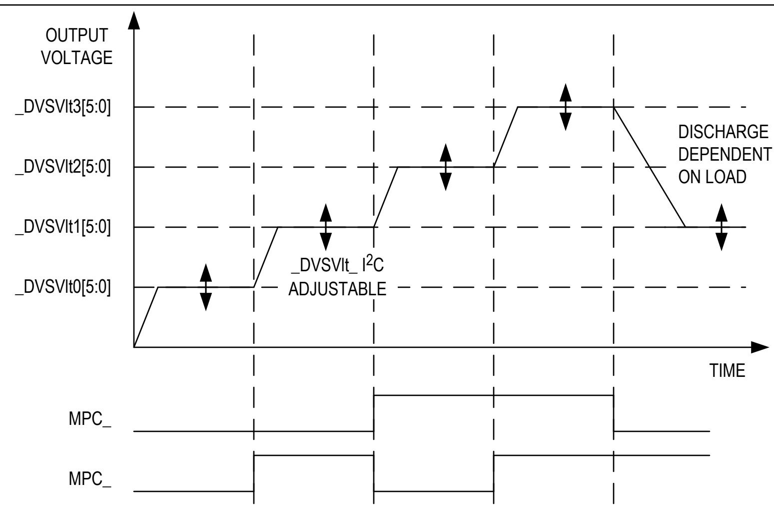


Figure 1. DVS Mode 1, GPIO Control

SPI DVS Mode (DVS Mode 2)

In DVS Mode 2, the regulator voltages are changed by writing command bytes to a 3-wire SPI interface. The SPI interface uses MPC0–MPC2. MPC0 becomes the active-low chip select pin $\overline{CS}$, MPC1 becomes the clock SCLK with polarity 0, and MPC2 becomes the data input pin DIN. Data is clocked in on the SCLK rising edge. The maximum SPI clock frequency is 8MHz. A command byte comprises two address bits (ADD[1:0]) that select the regulator and six voltage bits (VLT[5:0]) that set the voltage. Figure 2 shows how data is clocked in SPI mode.

The output voltage is latched on the 8^{th} rising edge of the clock. Note that voltages set by the SPI interface are mirrored in the Buck_SPIVlt and BBstSPIVlt bitfields for each converter and readback must be done over I^2C. Figure 3 shows two regulators controlled in DVS Mode 2.

The DVS SPI interface supports single-byte and burst-mode data transfer. In single-byte mode, $\overline{CS}$ goes high after each command byte is transferred. In burst-mode, all command bytes are written to the MAX20360 before $\overline{CS}$ returns high. Figure 4 shows how data is written in both modes.

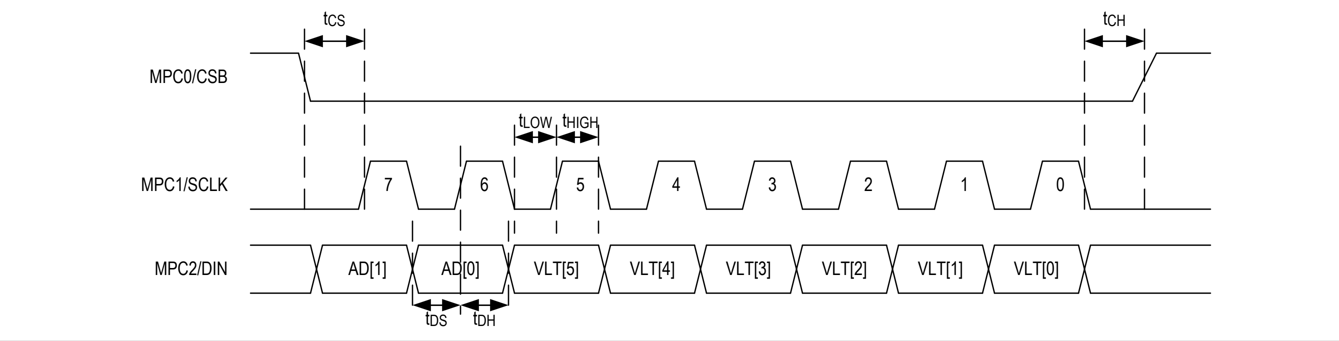


Figure 2. DVS Mode 2 SPI Timing

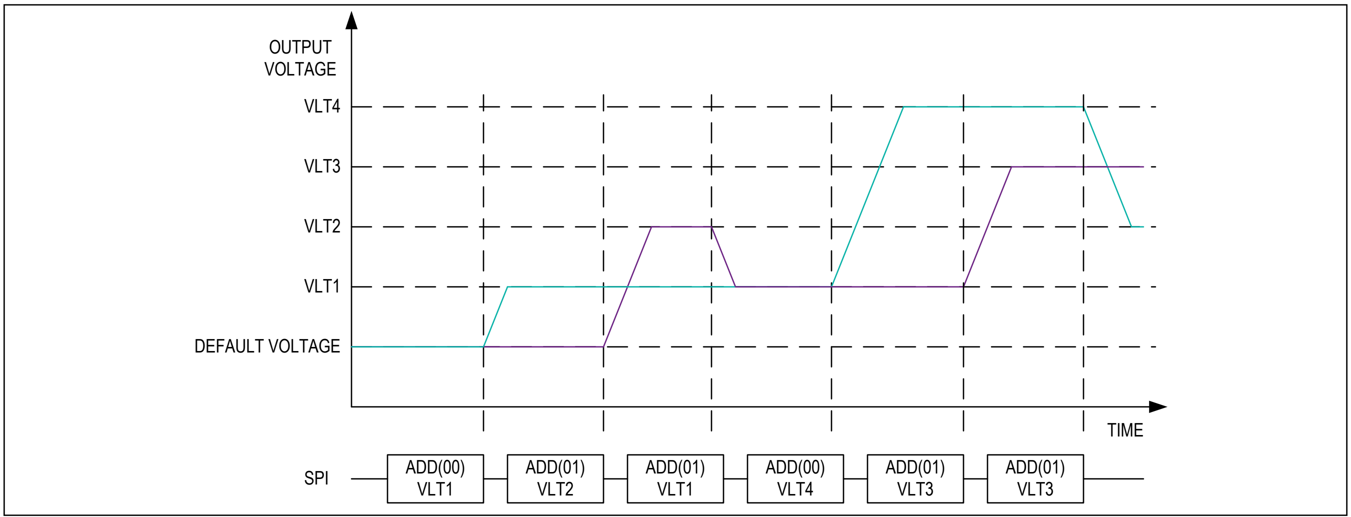


Figure 3. DVS Mode 2, SPI Control

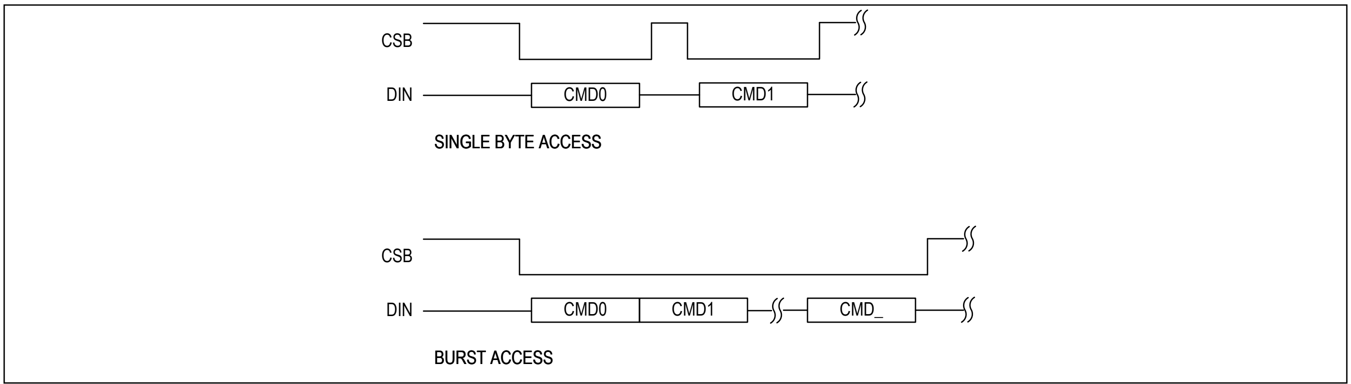


Figure 4. Single-Byte and Burst-Mode SPI Access

Dedicated DVS Interrupts

To quickly alert a host processor when a DVS transition is complete, the MAX20360 features the option to configure the MPC0–MPC6 pins as dedicated PGOOD interrupts. To configure the dedicated interrupt, write the desired BK_MPC_Sel bit(s) in registers 0x70–0x72. Additionally, interrupts signalling changes in the haptic driver, ADC, and USBOk statuses are available as dedicated MPC interrupts as well.

Buck Converter DVS Options

The MAX20360 buck converters feature two DVS valley current settings that can be selected using the Buck_DVSCur bits. Both 500mA and 1A settings are available. The 500mA valley-current setting offers a slightly slower transition time while minimizing the voltage overshoot that can occur due to demagnetization of the inductor at the end of the transition. The 1A valley-current setting offers the fastest DVS transition time, but can exhibit overshoot due to inductor demagnetization. Care should be taken that the overshoot is not potentially damaging to downstream devices.

LDOs

LDO Output Capacitance Selection

The LDOs on MAX20360 are designed to operate with a minimum of 1μF of real capacitance on the output. Pay attention to capacitance derating with DC voltage bias and other factors when making your capacitor selection.

LDO1 MPC0 Control

Both of the LDOs on MAX20360 can be enabled using an MPC input and are configurable as load switches. The low voltage LDO1 offers an additional, on-the-fly configuration option. Setting the LDO1_MPC0CNT (see bit *LDO1_MPC0CNT*) bit to 1 configures LDO1 to be controlled by MPC0 based on the state of LDO1_MPC0CNF (see bit *LDO1_MPC0CNF*). If LDO1_MPC0CNF = 0, MPC0 changes LDO1 between LDO mode and switch mode. If LDO1_MPC0CNF = 1, then MPC0 enables or disables LDO1 in switch mode. See Table 2 for LDO1 MPC0 control detail. Using this MPC control allows the state of LDO1 to be changed much more quickly than through I^2C writes on the order of microseconds. Rapid control of LDO1 supports applications that require minimal delays. For example, quickly increasing the LDO1 output voltage by changing from LDO mode to switch mode reduces the time required for an application processor to transition from a low-power sleep mode to a higher-voltage active state.

Table 2. LDO1 MPC0 Control

LDO1En	LDO1_MPC0CNF	LDO1_MPC0CNT	MPC0 CONTROL
00	1	1	MPC0 control switch mode on/off
01	0	1	MPC0 control LDO mode or switch mode
	1	1	
10	1	1	MPC0 control switch mode on/off
11	1	1	MPC0 control switch mode on/off

Internal Switchover for LDO2 Always-On Power

In order to power LDO2 when no battery voltage is present, an internal switchover circuit is available. This switchover circuit requires that the LDO be bypassed at the L2IN node by 1μF of capacitance. The L2IN node must otherwise be left unconnected. The switchover circuit automatically powers the LDO from a regulated voltage off of CHGIN so that it is powered even if no battery is present. This option can be enabled by default at the factory or left disabled by default. Either way, the behavior is programmable by I^2C after startup. This function is intended to support an output voltage of 1.8V or lower and a load current of 100μA (max) or smaller. The R_{ON_L2IN} specification in the electrical characteristics table is used to generate the worst-case output-power capability based on the minimum input voltage from V_{CCINT} (see *Note 2*), maximum output voltage of LDO2, and the maximum on-resistance.

Load Switches

The MAX20360 load switches allow a system to disconnect loads when inactive to reduce quiescent current. To limit inrush on enabled, each load switch initially behaves as a constant current source with the value I_{SW_START}. Current mode remains until the switch output is charged to meet the condition $V_{SW\_IN} - V_{SW\_OUT} < V_{SW\_PROT}$. Once the condition is met, the switch turns fully on and connects LSW_IN to LSW_OUT. If this condition is not met within the startup time-out t_{STUP_LSW}, the switch attempts to turn on after a retry delay t_{RTRY_LSW}.

Both switches feature optional voltage protection to prevent overcurrent. A protection comparator monitors the difference between the input and output voltages. If the difference exceeds V_{SW_PROT}, the switch is opened to protect downstream circuitry. The comparator can be disabled with the LSW_LowIq bit to reduce quiescent current if the upstream power supply has its own overcurrent protection.

Boost Regulator

The MAX20360 includes a high-voltage boost converter that supports output voltages up to 20V for powering display backlight LEDs, piezo buzzers, or other system components requiring high supply voltages. In order to maximize the ease of implementation, the peak current settings of the boost regulator are automatically adjusted to the most optimal settings for a given output voltage when BstISetLookUpDis = 0 (see *BstISetLookUpDis*). If a different peak current setting is desired, the BstISetLookUpDis = 1 (see *BstISetLookUpDis*) setting must be selected. In order to maintain stability, the boost must meet minimum capacitance requirements. Figure 5 below shows the required effective capacitance for a given output voltage to guarantee stability.

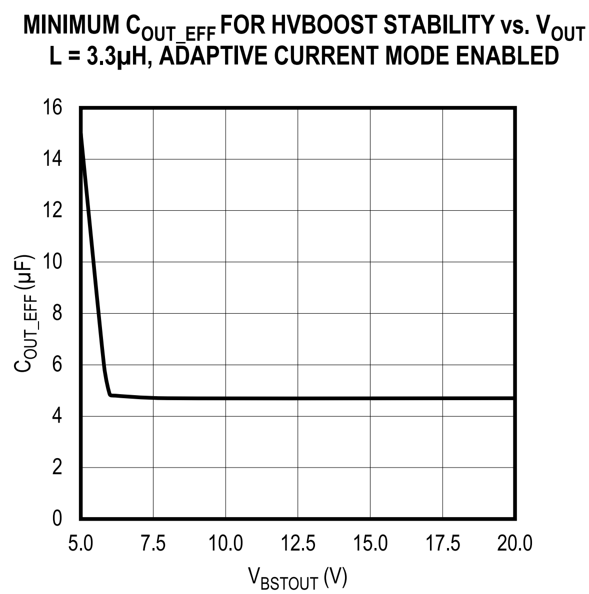


Figure 5. Minimum Effective Capacitance for HVBOOST Stability

Boost Inductor Selection

Inductor selection for the MAX20360 high-voltage boost converter should be optimized for the intended application. A 4.7µH inductor value is recommended for this boost; however, 3.3µH and 2.2µH inductors can be used for the tradeoff of efficiency. Aside from the inductor value physical size, DC resistance (DCR), maximum average current, and saturation current are the primary factors to consider. The maximum average inductor current is obtained using the following equation:

$$I_{L\_MAX} = \frac{V_{OUT\_MAX} \times I_{OUT\_MAX}}{\eta \times V_{IN\_MIN}}$$

where,

V_{OUT_MAX} = Maximum expected operating voltage

I_{OUT_MAX} = Maximum expected output current

V_{IN_MIN} = Minimum expected operating input voltage

η = Expected worst-case efficiency in the minimum input voltage and maximum output power case (see the *Typical Operating Characteristics* section for help in estimating efficiency)

The average inductor current calculated above dictates the required maximum average current for temperature rise on the inductor. In order to determine the required inductor saturation current, the peak current must be calculated. The peak current for this converter can be calculated as:

$I_{L\_PEAK\_CCM} = I_{L\_MAX} + \frac{1.15 \times BstISet}{2} + 100mA$ and $I_{L\_PEAK\_DCM} = 1.15 \times BstISet + 100mA$

where BstISet is the peak current setting set as described in the Boost Inductor Peak Current section. (see *BstISet*)

When selecting an inductor, one primary factor in achieving high efficiency is the DCR of the inductor. For maximum efficiency, select an inductor with the lowest DCR possible in the required package size. Another factor to consider is magnetic losses. Generally magnetic losses are lower in inductors with larger physical size and/or higher saturation current ratings. In most cases, ferrite inductors should be avoided as they tend to exhibit poor AC characteristics, especially in DCM.

Boost Capacitor Selection

The high-voltage boost is designed to operate with a minimum of 4.8μF of real capacitance on the output. Pay attention to capacitance derating with DC voltage bias and other factors when making your capacitor selection.

Inductor Peak Current Limit

The boost regulator monitors the maximum value of the inductor current each switching cycle to control the end of the On phase. The peak current can be fixed to the value BstISet (BstIAdptEn = 0) or allowed to change based on load requirements (BstIAdptEn = 1) (see bits: *BstISet*, *BstIAdptEn*). It is strongly recommended to leave BstIAdptEn = 1 as the setting as this greatly improves load regulation and extends the range over which the converter achieves high efficiency. Peak current is set in the BstISet register. In order to maximize the ease of implementation, the peak current settings of the boost regulator are automatically adjusted to the settings shown in Figure 6 when BstISetLookUpDis = 0 (see bit: *BstISetLookUpDis*). These are the optimal settings for a given output voltage. If a different peak current setting is desired the BstISetLookUpDis = 1 (see bit: *BstISetLookUpDis*) setting must be selected; only then will the BstISet register have any effect.

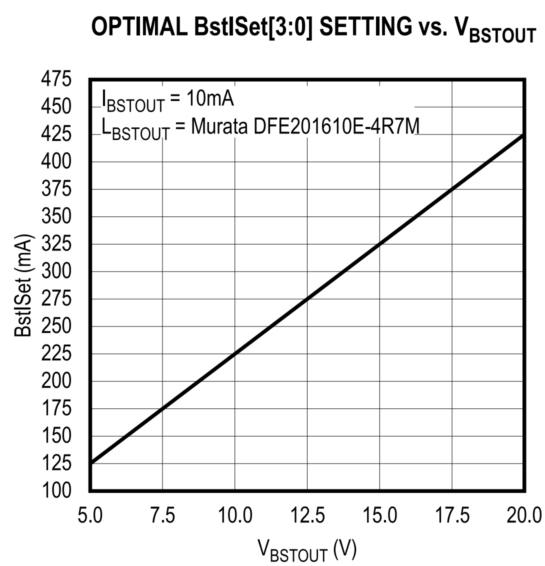


Figure 6. Optimal Peak Current vs. Voltage Lookup Table

Boost Converter and LED0 Closed Loop Operation

The boost regulator has a feature allowing it to work in closed loop with the LED current sink LED0. The intent is to allow LEDs that are driven by LED0 and the boost to be run as efficiently as possible. When LED_BoostLoop = 1 (see bit: *LED_BoostLoop*), the boost voltage is adjusted in order to regulate the voltage at LED0 to the value set by LED0_REFSEL (see bit: *LED0_REFSEL*). This allows the headroom at the LED0 current sink to be minimized, and as a result, the efficiency of driving the LEDs is maximized. The boost regulation circuit can only act to increase the voltage from the initial setting and has a 5V range of adjustability.

Buck-Boost Regulator

The MAX20360 buck-boost regulator provides a low-ripple voltage rail that can be used for voltage regulation near or above the battery voltage. The buck-boost is sized to be ideal in powering LEDs used in photoplethysmography (PPG) systems. This includes PPG systems with short wavelength LEDs that require large forward voltage drops. The buck-boost topology as well as the dynamic voltage scaling capabilities allow the user to adjust the output voltage to accommodate as little headroom on the LED current sink as possible to maximize efficiency.

Several other controls help to optimize the efficiency and output noise of the regulator. These include peak current control and automatic peak and valley current adjustment. Additionally, the Buck-Boost regulator can operate in buck-only mode to increase efficiency when V_{BBOUT} is much lower than V_{SYS}.

Buck-Boost Inductor Selection

Inductor selection for the MAX20360 should be optimized for the intended application. A 2.2μH inductor value is required for this buck-boost. Aside from the inductor value physical size, DC resistance (DCR), maximum average current, and saturation current are the primary factors to consider. The maximum average inductor current is obtained using the following equation:

$$I_{L\_MAX} = \frac{V_{OUT\_MAX} \times I_{OUT\_MAX}}{\eta \times V_{IN\_MIN}}$$

where,

V_{OUT_MAX} = Maximum expected operating voltage

I_{OUT_MAX} = Maximum expected output current

V_{IN_MIN} = Minimum expected operating input voltage

η = Expected worst-case efficiency in the minimum input voltage and maximum output power case (see the Typical Operating Characteristics section for help in estimating efficiency).

The average inductor current calculated above dictates the required maximum average current for temperature rise on the inductor. In order to determine the required inductor saturation current, the peak current must be calculated. The worst case peak current for this converter can be calculated as the higher value between:

$$I_{L\_PEAK\_CCM} = I_{L\_MAX} + \frac{1.15 \times (\text{BBstIPSet1} + \text{BBstIPSet2})}{2} + 100\text{mA}$$

and

$$I_{L\_PEAK\_DCM} = 1.15 \times (\text{BBstIPSet1} + \text{BBstIPSet2}) + 100\text{mA}$$

If I_{L_PEAK} is expected to occur when V_{IN} is lower than V_{OUT} by at least 100mV, a less pessimistic assumption can be taken as the lower of the below:

$$I_{L\_PEAK\_CCM} = I_{L\_MAX} + \frac{1.15 \times \text{BBstIPSet1}}{2} + 100\text{mA} \text{ and } I_{L\_PEAK\_DCM} = 1.15 \times \text{BBstIPSet1} + 100\text{mA}$$

where BBstIPSet1 and BBstIPSet2 are the peak current settings.

When selecting an inductor, one primary factor in achieving high efficiency is the DCR of the inductor. For maximum efficiency, select an inductor with the lowest DCR possible in the required package size. Another factor to consider is magnetic losses. Generally magnetic losses are lower in inductors with larger physical size and/or higher saturation current ratings. In most cases, ferrite inductors should be avoided as they tend to exhibit poor AC characteristics, especially in DCM. Refer to Table 3 for inductor recommendations for a given optimization parameter.

Table 3. Recommended Inductors

OPTIMIZATION PARAMETERS	VENDOR	PART NUMBER
Efficiency	Murata	DFE201610E-2R2M
Size	Murata	DFE18SBN2R2MEL

Buck-Boost Output Capacitor Selection

The buck-boost is designed to be compatible with small case-size ceramic capacitors. As such, the device has low output capacitance requirements to accommodate the steep voltage derating of 0603 and 0402 (imperial) case-size capacitors. The sample derating curve in Figure 7 shows the required minimum capacitance for the BBOUT node.

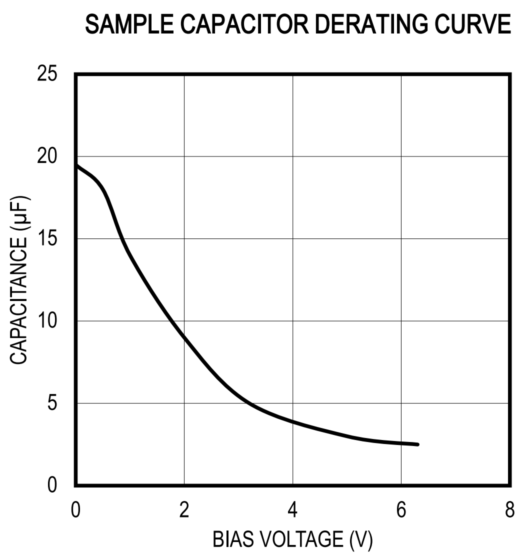


Figure 7. Buck-Boost Required Minimum Output Capacitance

Architecture and Switching Phases

The buck-boost comprises a typical noninverting buck-boost topology. Figure 8 illustrates the regulator's basic structure with arrows depicting the current flow in each switching phase. Depending on the register settings and input-to-output voltage relationship, the buck-boost sequences through the below switching phases in a particular order to deliver charge to the output. At most two switches are on in any given phase.

- Phase 1: MP1 on, MP2 on. Inductor charges.
- Phase 2: MP1 on, MN2 on. Inductor charges.
- Phase 3: MN1 on, MP2 on. Inductor discharges.
- Phase 4: MN1 on, MN2 on. Freewheeling.

The buck-boost features a frequency comparator to monitor its switching frequency. Switching frequency increases as the load current increases. Under light loads, the buck-boost optimizes its feedback loop for low quiescent current. When load requirements increase the switching frequency to the f_{HIGH} threshold, the low-quiescent current mode is disabled to improve response time. The transition above this threshold generates a discontinuity in the output-voltage ripple. If the transition occurs at a sensitive current causing noise on the output at a critical frequency, adjustment of the f_{HIGH}

threshold is recommended with the trade-off of a slight decrease in light load efficiency. The f_{HIGH} threshold is set by the BBFHighSh setting in the BBstCfg1 register (see register: *BBstCfg1*). Hysteresis prevents the buck-boost regulator from resuming the low-quiescent current mode until the switch frequency decreases to $f_{HIGH}/4$.

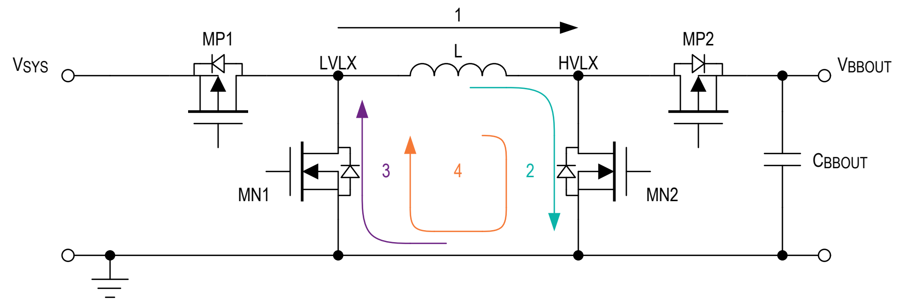


Figure 8. The Buck-Boost Regulator and Switching Phases

Buck-Boost Mode

When BBstMode (register 0x31[1]) is 0, the regulator operates in buck-boost mode. The inductor charges in phase 2 up to BBstIPSet1 (register 0x33[3:0]). This minimizes noise when V_{SYS} is close to V_{BBOUT}. The buck-boost then transitions to phase 1. If $V_{SYS} > V_{BBOUT}$, the inductor continues charging until either the current reaches BBstIPSet1 + BBstIPSet2 (register 0x33[7:4]) or after a 500ns delay. If $V_{SYS} \leq V_{BBOUT}$, the buck-boost waits for the 500ns delay to elapse or until the current drops to the valley limit. Next, the regulator enters phase 3 to discharge the inductor current to the valley limit. When the inductor current reaches the valley-current crossing threshold or falls below 0, the regulator freewheels in phase 4 until the next charge phase. When operating in continuous conduction mode (CCM), the buck-boost enters phase 4 for approximately 30ns if BBZCCmpEnb = 1. The buck-boost skips phase 4 when operating in CCM and BBZCCmpEnb = 0. The valley behavior is determined by BBZCCmpEnb (register 0x34[5]). Figure 9 shows the inductor current in buck-boost mode.

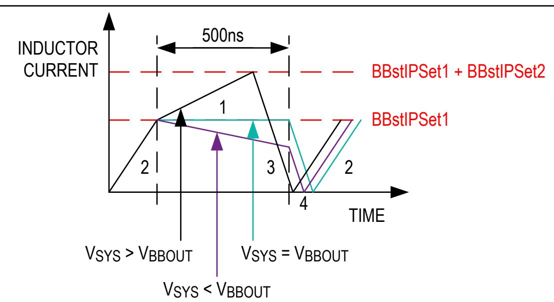


Figure 9. Buck-Boost Inductor Current in Buck-Boost Mode

Buck-Only Mode

To maximize efficiency when $V_{SYS} > V_{BBOUT}$, the buck-boost regulator has a buck-only mode. When BBstMode = 1, the regulator behaves as a synchronous buck regulator. The inductor charges in phase 1 until the inductor current reaches BBstIPSet1. The regulator then transitions to phase 3 to provide a path to deliver the inductor current to the output. Figure 10 shows the inductor current in buck-only mode.

Buck-only mode reduces switching losses present in buck-boost mode. Buck-only mode should be used when V_{BBOUT} is always less than V_{SYS} to maximize efficiency.

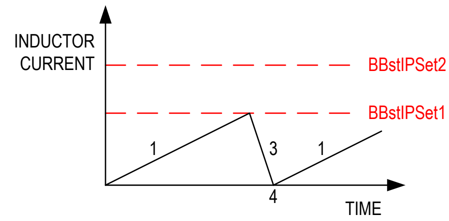


Figure 10. Buck-Boost Inductor Current in Buck-Only Mode

Inductor Peak and Valley Current Limits

The buck-boost regulator monitors the maximum and minimum values of the inductor current. Peak and valley currents can be fixed to the values in BBstIPSet_ and 0mA, respectively (see bits: *BBstIPSet1*, *BBstIPSet2*), or allowed to change based on load requirements if BBstIAdptDis = 0 (see bit: *BBstIAdptDis*).

Peak currents are set in the BBstISet register (see register: *BBstISet*). BBstIPSet1 controls the peak current when V_{SYS} < V_{BBOUT} and when the regulator is in buck-only mode. BBstIPSet2 sets a secondary current limit when V_{SYS} > V_{BBOUT} in buck-boost mode. The total inductor current limit when V_{SYS} > V_{BBOUT} is BBstIPSet1 + BBstIPSet2. The buck-boost regulator transitions from phase 1 to phase 3 if the inductor current reaches BBstIPSet1 + BBstIPSet2 or if the 500ns timeout has elapsed. Minimizing the difference between BBstIPSet1 and BBstIPSet2 reduces the output ripple, but decreases efficiency. Care must be taken to optimize the peak current settings to keep a low output ripple while maximizing efficiency. Figure 11 presents the safe operating area of BBstIPSet2 with respect to BBstIPSet1. Selecting values lower than those of Figure 11 for a given value can reduce efficiency and increase output ripple. Figure 12 is a graphical guide to selecting combinations of BBstPSet1 and BBstIPSet2 to maximize efficiency for specific BBstVSet values.

In order to maximize the ease of implementation, the peak current settings of the buck-boost regulator are automatically adjusted to the settings shown in Figure 12 for a given output voltage when BBstISetLookUpDis = 0. If a different peak current setting is desired, the BBstISetLookUpDis = 1 setting must be selected; only then will BBstIPSet1 and BBstIPSet2 have an effect (see bit: *BBstISetLookUpDis*) When BBstIAdptDis = 0 (see bit: *BBstIAdptDis*), the regulator automatically increases the peak current limits when the load increases to improve load regulation and efficiency at high loads. When BBstZCCmpDis = 1 (see bit: *BBstZCCmpDis*), the buck-boost operates with peak and valley current limits. In discontinuous conduction mode (DCM), the valley limit is 0mA and it acts as a zero crossing. In CCM, the peak and valley limits are automatically adjusted by the voltage loop if BBstIAdptDis = 0 (see bit: *BBstIAdptDis*). However, when BBstZCCmpDis = 0 (see bit: *BBstZCCmpDis*), the buck-boost operates with peak, valley, and zero crossing current limits. The zero crossing limit is fixed at 0mA while the peak and valley limits are adjusted by the voltage loop if BBstIAdptDis = 0 (see bit: *BBstIAdptDis*).

In DCM, the valley current limit is negative so the end of phase 1 or 3 is determined by the zero-crossing current. In CCM, the valley current limit is ≥ 0mA if BBstZCCmpDis = 0 (see bit: *BBstZCCmpDis*). The end of phase 1 or 3 is thus determined by the valley current comparator.

Disabling the zero current crossing comparator reduces the buck-boost output ripple. Enabling the comparator improves EMI in CCM by removing the phase 4 stage in CCM mode that is otherwise present when BBstZCCmpDis = 1 (see bit: *BBstZCCmpDis*).

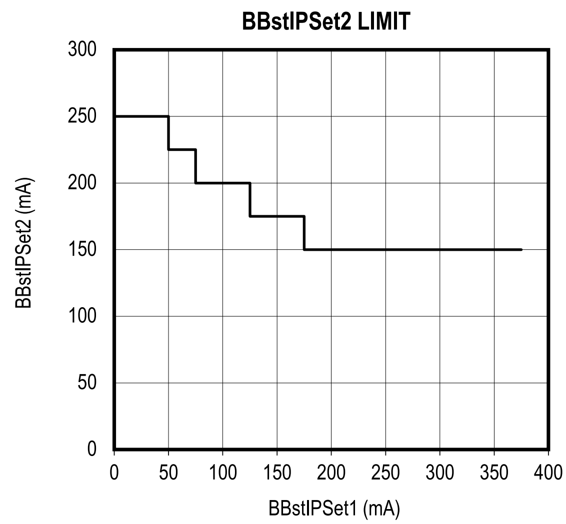


Figure 11. Minimum BBstIPSet2 Limit for a Given BBstIPSet1 Setting

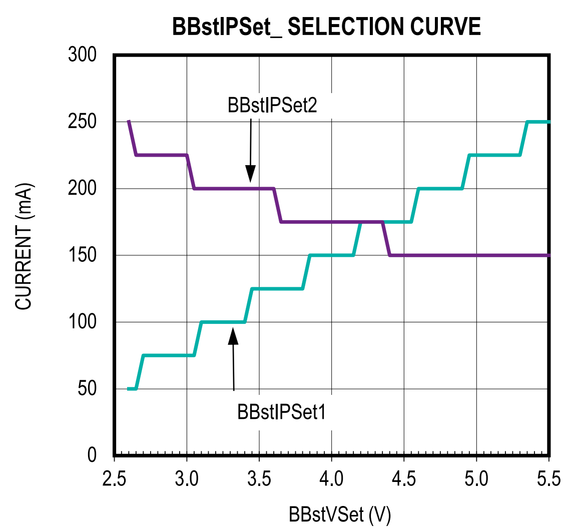


Figure 12. Recommended BBstIPSet1 and BBstIPSet2 Settings

Buck Regulators

The MAX20360 includes three buck regulators: two low-power 400mA bucks and one high-power 600mA buck. All of the buck regulators operate in a pulse-frequency modulation (PFM) scheme with peak and valley current control. At light loads, the buck converters operate in discontinuous conduction mode (DCM) to maximize efficiency. The buck regulators have minimum and maximum capacitance requirements. The effective output capacitance of each buck should fall within these limits to guarantee stable operation. Figure 13 illustrates the minimum and maximum capacitance for each output-voltage setting.

Buck Inductor Selection

Inductor selection for the MAX20360 should be optimized for the intended application. A 2.2μH inductor value is strongly preferred for these buck converters. A 1μH inductor is acceptable, but results in decreased efficiency with only marginal load transient response benefits. Aside from the inductor-value physical size, DC resistance (DCR), maximum average current, and saturation current are the primary factors to consider. The maximum average inductor current is simply equal to the maximum output current expected in the application.

The average inductor current calculated above dictates the required maximum average current for temperature rise on the inductor. In order to determine the required inductor saturation current, the peak current must be calculated. The peak current for this converter can be calculated as the higher value between the following equations:

$$I_{L\_PEAK\_CCM} = I_{L\_MAX} + \frac{1.15 \times BuckxISet}{2} + 100mA \text{ and } I_{L\_PEAK\_DCM} = 1.15 \times BuckxISet + 100mA$$

Where BuckxISet is the peak current setting for the relevant buck converter and I_{L_MAX} is the maximum expected load current on the converter.

When selecting an inductor, one primary factor in achieving high efficiency is the DCR of the inductor. For maximum efficiency, select an inductor with the lowest DCR possible in the required package size. Another factor to consider is magnetic losses. Generally, magnetic losses are lower in inductors with larger physical size and/or higher saturation current ratings. In most cases, ferrite inductors should be avoided as they tend to exhibit poor AC characteristics, especially in DCM. Refer to Table 4 for inductor recommendations for a given optimization parameter.

Table 4. Recommended Inductors Buck

OPTIMIZATION PARAMETERS	VENDOR	PART NUMBER
Efficiency	Murata	DFE201610E-2R2M
Size	Murata	DFE18SBN2R2MEL

Buck Output Capacitor Selection

The bucks are designed to be compatible with small case-size ceramic capacitors. As such, the device has low output capacitance requirements to accommodate the steep voltage derating of 0603 and 0402 (imperial) case-size capacitors. Additionally, there is a maximum output capacitance requirement to maintain stability. The required minimum and maximum capacitance requirements in Figure 13 show the required capacitance for the BK_OUT node.

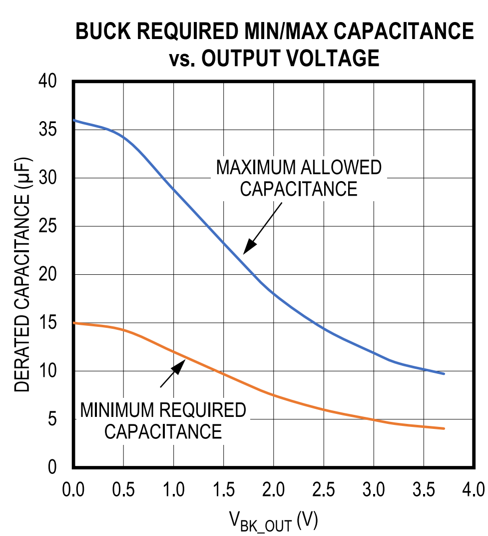


Figure 13. Buck Required Minimum and Maximum Capacitance to Guarantee Stability

Inductor Peak and Valley Current Limits

When a buck regulator is in DCM, the inductor's minimum current threshold (I_{VALLEY}) is 0mA and the inductor's peak current threshold (I_{PEAK}) is set automatically to the optimal value per Figure 14 by the regulator's automatic lookup table or by the Buck_ISet register (see bits: *Buck1ISet*, *Buck2ISet*, *Buck3ISet*) if Buck_ISetLookUpDis = 1 (see bits: *Buck1ISetLookUpDis*, *Buck2ISetLookUpDis*, *Buck3ISetLookUpDis*). In this mode, as the load increases the switching frequency also increases in accordance with the PFM control scheme.

As the load continues to increase, the switching frequency of the buck regulator eventually reaches roughly 1.1MHz. At this point, if the buck regulator adaptive current setting is enabled (Buck_IAdptDis = 0) (see bits: *Buck1IAdptDis*, *Buck2IAdptDis*, *Buck3IAdptDis*), I_{PEAK} and I_{VALLEY} shifts upward maintaining a roughly constant offset between themselves (set by the inductor peak current setting described in the first paragraph above). Once the valley current begins to increase, the regulator is operating in continuous conduction mode (CCM) as the inductor is no longer discharged completely to 0mA. The slope of the switching frequency flattens and rises only marginally for the remainder of the load range. This control scheme seeks to balance both the ohmic losses arising from the peak current level and the switching losses incurred by driving the gates of the FETs, extending load regulation and high efficiency over a wider range of loads.

If the adaptive current setting is disabled (Buck_IAdptDis = 1) (see bits: *Buck1IAdptDis*, *Buck2IAdptDis*, *Buck3IAdptDis*), the switching frequency continues to rise until the regulator reaches critical conduction mode. As the load increases past critical conduction mode, the switching frequency saturates and the buck regulator behaves as a current source. This results in increased load regulation error at the output of the regulator.

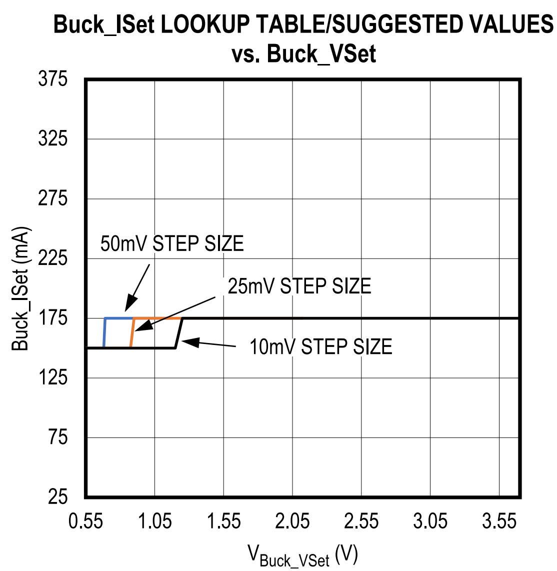


Figure 14. Optimal Peak Current Setting vs. Output Voltage

Adjustments to Manipulate Buck Switching Frequency

In some applications, the buck output-voltage ripple can generate noise at frequencies that interfere with sensitive analog circuitry. The adjustable peak current of the MAX20360 provides the flexibility to shift the ripple frequency out of the sensitive frequency ranges when the regulator is in DCM mode. Increasing the peak current delivers more charge to the output capacitor in a switching cycle, thereby decreasing the number of times the output capacitor requires charging to supply the same load. In this case, the output ripple frequency decreases for a given load current and shifts below sensitive, high-frequency ranges. Conversely, decreasing the peak current increases the switching frequency for a given load current to prevent injecting noise in sensitive, low-frequency ranges.

Note that increasing the peak current results in higher ohmic losses, which can lower efficiency and increased output-voltage ripple amplitude. Decreasing the peak current incurs higher switching losses, which can lower the efficiency. Refer to the Typical Operating Characteristics section.

In order to maximize the ease of implementation, the peak current settings of the buck regulator can be automatically adjusted to the optimal settings for a given output voltage. When Buck_ISetLookUpDis = 0 (see bits: *Buck1ISetLookUpDis*, *Buck2ISetLookUpDis*, *Buck3ISetLookUpDis*), the MAX20360 updates the peak current settings when the output voltage of the buck regulator is changed in any DVS mode. If an application requires independent peak current control, setting Buck_ISetLookUpDis = 1 (see bits: *Buck1ISetLookUpDis*, *Buck2ISetLookUpDis*, *Buck3ISetLookUpDis*) disables the automatic update function.

High Power Buck Converter with LDO Mode

The charging phase of a buck regulator delivers energy to the inductor by creating a path from the regulator input to its output. Current through the inductor rises according to the equation:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{L} \times \Delta t$$

Because the inductor current must ramp to a fixed value (i.e., ΔI is fixed and is the peak current limit), as the input voltage approaches the output voltage, the time required for the inductor to reach its peak current (Δt) increases. This causes the regulator output-voltage ripple amplitude on the output of the converter to grow as the V_{IN} - V_{OUT} value decreases, reducing the efficiency and increasing the output ripple noise.

To avoid an excessively large Δt, the high-current Buck3 regulator of the MAX20360 automatically transitions into an LDO operation mode when V_{IN} – V_{OUT} reaches $V_{IN\_BOUT\_DRPOUT\_TH\_F}$. This eliminates the performance reduction when Buck3 operates at low buck voltage ratios. The LDO mode also improves performance over a standard buck architecture since LDOs are efficient and maintain noise immunity at low step-down ratios. Transitions into and out of LDO mode have substantial hysteresis to prevent oscillations when entering and exiting LDO mode.

Charge Pump

A low-quiescent current 5V charge pump is included in MAX20360. For proper operation a 22nF (min), 33nF (max) capacitor should be connected between the CPP and CPN bumps.

Power Switch and Reset Control

The MAX20360 features a power switch that provides the ability to execute a reset sequence or to turn off the main system power and enter OFF or SEAL mode to extend battery life. In OFF mode, the SYS node and all PMIC outputs are turned off except LDO2 when it is configured as always on, either by the LDO2Seq (see bit: *LDO2Seq*) or when it is kept on before entering OFF mode. In SEAL mode, all regulators and the SYS node are turned off. SEAL mode is the lowest-quiescent current mode of the MAX20360 and maximizes battery life when a product cannot be used for an extended period, such as when shipping from the factory to a retailer. More details on the power modes can be found in the *PMIC Power Modes* section.

Shutdown and reset events are triggered by an external control using the power function (PFN) control inputs, I^2C commands, or if other conditions are met. The behavior of the PFN pins is preconfigured to support one of the multiple types of wearable application cases. Table 5 describes the behavior of the PFN1 and PFN2 pins based on the PwrRstCfg bits (see *PwrRstCfg* in Table 5), while Figure 15 through Figure 23 show the state diagrams associated with each mode.

A soft-reset sends a 10ms pulse on $\overline{RST}$ and either leaves register settings unchanged or resets them to their default values depending on the device version (see bit: *SftRstCfg*). A hard reset on any device initiates a complete power-on reset (POR) sequence.

Devices with HrvEn = 0 enter SEAL mode on cold boot (battery attach with no CHGIN present). Devices with HrvEn = 1 enter battery recovery (BR) mode on cold boot. When the MAX20360 is in ON mode, it enters OFF/SEAL/BR mode after receiving PWR_OFF_CMD/PWR_SEAL_CMD/PWR_BR_CMD I^2C command in the PwrCmd register (see register: *PwrCmd*), respectively. When the device detects a valid PFN signal it enters OFF mode or BR mode based on the PwrRstCfg and HrvEn setting.

The MAX20360 exits OFF/SEAL mode and turns the main power back on when there is a qualified PFN1 signal for PwrRstCfg settings where PFN1 is KIN, or when a valid voltage is applied to CHGIN. In the powered-on state, the SYS node is enabled and other functions can be controlled through the I²C registers. Figure 24 and Figure 25 illustrate a complete boot sequence coming out of OFF/SEAL mode.

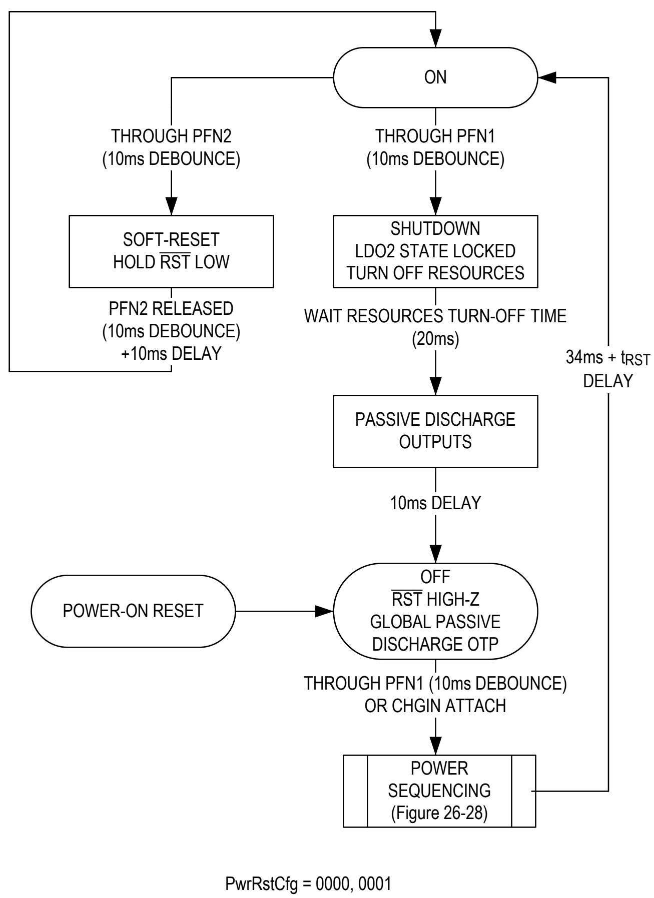


Figure 15. PwrRstCfg 0000, 0001

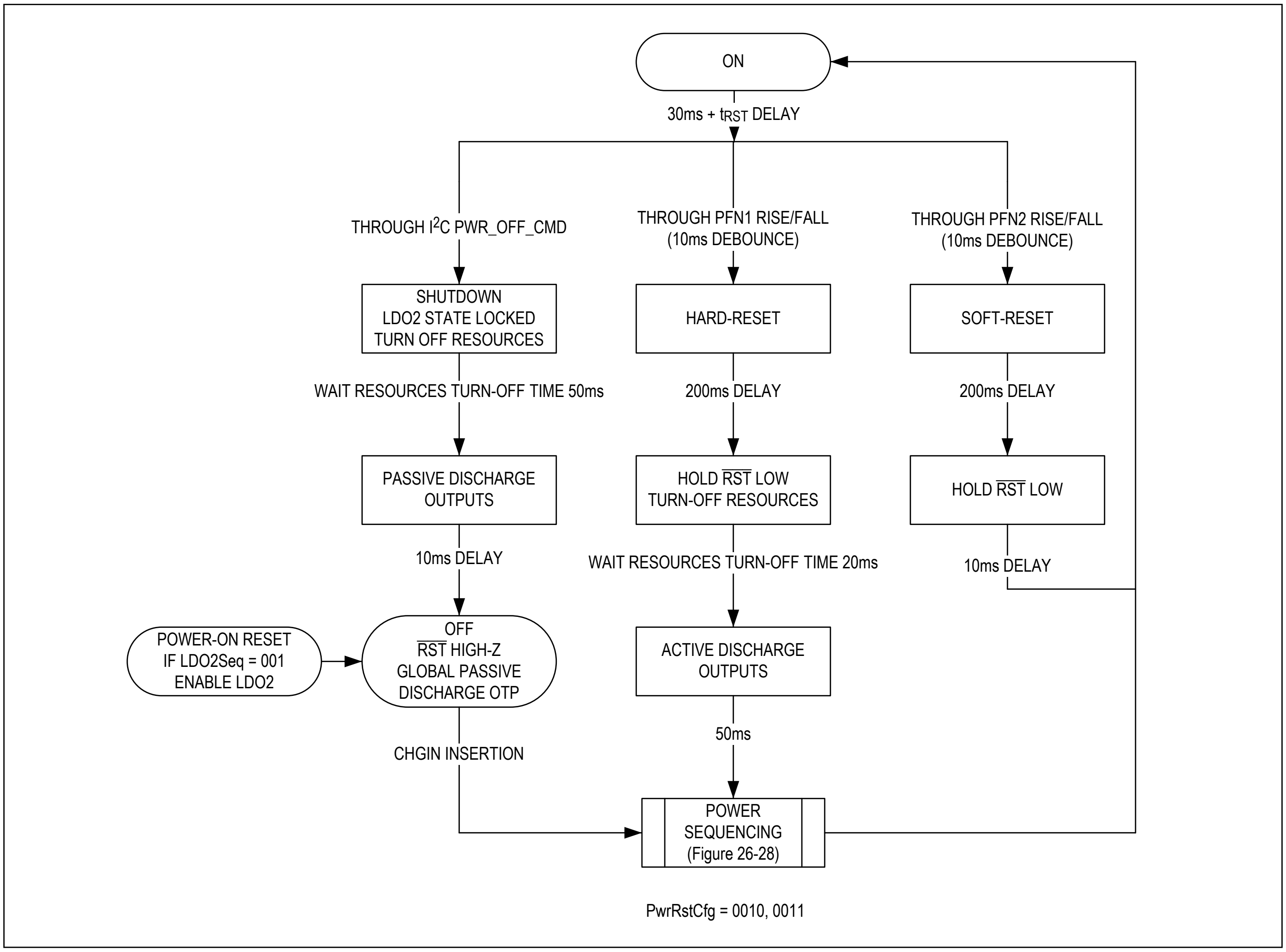


Figure 16. PwrRstCfg 0010, 0011

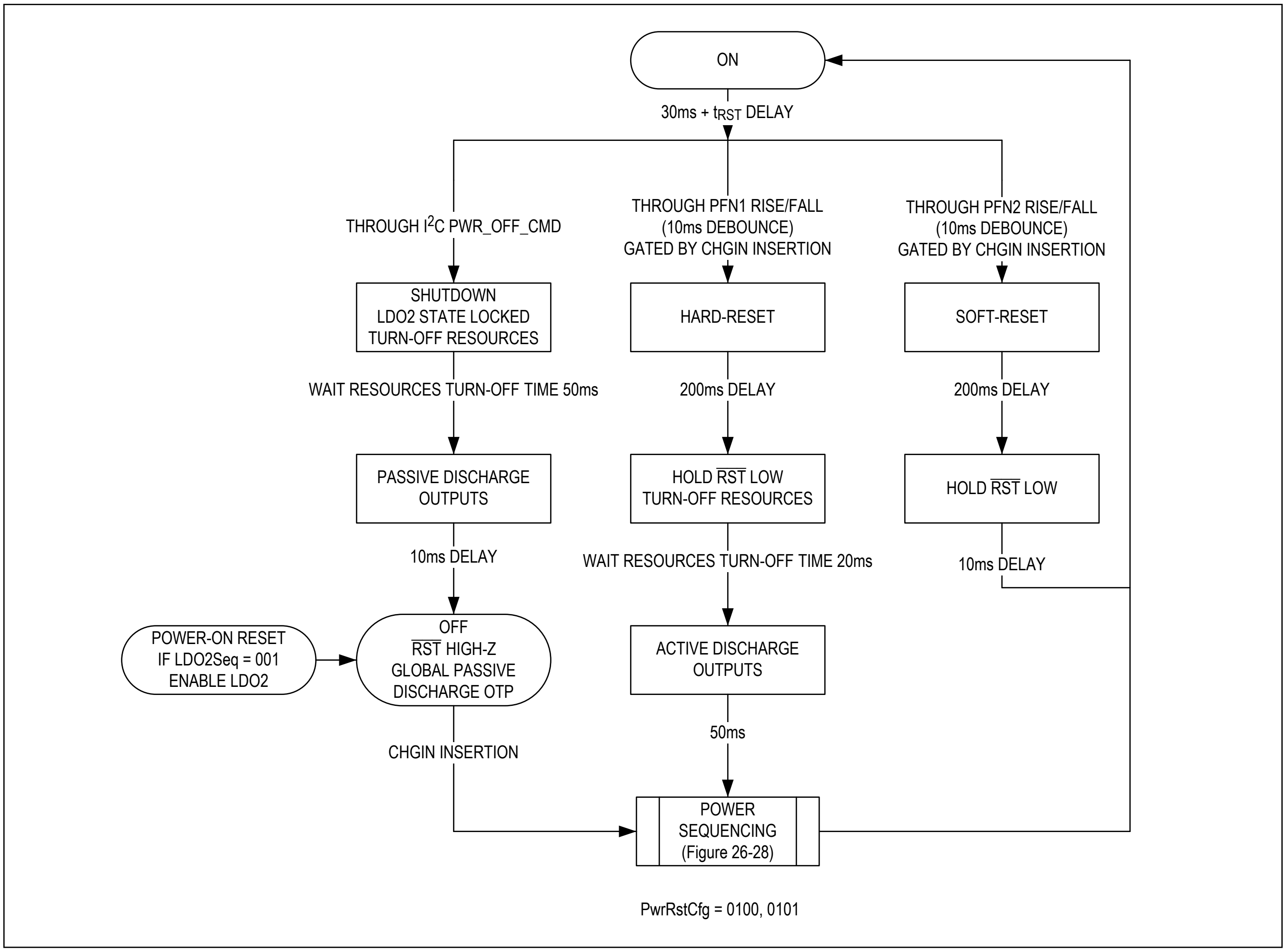


Figure 17. PwrRstCfg 0100, 0101

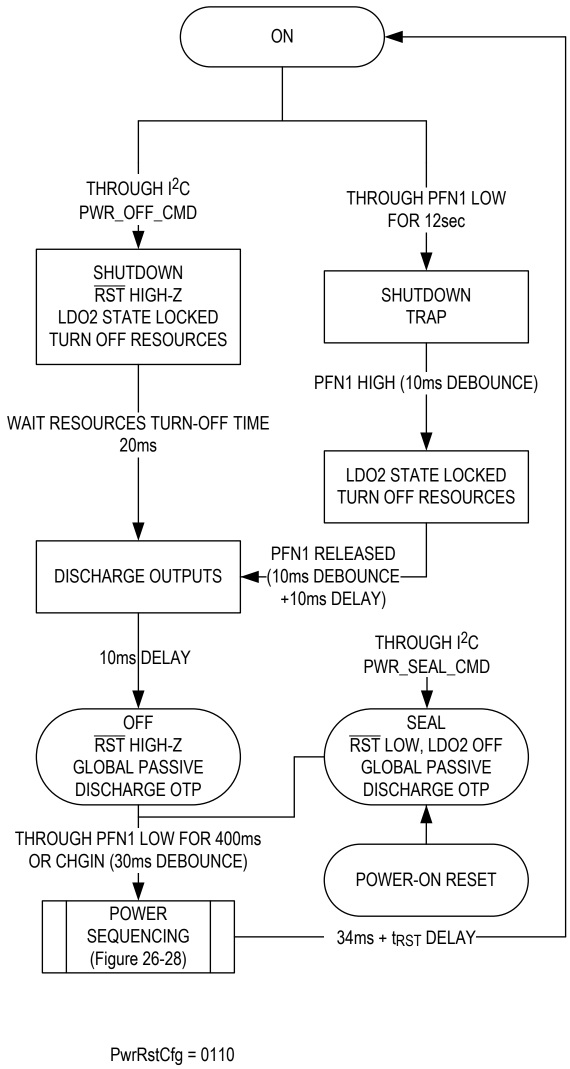


Figure 18. PwrRstCfg 0110

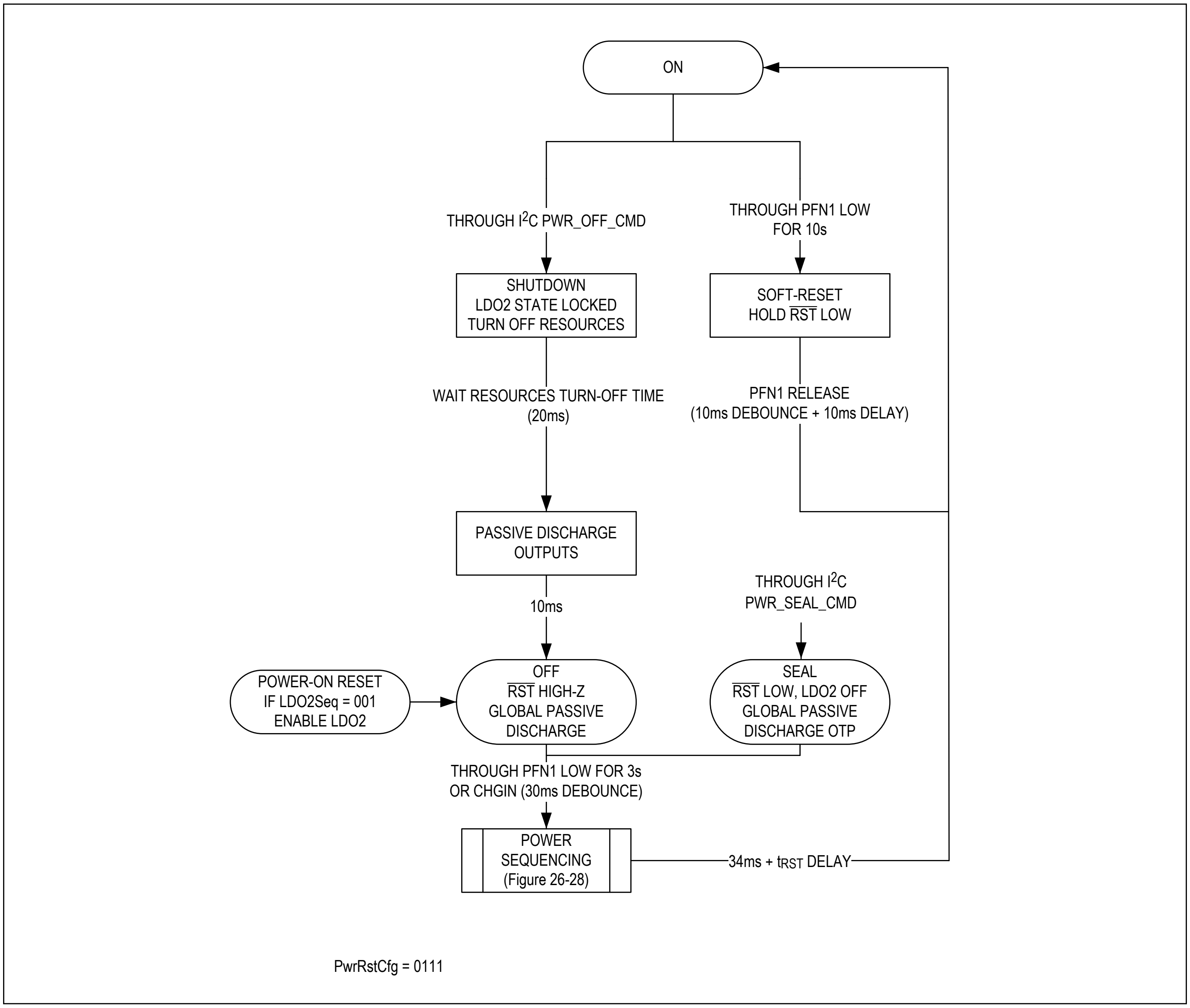


Figure 19. PwrRstCfg 0111

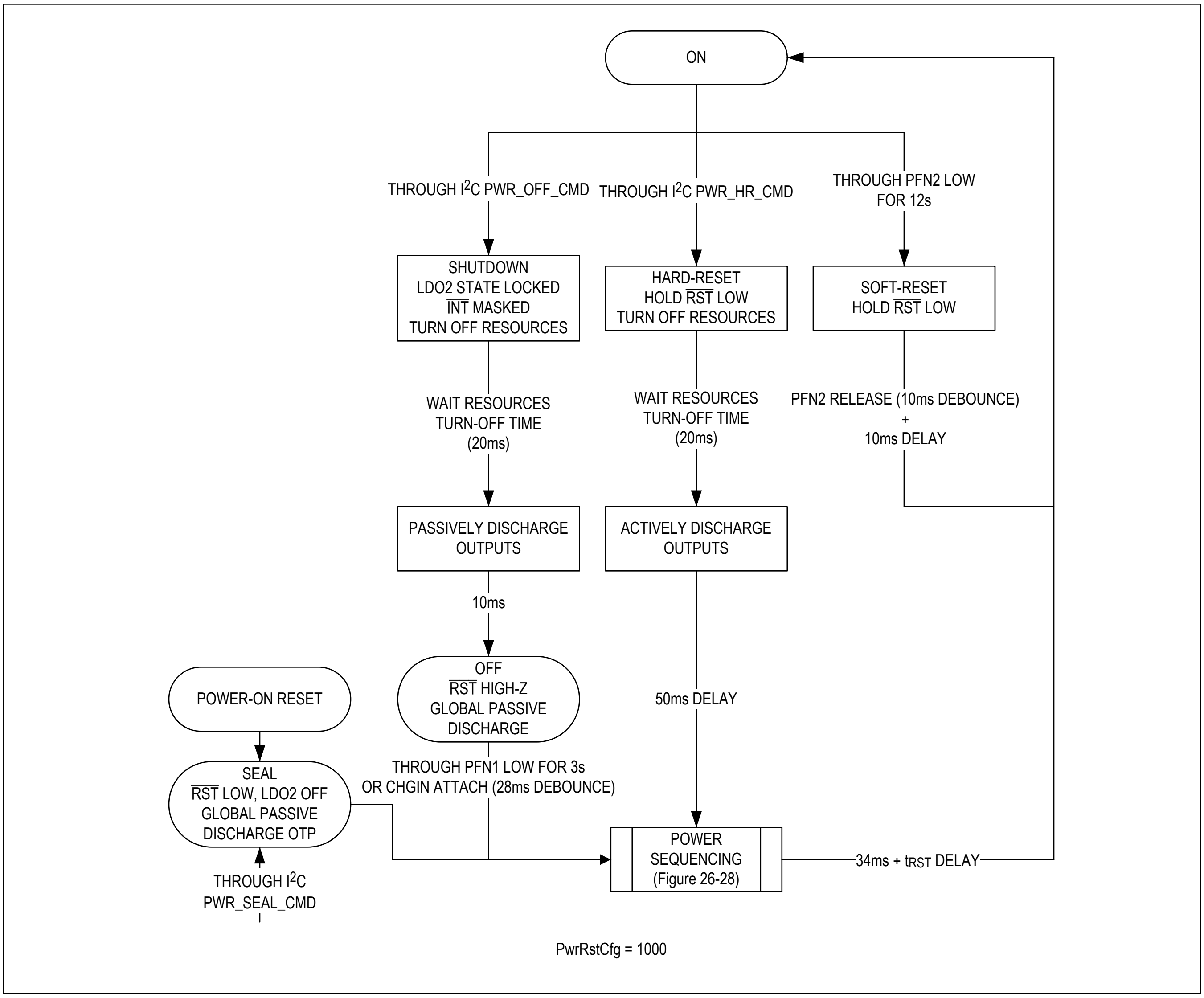


Figure 20. PwrRstCfg 1000

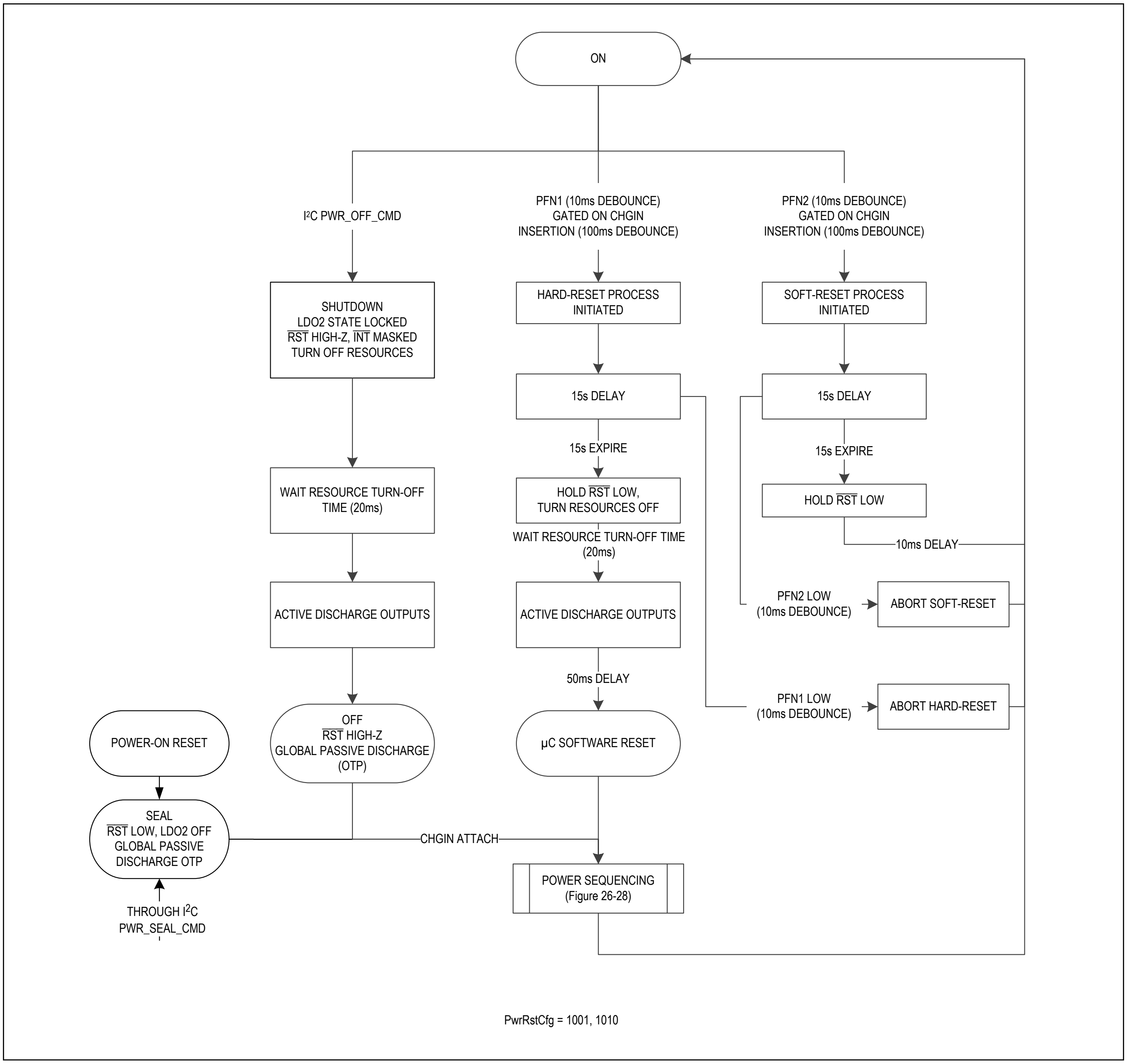


Figure 21. PwrRstCfg 1001, 1010

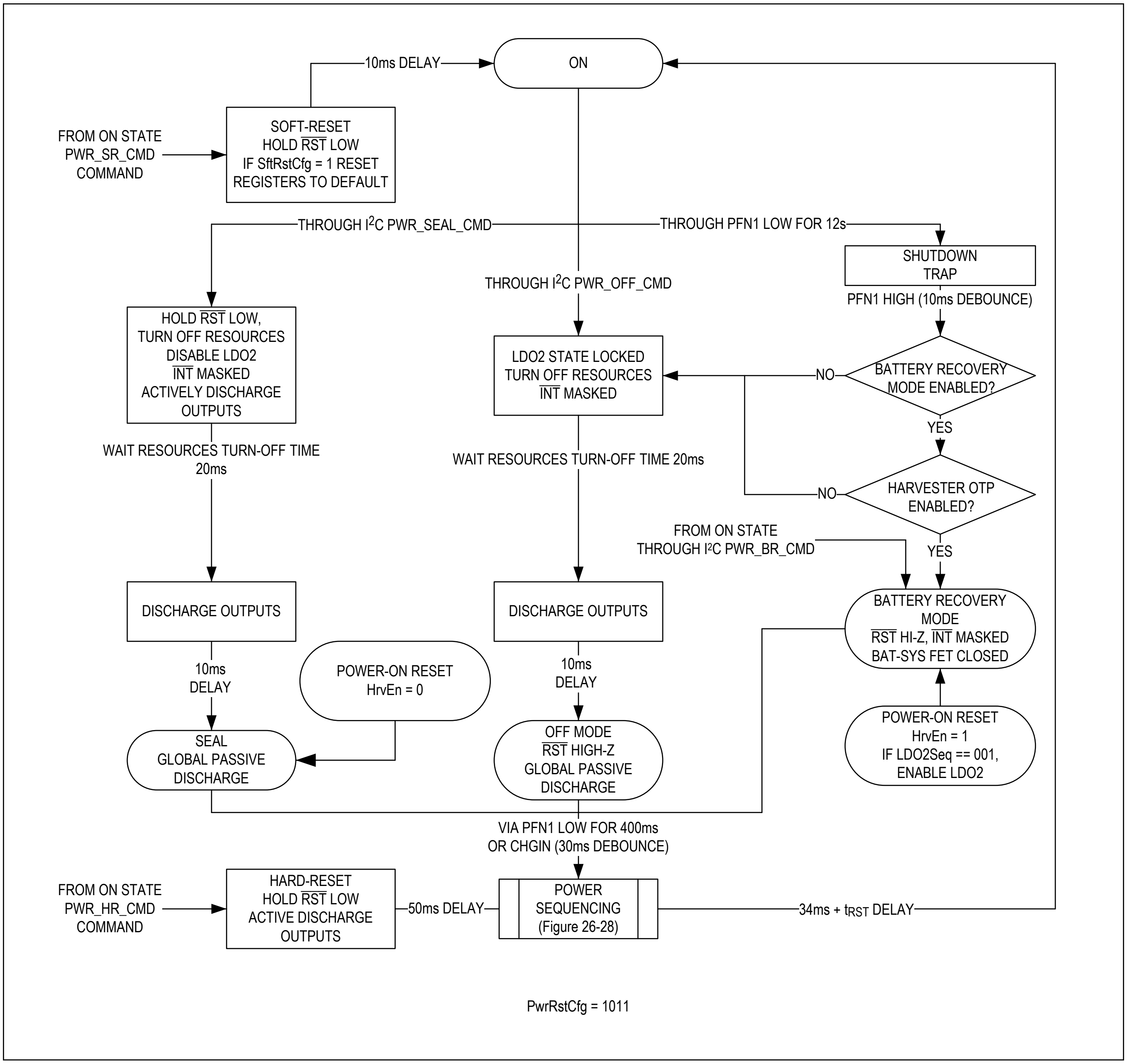


Figure 22. PwrRstCfg 1011

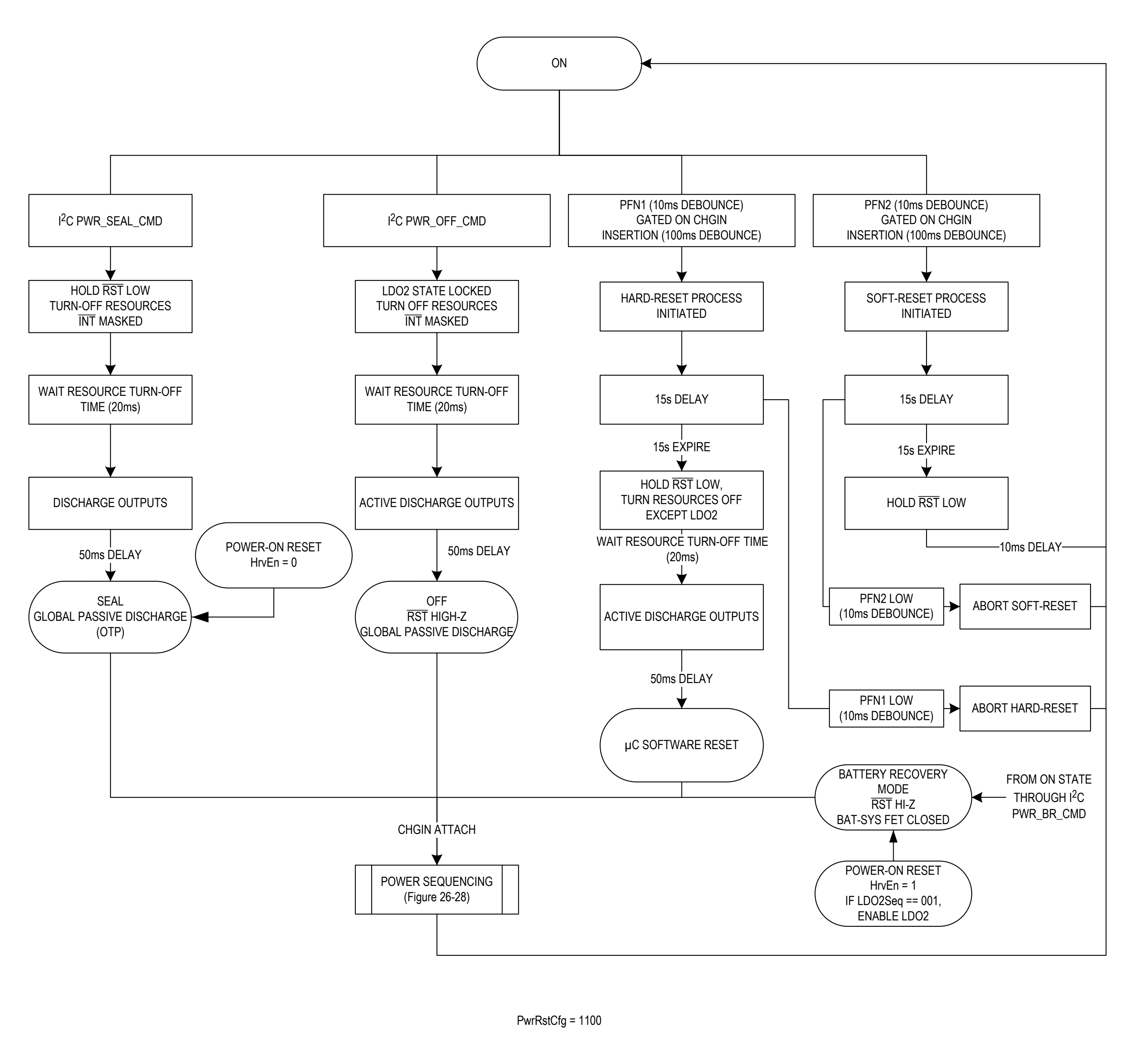


Figure 23. PwrRstCfg 1100

Table 5. PwrRstCfg Settings

PwrRstCfg[3:0]	FIGURE	MODE NAME	BEHAVIOR
0000	Figure 15	ON/$\overline{OFF}$	ON/OFF Mode with 10ms Debounce. PFN1 is the active-high ON/OFF control input. PFN2 is the active-low soft-reset input.
0001	Figure 15	$\overline{ON}$/OFF	ON/OFF Mode with 10ms Debounce. PFN1 is the active-low ON/OFF control input. PFN2 is the active-low soft-reset input.

Table 5. PwrRstCfg Settings (continued)

0010	Figure 16	AON	Always-On Mode. A rising edge on PFN1 generates a hard-reset after a 200ms delay. A rising edge on PFN2 generates a soft-reset after a 200ms delay. The device can only enter the OFF state by writing to the PwrCmd register.
0011	Figure 16	$\overline{AON}$	Always-On Mode. A falling edge on PFN1 generates a hard-reset after a 200ms delay. A falling edge on PFN2 generates a soft-reset after a 200ms delay. The device can only enter the OFF state by writing to the PwrCmd register.
0100	Figure 17	CR High	Always-On Mode. Holding PFN1 high during a CHGIN insertion generates a hard-reset after a 200ms delay. Holding PFN2 high during a CHGIN insertion triggers a soft-reset after a 200ms delay. The device can only enter the OFF state by writing to the PwrCmd register.
0101	Figure 17	CR Low	Always-On Mode. Holding PFN1 low during a CHGIN insertion generates a hard-reset after a 200ms delay. Holding PFN2 low during a CHGIN insertion triggers a soft-reset after a 200ms delay. The device can only enter the OFF state by writing to the PwrCmd register.
0110	Figure 18	$\overline{KIN}$	ON/OFF Through Key Presses. PFN1 is the active-low $\overline{KIN}$ button. PFN2 is the open-drain $\overline{KOUT}$ output, which buffers the $\overline{KIN}$ input. The device enters on mode through a short (400ms) $\overline{KIN}$ press or a CHGIN insertion. The device enters OFF mode through a long (> 12s) $\overline{KIN}$ press or through the PwrCmd register.
0111	Figure 19	CSR1	On/Reset Through Key Presses. PFN1 is the active-low $\overline{KIN}$ button. PFN2 is the open-drain $\overline{KOUT}$ output, which buffers the $\overline{KIN}$ input. The device enters on mode through a long (> 3s) $\overline{KIN}$ press or a CHGIN insertion. A long (> 12s) $\overline{KIN}$ press generates a soft-reset. The device can only enter the off state by writing to the PwrCmd register.
1000	Figure 20	CSR2	On/Reset Through Key Presses. PFN1 is the active-low $\overline{KIN}$ button. The device enters on mode through a long (> 3s) $\overline{KIN}$ press or a CHGIN insertion. A long (> 12s) PFN2 press generates a soft-reset. The device can only enter the off-state by writing to the PwrCmd register.
1001	Figure 21	Custom CR High	Always-On Mode. The device can only enter the on state through a CHGIN insertion. Holding PFN1 high during a CHGIN insertion generates a hard-reset after a 15 second delay. If PFN1 is brought low during this delay (10ms debounce), the hard-reset is aborted. Holding PFN2 high during a CHGIN insertion generates a soft-reset after a 15 second delay. If PFN2 is brought low during this delay (10ms debounce), the hard-reset is aborted.
1010	Figure 21	Custom CR Low	Always-On Mode. The device can only enter the on state through a CHGIN insertion. Holding PFN1 low during a CHGIN insertion generates a hard-reset after a 15 second delay. If PFN1 is brought high during this delay (10ms debounce), the hard-reset is aborted. Holding PFN2 low during a CHGIN insertion generates a soft-reset after a 15 second delay. If PFN2 is brought high during this delay (10ms debounce), the hard-reset is aborted.
1011	Figure 22	$\overline{KIN}$ with OFF/ SEAL	ON/OFF Through Key Presses with OFF/SEAL. PFN1 is the active-low $\overline{KIN}$ button. PFN2 is the open-drain $\overline{KOUT}$ output, which buffers the $\overline{KIN}$ input. The device enters on mode through a short (400ms) $\overline{KIN}$ press or a CHGIN insertion. The device enters OFF mode through a long (> 12s) $\overline{KIN}$ press or through the PwrCmd register.
1100	Figure 23	Custom CR High with OFF/ SEAL	Always-On Mode with OFF/SEAL. The device can only enter the on-state through a CHGIN insertion. Holding PFN1 high during a CHGIN insertion generates a hard-reset after a 15-second delay. If PFN1 is brought low during this delay (10ms debounce), the hard-reset is aborted. Holding PFN2 high during a CHGIN insertion generates a soft-reset after a 15-second delay. If PFN2 is brought low during this delay (10ms debounce), the hard-reset is aborted.
1101-1111	—	RFU	—

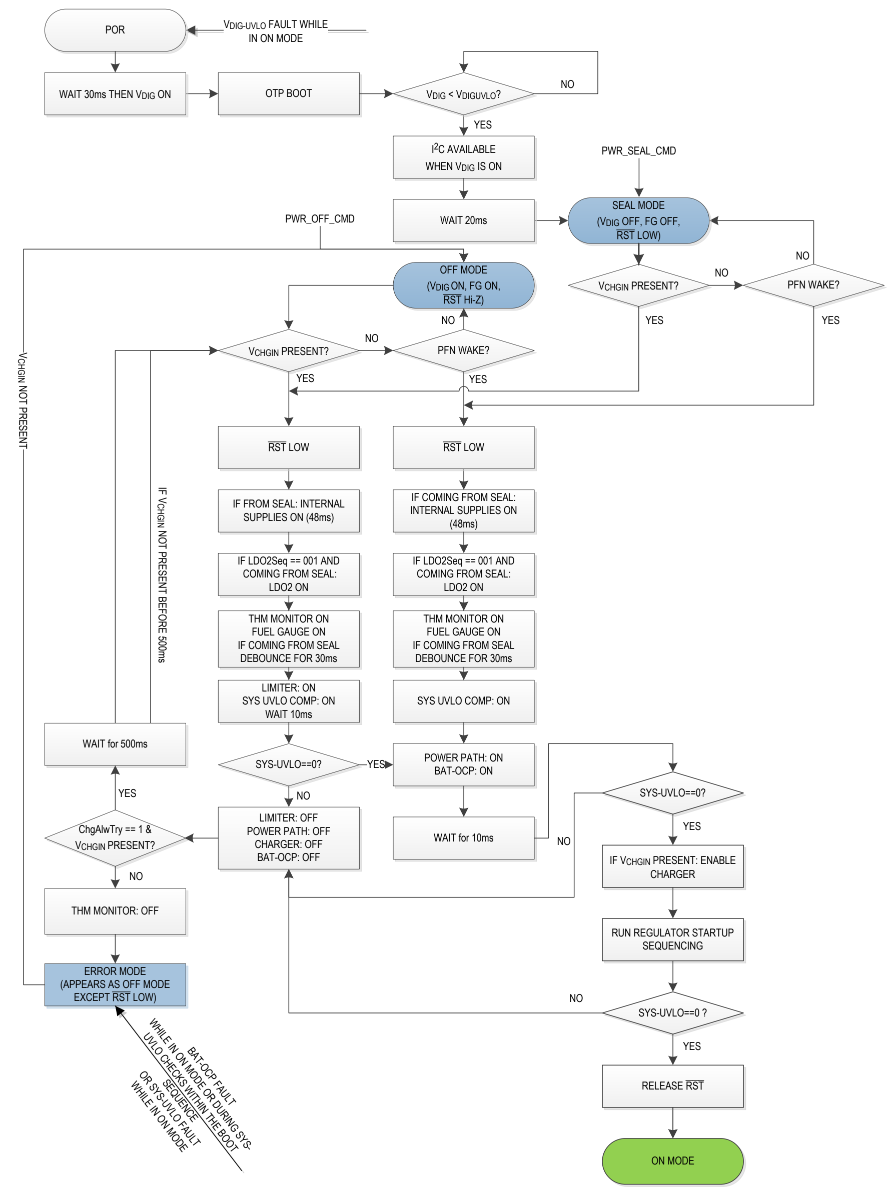


Figure 24. Boot Sequence—Harvester Mode Disabled

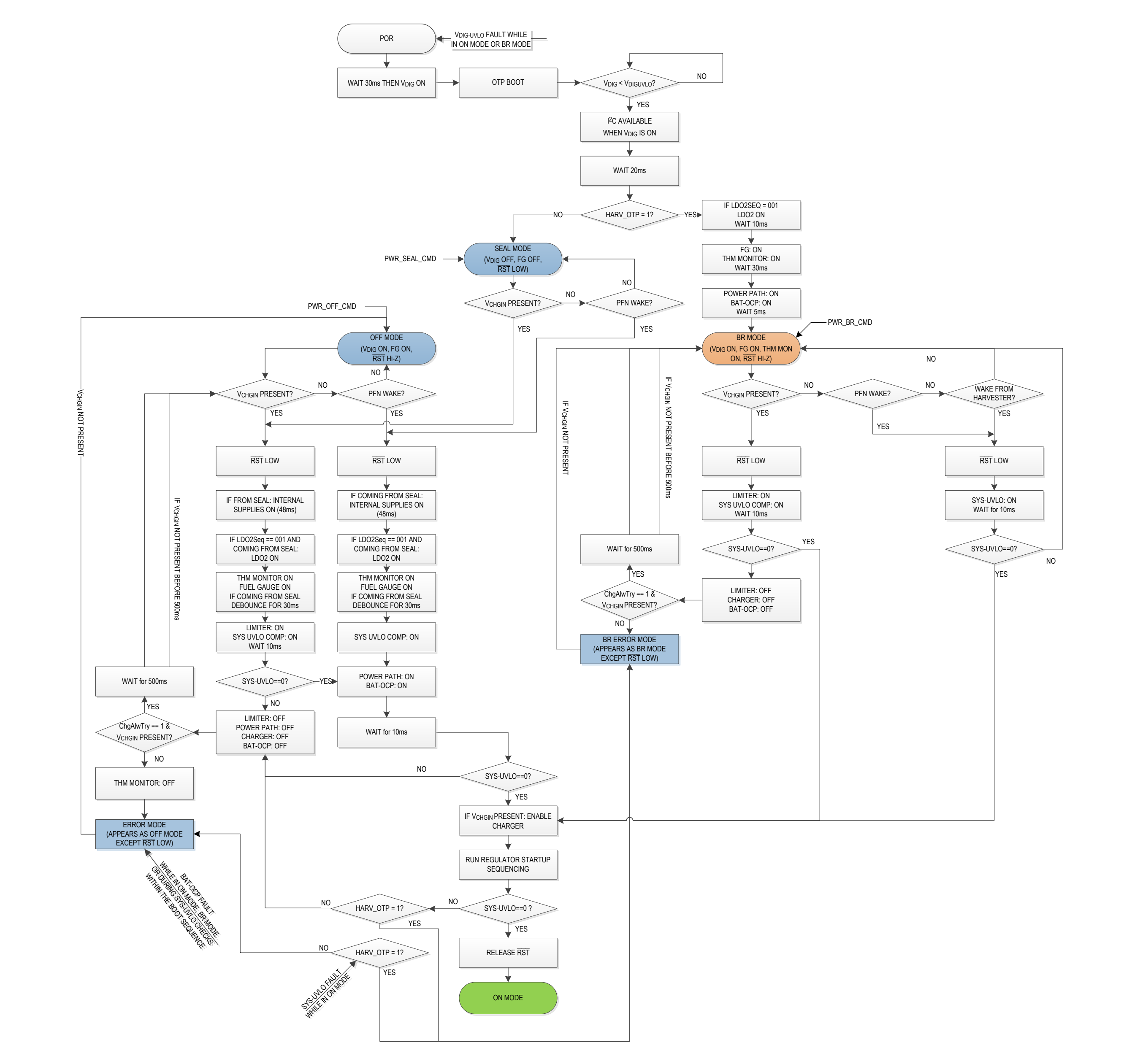


Figure 25. Boot Sequence—Harvester Mode Enabled

PMIC Power Modes

The following sections describe the basic operating modes of the MAX20360.

SEAL Mode

SEAL mode is the lowest-quiescent current mode on the MAX20360. In this mode, all resources are off except the button monitor and V_{CHGIN} insertion detection circuitry.

OFF Mode

The MAX20360 must in some cases power an RTC. OFF mode is the lowest quiescent current mode in which the fuel gauge and the always on LDO are powered. In this mode, the V_{DIG} supply, the button and V_{CHGIN} monitor circuits, and the fuel gauge are on. If LDO2 was on before entering OFF mode or if LDO2Seq = 001 (see bit: *LDO2Seq*), LDO2 is also on in OFF mode.

ON Mode (Versions with HrvEn = 0)

ON mode is the most common operating mode. In ON mode, all regulators are or can be enabled, the fuel gauge is on, and all features are accessible.

Battery Recovery Mode (Versions with HrvEn = 1)

On versions of MAX20360 with HrvEn = 1, MPC7 and MPC6 are permanently reconfigured as “Wake Input” (from Harvester) and “Disable Output” (to Harvester, high-side open-drain to V_{CCINT}), respectively. In battery recovery mode, the part is in the same operating condition as OFF mode; however, in addition the switch between SYS and BAT is closed in order to allow a charging path for recovery from a dead battery situation and the battery thermistor is actively monitored to ensure safe operating conditions. As soon as the battery reaches a threshold which is programmed on the MAX20361 harvester, the MAX20361 sends a wake signal, bringing the part into ON Mode (Versions with HrvEn = 1) as described below. In situations where the THM monitor detects an out-of-bound condition and the charging is considered unsafe, a disable signal is sent to the harvester to halt charging.

ON Mode (Versions with HrvEn = 1)

ON mode with HrvEn = 1 is very similar to ON mode with HrvEn = 0 as described above with the exception that harvester functionality is enabled. In this mode, an ideal diode can be applied to the BAT-SYS relationship. In the default operation, the harvester supplies SYS directly until it is unable to further support the output at which point the battery supplements the supply. This mode also includes the rest of the harvester interaction functionality described in the *MAX20361 Harvester Interaction* section. This behavior can be modified per the HrvBatSys, HrvThmEn and HrvThmDis bit fields (see bits: *HrvBatSys*, *HrvThmEn*, *HrvThmDis*).

Power Sequencing

The sequencing of the switching regulators, load switches, and LDOs during power-on is configurable. See each function’s sequencing bits for details. Regulators and switches can turn on at one of three points during the power-on process: 0% of t_{RST} time after the power-on event, at the time the $\overline{RST}$ signal is released, or at two points in between. The two points between 0% of t_{RST} time delay and the $\overline{RST}$ rising edge are fixed proportionally to the duration of the power-on reset (POR) process boot delay (t_{RST}). The value of the t_{RST} delay ranges from 80ms to 420ms and is stored in the BootDly bits (see bit: *BootDly*). The timing relationship is presented graphically in Figure 26, Figure 27, and Figure 28.

Alternatively, the regulators and switches can remain off by default and turn on manually with an I^2C command after $\overline{RST}$ is released. LDO2 can be configured to be always on.

The SYS voltage is monitored during the power-on sequence. If V_{SYS} falls below V_{SYS_UVLO} during the sequencing process with a valid voltage at CHGIN and ChgAlwTry = 1, the process repeats from the point where SYS was enabled to allow more time for the voltage to stabilize. If there is not a valid voltage at CHGIN, the device returns to the off state to avoid draining the battery. Power is also turned off if BAT experiences a current greater than I_{BAT_OCP} for more than $t_{BAT\_OCP\_RD}$.

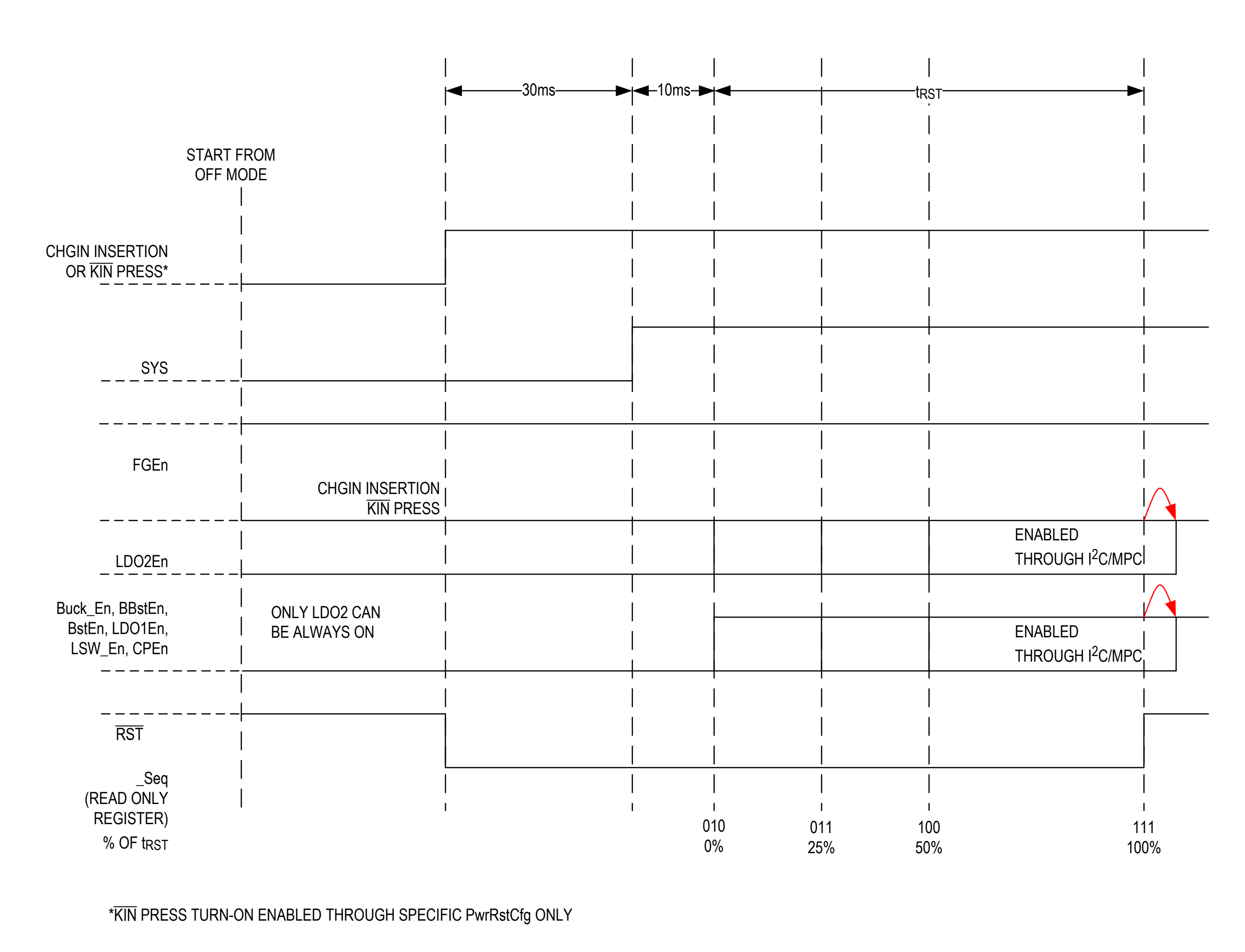


Figure 26. Power Sequencing, HrvEn = 0 from OFF Mode

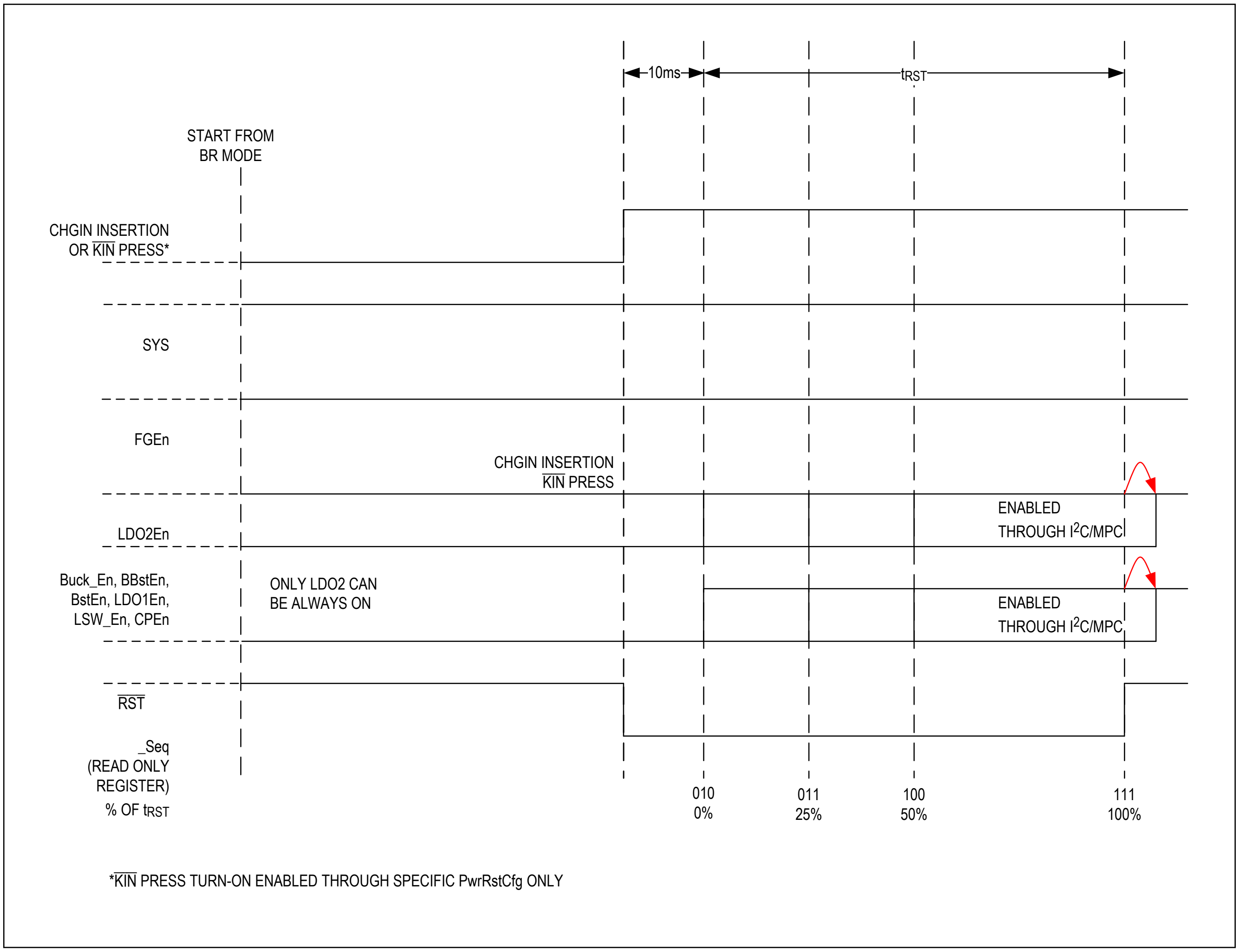


Figure 27. Power Sequencing, HrvEn = 1 from BR Mode

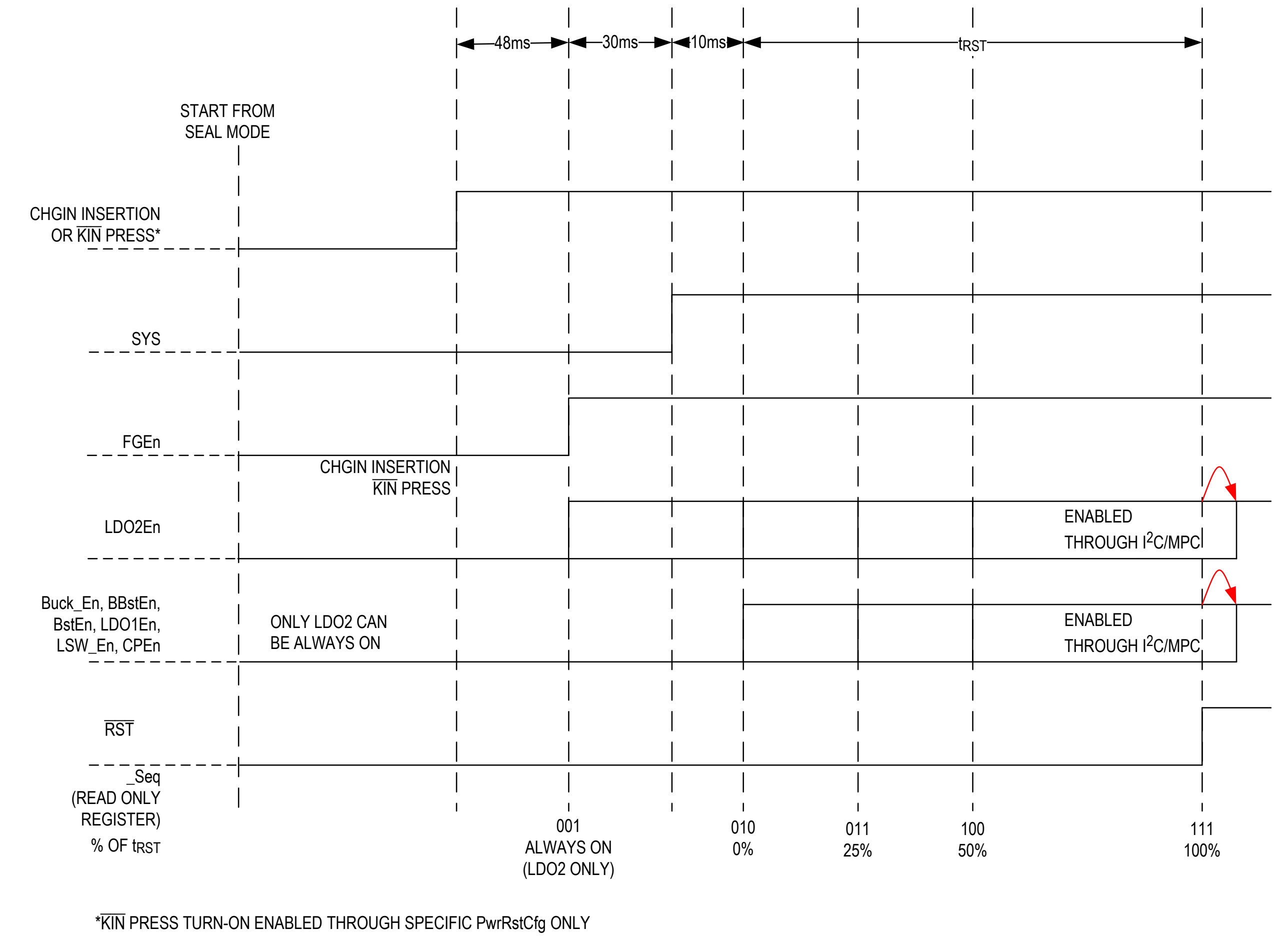


Figure 28. Power Sequencing, from SEAL Mode

System Load Switch

An internal 80mΩ (typ) MOSFET connects BAT to SYS when no voltage source is available on CHGIN. When an external source is detected at CHGIN, this switch opens and SYS is powered from the input source through the input current limiter. The SYS-to-BAT switch also prevents V_{SYS} from falling below V_{BAT} when the system load exceeds the input current limit. If V_{SYS} drops to V_{BAT} due to the current limit (I_{LIM}), the SYS-to-BAT switch turns on so the load is supported by the battery. If the system load continuously exceeds the input current limit, the battery is not charged. This is useful for handling loads that are nominally below the input current limit, but have high current peaks exceeding the input current limit. During these peaks, battery energy is used, but at all other times the battery charges.

Smart Power Selector

The smart power selector seamlessly distributes power from the external CHGIN input to the BAT and SYS nodes. With both an external adapter and battery connected, the smart power selector basic functions are:

- When the system load requirements are less than the input-current limit, the battery is charged with residual power from the input.
- When the system load requirements exceed the input-current limit, the battery supplies supplemental current to the load.
- When the battery is connected and there is no input-current limit, the system is powered from the battery.

Input Limiter

The input limiter distributes power from the external adapter to the system load and battery charger. In addition to the input limiter's primary function of passing power to the system load and charger, it performs several additional functions to optimize use of available power.

Invalid CHGIN Voltage Protection

If CHGIN is above the overvoltage threshold V_{CHGIN_OV}, the device enters overvoltage lockout (OVLO). OVLO protects the MAX20360 and downstream circuitry from high-voltage stress up to +28V. During OVLO, the internal circuit remains powered and an interrupt is sent to the host. The negative voltage protection down to -5.5V disconnects CHGIN and the device is powered only by BAT. The charger turns off and the system load switch closes, allowing the battery to power SYS. CHGIN is also invalid if it is less than V_{BAT}, or less than the V_{CHGIN_DET} threshold. With an invalid input voltage, the SYS-to-BAT load switch closes and allows the battery to power SYS.

CHGIN Input Current Limit

The CHGIN input current is limited to prevent input overload. The input current limit I_{LIM} is I^2C-controlled through paramter ILimCntl (see bit: *ILimCntl*). To accommodate systems with a high inrush current, the limiter includes a blanking time t_{ILIM_BLANK}, I^2C programmable through the parameter ILimBlank (see bit: *ILimBlank*), during which the input current limit increases to I_{LIM_MAX}.

Thermal Limiting

In case the die temperature exceeds T_{CHG_LIM}, the MAX20360 attempts to limit temperature increases by reducing the input current from CHGIN. In particular, the system load has priority over the charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit (T_{CHG_SHDN}), no input current is drawn from CHGIN and the battery powers the entire system load.

Battery Charger

Adaptive Battery Charging

While the system is powered from CHGIN, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent V_{SYS} from collapsing below the maximum between V_{SYS_LIM} that is I^2C programmable through the SysMinVlt parameter (see bit: *SysMinVlt*), and $V_{SYS\_BAT\_REG}$ values. When the charge current is reduced below 50% (I_{FCHG_TEXT} threshold) due to $V_{SYS\_LIM}/V_{SYS\_BAT\_REG}$ or T_{CHG_LIM} limits, the timer clock operates at half speed. When the charge current is reduced below 20% (I_{FCHG_TSUS} threshold) due to $V_{SYS\_LIM}/V_{SYS\_BAT\_REG}$ or T_{CHG_LIM} limits, the timer clock pauses.

Fast Charge Current Setting

The MAX20360 uses an external resistor connected from ISET to GND to set the fast-charge current I_{FCHG}. The precharge (I_{PCHG}) and charge-done, I_{CHG_DONE}, currents are I^2C programmed using IPChg and IChgDone parameters (see bits: *IPChg*, *IChgDone*), respectively, as a percentage of this value. The fast-charge current resistor can be calculated as:

$R_{ISET} = K_{ISET} \times V_{ISET} / I_{FCHG}$

where K_{ISET} has a typical value of 2000A/A and V_{ISET} has a typical value of +1V. The range of acceptable values for R_{ISET} is 4kΩ to 400kΩ. A capacitive load on the ISET pin can cause instability of the charger if the condition (C_{ISET} < 5µs / R_{ISET}) pF is violated.

JEITA Monitoring with Charger Control

To enhance safety when charging lithium-ion batteries, the MAX20360 includes a JEITA compliant temperature monitoring. A resistive divider is formed on THM by attaching a pullup resistor to TPU and connecting the thermistor of a battery-pack (do not exceed 2mA load on TPU). TPU is internally connected internally to V_{DIG} through a switch. The divider output is read by internal comparators when JEITA monitoring is enabled and the resulting temperature measurement places the battery into one of five temperature zones: cold, cool, room, warm, and hot. Charging is always inhibited in cold and hot regions or if the thermistor is not detected while charging behavior is configurable in warm, room, and cool regions using the I^2C-controlled ChgThmEn parameter (see bit: *ChgThmEn*). In particular, the battery regulation voltage can be reduced to the $V_{BAT\_REG\_JTA}$ value using the I^2C-programmed ChgCool/Room/WarmBatReg[1:0] parameters (see bits: *ChgCoolBatReg*, *ChgRoomBatReg*, *ChgWarmBatReg*) while the fast-charge current can be reduced to the I_{FCHG_JTA} value using the I^2C-programmed ChgCool/Room/WarmIFChg parameters (see bits: *ChgCoolIFChg*, *ChgRoomIFChg*, *ChgWarmIFChg*). Charging can also be inhibited in cool and warm regions using ChgThmEn (see bit: *ChgThmEn*). See figures Figure 29, Figure 30, and Figure 31 for representations of the JEITA charging profile in each of the charging phases.

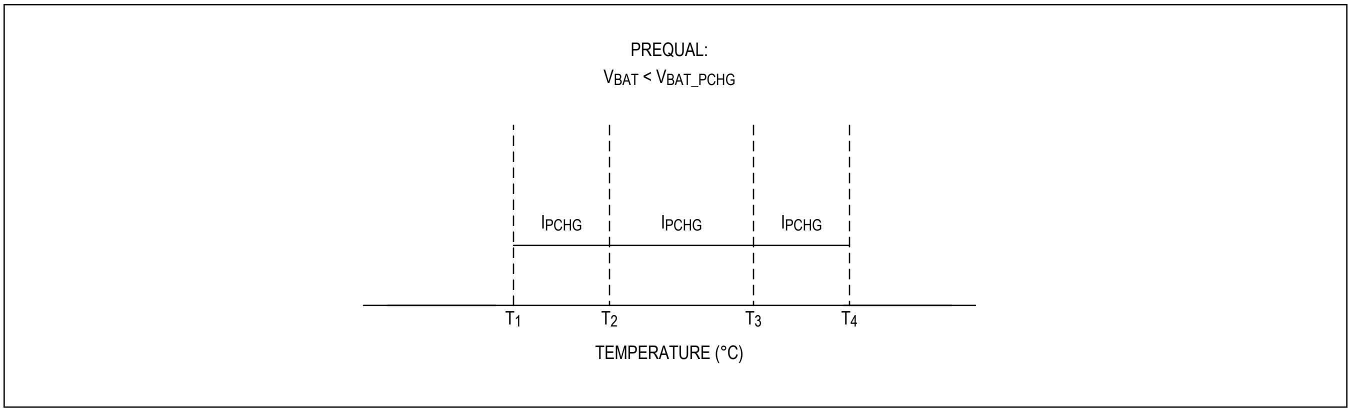


Figure 29. Sample JEITA Pre-Charge Profile

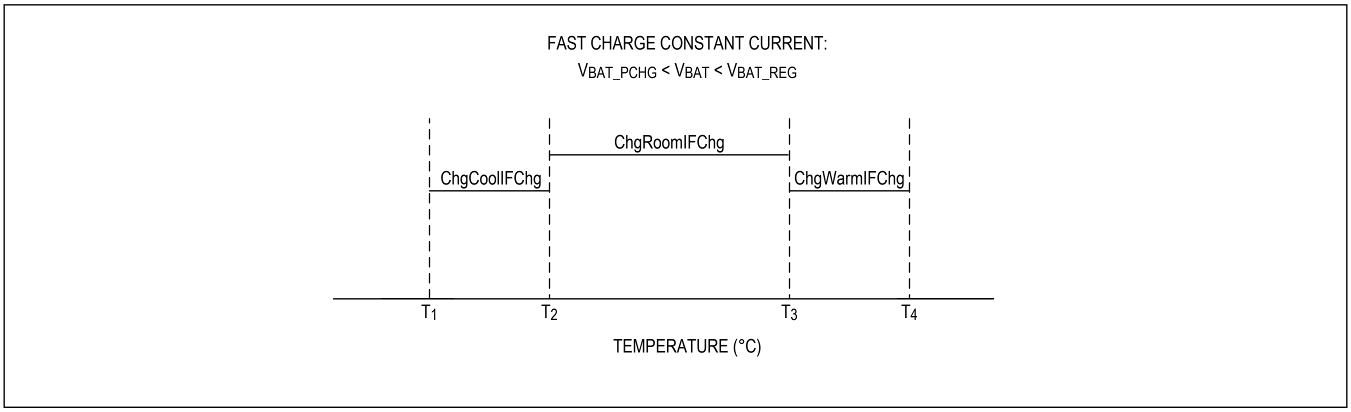


Figure 30. Sample JEITA Fast Charge Profile

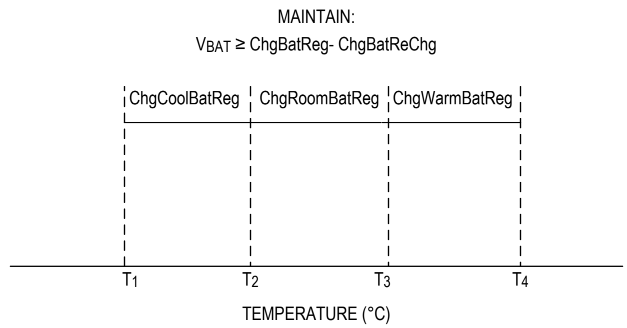


Figure 31. Sample JEITA Maintain Charge Profile

Step Charging

Lithium-ion batteries suffer capacity degradation over their lifetimes. One of the primary causes of degradation over the lifetime of a battery is due to an effect called lithium plating, which describes the formation of metallic lithium on the anode of the battery. Lithium plating has many causes, but one of the most common is when the battery is charged at high rates relative to the capacity of the battery when the battery is at a high state of charge (SOC). To combat this effect, the MAX20360 includes a step-charge function. This function allows the user to select a voltage threshold at which the charge current can be reduced in order to avoid lithium plating and prolong the lifetime of the battery. The settings of this function can be found in the StepChgCfg0 and StepChgCfg1 registers (see bits: *StepChgCfg0*, *StepChgCfg1*). The ChgStepRise (see bit: *ChgStepRise*) field allows the setting of the rising voltage V_{BAT_STPCHG} at which the charge current should be reduced. The ChgIStep (see bit: *ChgIStep*) field sets the percentage I_{FCHG_STPCHG} of the full fast-charge current to which the charger should be set when the battery is above the V_{BAT_STPCHG} value specified with ChgStepRise (see bit: *ChgStepRise*). Lastly, the ChgStepHys (see bit: *ChgStepHys*) field sets the $V_{BAT\_STPCHG\_H}$ hysteresis for the step charge function in order to avoid oscillations in case a high battery impedance causes the voltage to fall a large amount upon reduction of the battery current. If this function is not desirable, set the ChgIStep (see bit: *ChgIStep*) setting to 100% ("111") to disable it.

In case both JEITA and step-charging related fast-charge current reductions are active, the minimum between the two is selected and applied.

Battery Charger State Diagram

A battery charger-state diagram is shown below in Figure 32. User can read ChgStat bits (see bit: *ChgStat*) to know the status of charger.

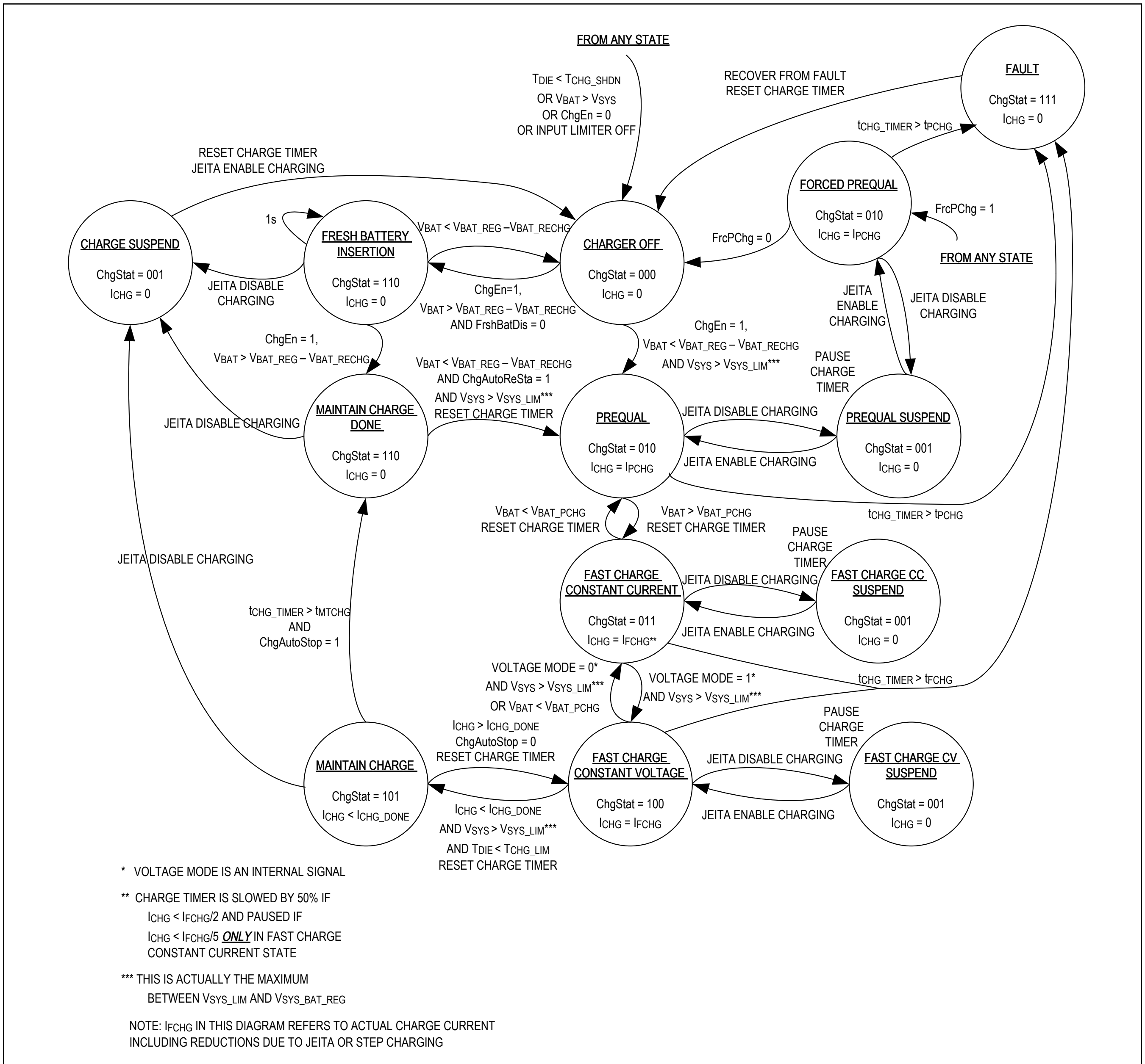


Figure 32. Battery Charger-State Diagram

Battery or Pack Protector Presence Detection

When pack protectors open due to a discharge-related fault, the pack protector turns off the discharge FET, placing a reverse-biased body diode in the discharge path and preventing further discharge. In this state, the system designer can decide that the battery has been damaged and that they would like to prevent a full charge cycle in the future. Even if the system designer does decide that the battery can be recovered, they can have concerns that the diode drop of the pack protector can cause the charger to believe that the battery is above the precharge voltage threshold, which would mean that the fast charge current is applied.

In this scenario, it is useful for the system to understand before starting a full charge cycle whether a pack is present on the BAT node (with an open protector) or if the battery has simply been removed. The MAX20360 contains all of the necessary circuitry to allow the system designer to implement such a check.

One example of a simple algorithm to check for such a condition is to run the below check every time before starting a battery charging cycle:

1. After receiving a UsbOkInt interrupt (see bit: *UsbOkInt*) and before enabling the charger the BAT pulldown resistor by writing BatPD = 1 (see *BatPD*), wait enough time for any BAT capacitance to discharge, then check the BatGood (see bit: *BatGood*) status and disable the BAT pull-down resistor. If BatGood = 1 (see bit: *BatGood*), then the battery is present and charging can resume. If BatGood = 0 (see bit: *BatGood*) indicating that the BAT voltage is below the UVLO threshold either:

a.The battery is not present.

or

b.The pack protector is open.

2. Now turn the charger on in a “forced precharge” mode by writing FrcPChg = 1 and ChgEn = 1 (see bits: *FrcPChg*, *ChgEn*) simultaneously and check BatRegDone (see bit: *BatRegDone*). If BatRegDone = 1 meaning that $V_{BAT} \geq V_{BAT\_REG}$, it means that the battery is not present since if it were, the BAT voltage would only be allowed to rise one diode drop above the actual battery voltage. If instead BatRegDone = 0, the battery must be present and forced precharge mode should be maintained at least long enough to unlock the pack protector.

SAR ADC/Monitor Mux

In order to simplify system monitoring, the MAX20360 includes a voltage monitor multiplexer (MUX). The MUX, which is I^2C controlled using the IVMONCntl parameter (see bit: *IVMONCntl*) in the PMIC register map, connects the IVMON pin to the scaled value of one of the seven voltage regulators, BAT, or SYS. A resistive divider scales the selected voltage to one of four ratios determined by IVMONRatioConfig (see bit: *IVMONRatioConfig*). Because the MUX can only tolerate voltages up to +5.5V, CHGIN, CPOUT and BSTOUT are not available on IVMON. Additionally, the ISET voltage is available to monitor the charging current according to the following equation:

$$I_{CHG} = \frac{\left(K_{ISET} \times V_{ISET} \times RED\_FCT\right)}{R_{ISET}}$$

where:

I_{CHG} = Actual charging current flowing into BAT

K_{ISET} = Gain factor (2000A/A)

V_{ISET} = Voltage read from monitor mux.

RED_FCT = Eventual reduction factor can be due to JEITA and/or step-charging (see bits: *ChgIStep*, *ChgCoolIFChg*, *ChgRoomIFChg*, *ChgWarmIFChg* parameters). If neither JEITA nor step-charging current reduction is active, RED_FCT is equal to 1.

R_{ISET} = Nominal resistor value on ISET

The MAX20360 also contains an internal ADC that can be used to read the voltage rails and performs system tasks such as SYS tracking for automatic level compensation (ALC) during haptic driver operations. Manual ADC measurements are initiated by first selecting a channel by writing to ADCSel (see bit: *ADCSel*) in the Haptic Driver/ADC register map. The measurement is then launched by writing a 1 to ADCConvLnch (see bit: *ADCConvLnch*). Once the measurement is complete, an ADCEOCInt interrupt (see bit: *ADCEOCInt*) is set to inform the system that the value is available for read in the ADCAvg, ADCMin, and ADCMax register fields (see bits: *ADCAvg*, *ADCMin*, *ADCMax*). Averaging of measurements can be performed by setting the number of measurements to average using the ADCAvgSiz register field (see bit: *ADCAvgSiz*). The ADC can also measure the IVMON voltage when the MUX is enabled with a 1:1 ratio. The full-scale range of the ADC for different voltage rails is detailed in Table 6.

Table 6. ADC Full-Scale Range

VOLTAGE RAIL	AVAILABLE RANGE (V)	CONVERSION (V)
V_{HDIN}	0 to +5.5	(ADC___[7:0] x 5.5V)/255
V_{IVMON} (use IVMONRatioConfig = 00) (see *IVMONRatioConfig*)	0 to +5.5	(ADC___[7:0] x 5.5V)/255
CHGIN	+3 to +8.25	(ADC___[7:0] x 8.25V)/255
CPOUT	+3 to +8.25	(ADC___[7:0] x 8.25V)/255
BSTOUT	+3 to +21	(ADC___[7:0] x 21.0V)/255

Haptic Driver

The MAX20360 features a versatile, integrated haptic driver. The driver allows for real-time control of haptic devices through PWM or I^2C as well as the ability to run haptic patterns from internal RAM. For added flexibility, the driver is capable of driving both linear resonant actuator (LRA) and eccentric rotating mass (ERM) actuators.

Eccentric Rotating Mass (ERM)

An ERM is the simplest haptic actuator to drive. The driving signal is taken directly as the PWM output of an integrated H-bridge, allowing for bidirectional operation of the actuator. To configure the MAX20360 to drive an ERM, the HptSel bit (see bit: *HptSel*) must be set to 0.

Linear Resonant Actuator (LRA)

Unlike the on-off control of an ERM, LRAs require a sinusoidal driving signal. The MAX20360 realizes this with a Class-D amplifier that converts the driver input to a sinusoidal output.

An LRA's vibration magnitude is maximized when the driving signal matches the LRA's resonant frequency. To ensure the haptic driver closely tracks this frequency, the MAX20360 includes an auto-resonance tracking feature that measures the back-electromotive force (BEMF) of the LRA to track the resonance of the actuator. The resonant tracking feature should remain enabled any time an LRA is driven. Resonance tracking is enabled by setting the EmfEn bit to 1 (see bit: *EmfEn*). The range of resonant frequencies that are tracked is clamped by the driver to be no lower than max(200kHz/IniGss[11:0], 100Hz) and no greater than min(800kHz/IniGss[11:0], 1kHz). See the description of IniGss (see bit: *IniGss*) in the register map for calculation of frequency. This mitigates the risk of audible noise during a fault event.

To select LRA mode, set the HptSel bit to 1 (see bit: *HptSel*).

LRA Braking

The haptic driver features a braking function to efficiently stop or reverse the direction of an LRA. Each time the driving polarity is reversed, the BEMF measuring configurations are overridden by the values in BrkLpGain, BrkCyc, and BrkWdw for BrkCyc number of half cycles (see bits: *BrkLpGain*, *BrkCyc*, *BrkWdw*). This allows the haptic driver to optimize the redetection of the BEMF after the sudden change in direction.

Additionally, the haptic driver can automatically detect the optimal braking time when running patterns in the RAMHP and ETRG modes. When the RAM pattern reaches a brake sample (nLSx = 00 and RPTx = 0000) (see bits: *nLSx*, *RPTx*), or when the ETRG pattern reaches the brake amplitude, the haptic driver measures the LRA's BEMF amplitude centered about either two or four sample points of the sine wave (depending on AutoBrkPeakMeas setting) (see bit: *AutoBrkPeakMeas*). If the absolute value of the BEMF is lower than the threshold AutoBrkMeasTh (see bit: *AutoBrkMeasTh*) for more than half of the duration of AutoBrkMeasWdw (see bit: *AutoBrkMeasWdw*) for a number of consecutive sample points where BEMF amplitude is measured (set by AutoBrkMeasEnd, see bit: *AutoBrkMeasEnd*), then the driver determines that the BEMF is sufficiently small and driving stops.

Note that all LRA registers except those that set the full-scale voltage and initial guess for the resonant frequency of the LRA should be left at their defaults for most actuators. The only exceptions are that EmfSkipCyc (see bit: *EmfSkipCyc*) should be written to 0 for optimal performance and when an LRA with a very fast time constant is in use, the AutoBrkPeakMeas (see bit: *AutoBrkPeakMeas*) might need to be changed to 1 in order to accommodate that LRA's characteristics.

Automatic Level Compensation

Because V_{HDIN} can vary over time, the driver must adjust its output duty cycle to maintain a constant reference to the full-scale voltage. An automatic level compensation (ALC) function measures V_{HDIN} and handles this adjustment. ALC can be enabled by setting the AlcEn bit (see bit: *AlcEn*) to 1 and uses the MAX20360 internal ADC to monitor V_{HDIN}. The ALC function then scales the haptic driver duty cycle as needed to maintain the programmed driver amplitude. If ALC is not enabled, V_{HDIN} is assumed to be Vfs (see bit: *Vfs*).

Haptic UVLO

Additionally, if AlcEn = 1 (see bit: *AlcEn*), V_{HDIN} is measured after the driver is enabled but prior to starting a vibration. At any moment, if V_{HDIN} goes below the maximum between the value programmed through HDINDisTh (see bit: *HDINDisTh*) and the V_{HDIN_UVLO} threshold, the vibration event is aborted and the haptic driver is locked. See the *Haptic Driver Lock* section for details regarding restarting vibration if a haptic UVLO condition is reached.

The time required to perform the initial V_{HDIN} measurement, as well as other startup delays, results in a small initial latency of the haptic driver. To avoid partial pattern skipping in real-time modes, vibration patterns should be provided at least t_{HD_START} after enabling the desired real-time vibration mode (PPWM or RTI2C).

Driver Amplitude

The haptic driver features a configurable voltage basis for the amplitude of the driving signal. Setting this basis, referred to as the full-scale voltage (V_{FS}), configures the maximum amplitude of the driver output. It is set using Vfs (see bit: *Vfs*) and has a range of 0V to 5.5V (LSB = 21.57mV). Since the H-bridge is supplied by V_{HDIN}, the actual full-scale voltage of the driver at any given moment is the minimum of the value stored in Vfs (see bit: *Vfs*) and V_{HDIN}.

Once V_{FS} has been set, all driver amplitudes are scaled as a percentage of the full-scale voltage. The resolution of the amplitude is always $V_{HDIN}/128$. Therefore, the effective resolution of the amplitude scales with the V_{FS}/V_{HDIN} ratio. For example, if $V_{FS} = V_{HDIN}/2$, the effective resolution is 6 bits.

Vibration Timeout

A vibration timeout parameter is programmable through I^2C. If a vibration lasts longer than the programmed timeout period, the vibration is aborted. The timeout period is stored in DrvTmo (see bit: *DrvTmo*) (LSB = 1s). Writing code “000000” disables the timeout function. See the *Haptic Driver Lock* section for details regarding restarting vibration if a timeout is reached.

Overcurrent/Thermal Protection

The haptic driver also includes overcurrent and thermal shutdown protection. While the haptic driver is active, the MAX20360 monitors the current from DRP and DRN. If overcurrent protection is enabled (HptOCProtDis = 0) (see bit: *HptOCProtDis*) and the DRP or DRN current exceeds I_{HD_OCP}, the haptic driver issues a fault, aborts vibration, and enters the locked state.

Thermal protection allows the MAX20360 to immediately shut down the haptic driver should the die temperature exceed T_{HD_SHDN}. This feature is enabled by setting HptThmProtDis = 0 (see bit: *HptThmProtDis*).

See the *Haptic Driver Lock* section for details regarding restarting vibration if an overcurrent or overtemperature condition is reached.

Haptic Driver Lock

If the MAX20360 detects a fault in the haptic driver, vibrations in progress are aborted and the haptic driver is locked by the haptic fault locking function. The user must manually set the HptFltUnlock bit (see bit: *HptFltUnlock*) in order to run a new vibration attempt. A fault occurs under any of the following conditions: V_{HDIN} drops below the threshold programmed in HDINDisTh (see bit: *HDINDisTh*) or below V_{HDIN_UVLO}, an overcurrent is detected on DRN or DRP (see bits: *HptDRPOCPLow*, *HptDRNOCPLow*, *HptDRPOCPHigh*, *HptDRNOCPHigh*), the die temperature exceeds the thermal protection threshold HptThm (see bit: *HptThm*), or a vibration duration exceeds the timeout period stored in DrvTmo (see bit: *DrvTmo*). Writing HptFltUnlock (see bit: *HptFltUnlock*) to 1 clears the fault and automatically clears the HptFltUnlock bit to 0.

Interface Modes

There are a total of four interface modes for controlling the haptic driver. These include two real-time modes and two stored memory modes. The haptic driver mode is set through HptDrvMode (see bit: *HptDrvMode*). Selecting an operation mode also enables the driver. In addition, HptDrvClkEn (see bit: *HptDrvClkEn*) must be set and kept to 1 before setting HptDrvMode (see bit: *HptDrvMode*) and for the whole duration of vibration. Once the vibration finishes, HptDrvMode (see bit: *HptDrvMode*) must be set to “00000” before the haptic driver can be disabled by setting HptDrvClkEn = 0 (see bit: *HptDrvClkEn*) for power savings. In all cases haptic patterns must begin with driving in the positive direction.

Pure-PWM (PPWM)

PPWM mode offers real-time control of the haptic driver. Patterns are generated by applying a PWM signal to the MPC_ pin selected by HptDrvMode (see bit: *HptDrvMode*). The duty cycle of the applied signal determines the amplitude of the driving signal, scaled by Vfs (see bit: *Vfs*). The driving direction is centered to about a 50% duty cycle. A duty cycle of 0% to 47.5% produces a 100%Vfs to 0%Vfs amplitude in the negative direction and a duty cycle of 52.5% to 100% produces a 0%Vfs to 100%Vfs amplitude in the positive direction (see bit: *Vfs*). The region between 47.5% and 52.5% duty cycle is a dead zone and inputs within this range correspond to a null output. All patterns must begin with driving in the positive direction (duty cycle between 52.5% to 100%).

A timeout feature prevents idle PWM inputs from causing unwanted vibrations of the haptic motor. If the input signal remains at 0% duty cycle or 100% duty cycle for more than 2.56ms, the output is null and vibration stops. As such, the MPC_ input must remain dynamic to produce a continuous output.

Real-Time I^2C (RTI^2C)

Similar to PPWM mode, RTI^2C mode offers real-time control of the haptic driver. The HptRTI2CPat register (see register: *HptRTI2CPat*) determines the amplitude of the output signal. The lower seven bits of the register (HptRTI2CPat[6:0]) set the amplitude as a percentage of V_{FS} and the MSB (HptRTI2CPat[7]) sets the direction of rotation. 100% amplitude, reverse drive, for example, is produced by setting HptRTI2CPat to 0x7F (0b01111111).

Once RTI^2C mode is enabled through HptDrvMode (see bit: *HptDrvMode*), the haptic driver continuously outputs the amplitude and direction defined by the latest data in HptRTI2CPat (see bit: *HptRTI2CPat*). In order to generate haptic patterns, the HptRTI2CPat register must receive new data. All patterns must begin with driving in the positive direction (MSB of initial write to HptRTI2CPat = 0).

External Triggered Stored Pattern (ETRG)

In ETRG mode, a rising edge on an MPC_ pin or a 0-to-1 transition of the HptExtTrig bit (see bit: *HptExtTrig*) initiates a vibration sequence. The sequence is contained in six registers and comprises an overdrive (startup) amplitude, active drive amplitude, braking amplitude, and the duration of each driving behavior.

Amplitudes contained in HptETRGOdAmp, HptETRGActAmp, and HptETRGBrkAmp (see bits: *HptETRGOdAmp*, *HptETRGActAmp*, *HptETRGBrkAmp*) follow the same format as HptRTI2CPat (see bit: *HptRTI2CPat*) (i.e., the lower-seven bits store the amplitude as a percentage of V_{FS} and the MSB determines the direction).

The trigger input is selected when the driver enters ETRG mode through HptDrvMode (see bit: *HptDrvMode*). In order to properly register the rising edge, the trigger signal must remain high for a few clock cycles of the driver.

Once the sequence begins, the haptic driver follows the duration values stored in HptETRGOdDur, HptETRGActDur, and HptETRGBrkDur (see bits: *HptETRGOdDur*, *HptETRGActDur*, *HptETRGBrkDur*). It is possible, however, to extend the active drive time by leaving the trigger high longer than the time specified in HptETRGActDur (see *HptETRGActDur*). Doing so causes the driver to output the amplitude stored in HptETRGActAmp (see bit: *HptETRGActAmp*) until a falling edge is detected. Once the trigger signal falls low, the brake sequence executes. All patterns must begin with driving in the positive direction (MSB of HptETRGOdAmp = 0, see bit: *HptETRGOdAmp*).

RAM Stored Haptic Pattern (RAMHP)

The final method of controlling the haptic driver is RAMHP mode. The MAX20360 contains an internal 256 x 24-bit RAM in which haptic patterns are stored. By storing haptic sequences in RAM at startup, the driver can perform sophisticated haptic sequences upon receipt of a trigger signal as in ETRG mode. The direct I^2C register HptRAMPatAdd (see bit:

HptRAMPatAdd) specifies the RAM address where the sequence begins.

RAM should be loaded when the MAX20360 comes out of OFF/SEAL mode. To write data to the RAM, the HptRAMEn (see bit: HptRAMEn) must first be set high. Next, writing a value to the direct register HptRAMAdd (see bit: HptRAMAdd) specifies the RAM address in which data written to HptRAMDataH, HptRAMDataM, and HptRAMDataL is store (see bit: HptRAMDataH, HptRAMDataM, HptRAMDataL). It is possible to read back data from RAM. Writing an address to HptRAMAdd (see bit: HptRAMAdd), then initiating an I^2C read transaction of the HptRAMDataH, HptRAMDataM, and HptRAMDataL registers allow readback of the three bytes stored in the RAM address. RAM read and write procedures are depicted graphically in Figure 33. Note that all patterns must begin with driving in the positive direction (AmpSign of first RAM address in a pattern = 0).

A haptic pattern is composed of multiple pattern samples. Pattern samples define the amplitude, duration, wait time, transition, and repetition of a segment of a haptic pattern. These samples are defined in three bytes and written to RAM through HptRAMDataH, HptRAMDataM, and HptRAMDataL. HptRAMDataH (see bit: HptRAMDataH) contains the sign of the sample's amplitude (AmpSign), the upper-five bits of the amplitude (Amp[6:2]), and instructions to the haptic driver on handling the pattern sample (nLSx). HptRAMDataM (see bit: HptRAMDataM) contains the lower two bits of the sample's amplitude (Amp[1:0]), the duration of the sample (Dur), and the upper bit of the wait time before the next sample in the pattern (Wait[4]). HptRAMDataL (see bit: HptRAMDataL) contains the lower four bits of the wait time (Wait[3:0]) and the repetition behavior (RPTx). Table 7 describes the definition of a pattern sample and Figure 34 and Figure 35 provide a sample haptic pattern with a corresponding waveform.

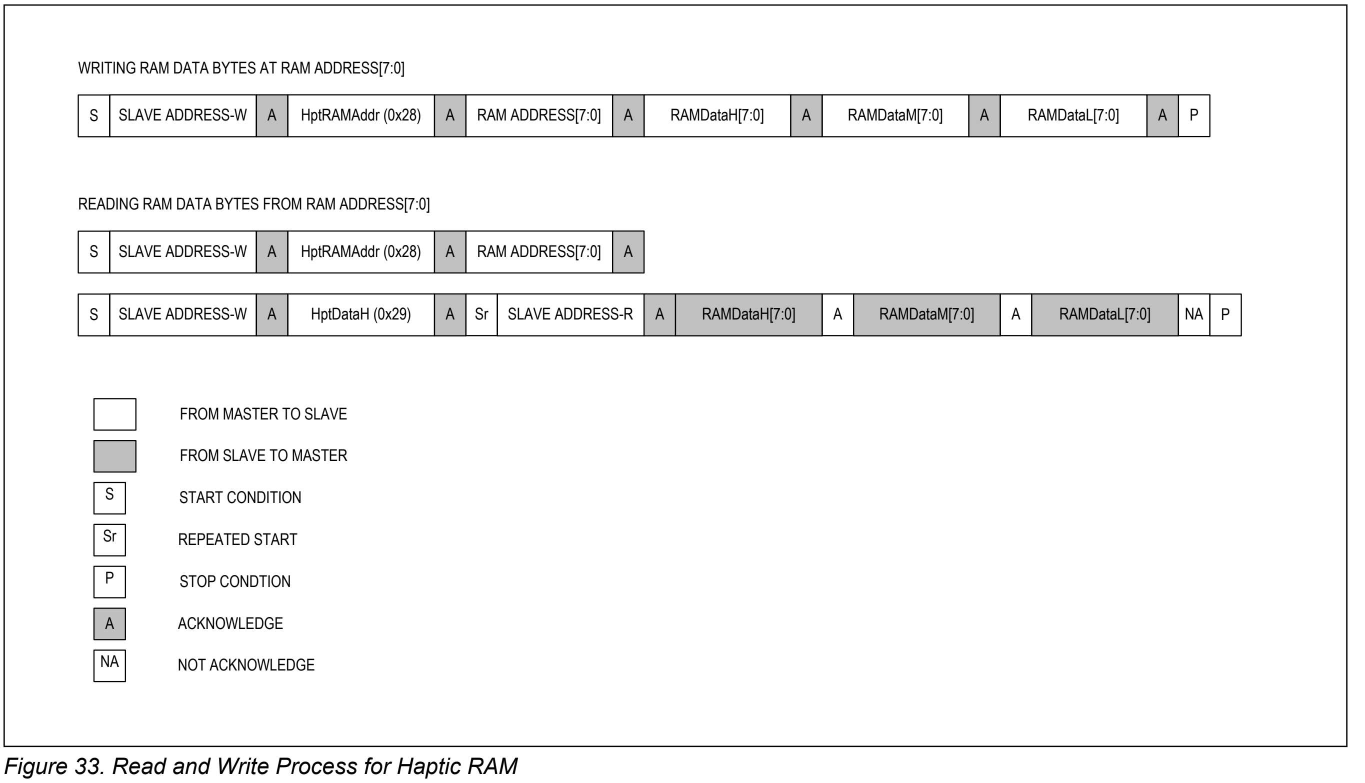


Figure 33. Read and Write Process for Haptic RAM

Table 7. RAMHP Pattern Storage Format

ADDRESS	0x40-0x43							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
HptRAMAdd	HptRAMAdd[7:0]							

Table 7. RAMHP Pattern Storage Format (continued)

<table>
<tr><td>HptRAMDataH</td><td colspan="2">nLSx[1:0]</td><td colspan="1">AmpSign</td><td colspan="5">Amp[6:2]</td></tr>
<tr><td>HptRAMDataM</td><td colspan="2">Amp[1:0]</td><td colspan="5">Dur[4:0]</td><td colspan="1">Wait[4]</td></tr>
<tr><td>HptRAMDataL</td><td colspan="4">Wait[3:0]</td><td colspan="4">RPTx[3:0]</td></tr>
<tr><td>HptRAMAdd[7:0]</td><td colspan="8">The RAM address in which the pattern sample is stored</td></tr>
<tr><td>nLSx[1:0]</td><td colspan="8">Sets the behavior of a sample in the pattern.
00 = Current sample is the last sample in the pattern
01 = Current sample is not the last sample in the pattern
10 = Interpolate current sample with next sample
11 = Current sample is the last sample in the pattern. Repeat the entire pattern RPTx[3:0] times</td></tr>
<tr><td>AmpSign[1:0]</td><td colspan="8">Sign of haptic amplitude in current sample
0 = Positive
1 = Negative
Patterns must always use the convention that driving begins with positive (0) amplitude and braking is done with negative (1) amplitude.</td></tr>
<tr><td>Amp[6:2]</td><td colspan="8">Sets the amplitude of pattern sample x as a 7-bit percentage of V_{FS} and a 1-bit direction (see Vfs[7:0]).</td></tr>
<tr><td>Dur[4:0]</td><td colspan="8">Sets the duration of time the driver outputs the amplitude of the current sample in increments of 5ms
00000 = 0ms
00001 = 5ms
…
11110 = 150ms
11111 = 155ms</td></tr>
<tr><td>Wait[4:0]</td><td colspan="8">Sets the duration of time the driver waits at zero amplitude before the next sample in increments of 5ms
00000 = 0ms
00001 = 5ms
...
11110 = 150ms
11111 = 155ms</td></tr>
<tr><td>RPTx[3:0]</td><td colspan="8">Sets the number of times to repeat the sample before moving to the next sample in the pattern. If nLSx[1:0] = 11, this sets the number of times to repeat the whole pattern.
0000 = Repeat 0 times. If nLSx = 00, automatic braking is performed on this sample with a maximum braking time equal to Wait[4:0].
0001 = Repeat 1 time
…
1110 = Repeat 14 times
1111 = Repeat 15 times</td></tr>
</table>

nLS0[1:0]	A[7:0]	D[4:0]	W[4:0]	RPT[3:0]

nLS_{PREV}	A_{PREV}	D_{PREV}	W_{PREV}	RPT_{PREV}
01	A0	00010	00001	0001
01	A1	00011	00000	0010
10	A2	00011	00000	DC
10	A3	00011	00000	DC
11	A4	DC	00010	0010

← END OF PREVIOUS PATTERN

DC = DON'T CARE

Figure 34. Sample Pattern Stored in RAM

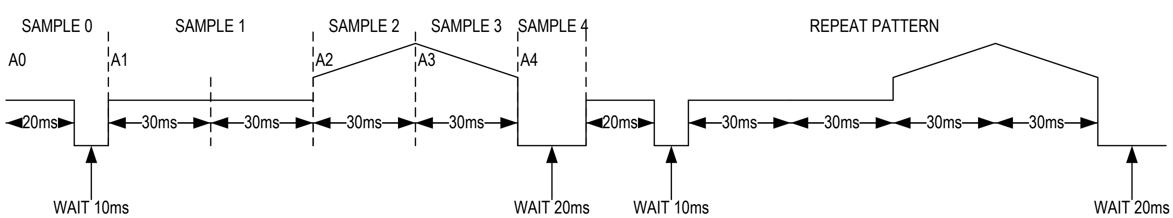


Figure 35. Diagram of Haptic Driver Output for Sample Pattern Stored Pattern

Fuel Gauge

The MAX20360 integrates ModelGauge m5 EZ with high-side current sensing. For more details about the ModelGauge m5 algorithm, a link to the ModelGauge m5 EZ User Guide/software implementation guide, etc., refer to the Design Resources tab at the *MAX17260 product page*, and see the Register Map in the *MAX17620 data sheet*.

MAX20361 Harvester Interaction

The MAX20360 implements a few features that allow it to seamlessly interact with the MAX20361 solar-energy harvester chip. Registers ThmCfg2, HrvCfg0, and HrvCfg1 (see bits: *ThmCfg2*, *HrvCfg0*, *HrvCfg1*) offer some settings for how the harvester-PMIC interaction takes place. Thresholds set on the PMIC for battery full-charge voltage and a restart threshold (see bits: *HrvBatReg*, *HrvBatReChg*) set the conditions for the behavior of the PMIC described in per the HrvBatSys register setting (see bit: *HrvBatSys*). Interactions between the charger and harvester are intended to be seamless and system intervention should not be necessary.

Harvester Thermistor Monitoring

The MAX20360 features harvester temperature thresholds that are distinct from those of the battery charger for hot and cold regions. These thresholds are more relaxed offering a wider temperature range over which the harvester is permitted to charge. According to the device specific setting (see JEITASet in Table 8) the hot threshold can be set to either 14.51% (JEITASet = 0) or 23.53% (JEITASet = 1) while the cold threshold is fixed at 81.64% for both. For additional flexibility, register HrvCfg1 (see register: *HrvCfg1*) also allows behavior in the various charging temperature regions to be defined.

Register Map

Haptic Driver and ADC Registers - SlaveID: 0xA0/0xA1

ADDRESS	NAME	MSB							LSB
ADC and Haptic Status/Interrupts									
0x00	HptStatus0[7:0]	HptHDINDis	HptDRPOCPLow	HptDRNOCPLow	HptDRPOCPHigh	HptDRNOCPHigh	HptThm	HptClkOn	HptFrqLock
0x01	HptStatus1[7:0]	–	–	–	–	–	–	–	HptFlt
0x02	HptStatus2[7:0]	–	–	–	–	–	–	ADCBusy	–
0x03	HptInt0[7:0]	HptHDINDisInt	HptDRPOCPLowInt	HptDRNOCPLowInt	HptDRPOCPHighInt	HptDRNOCPHighInt	HptThmInt	HptClkOnInt	HptFrqLockInt
0x04	HptInt1[7:0]	–	–	–	–	HptAutoTuneDoneInt	HptTmoInt	HptHDINUVLOInt	HptFltInt
0x05	HptInt2[7:0]	–	–	–	–	–	–	ADCBusyInt	ADCEOCInt
0x06	HptIntMask0[7:0]	HptHDINDisIntM	HptDRPOCPLowIntM	HptDRNOCPLowIntM	HptDRPOCPHighIntM	HptDRNOCPHighIntM	HptThmIntM	HptClkOnIntM	HptFrqLockIntM
0x07	HptIntMask1[7:0]	–	–	–	–	HptAutoTuneDoneIntM	HptTmoIntM	HptHDINUVLOIntM	HptFltIntM
0x08	HptIntMask2[7:0]	–	–	–	–	–	–	ADCBusyIntM	ADCEOCIntM
Haptic Control									
0x09	HptControl[7:0]	HptExtTrig	HptRamEn	HptDrvClkEn	HptDrvMode[4:0]				
0x0A	HptRTI2CPat[7:0]	HptRTI2CPat[7:0]							
0x0B	HptRAMPatAdd[7:0]	HptRAMPatAdd[7:0]							
0x0C	HptProt[7:0]	–	–	–	–	–	HptOffImp	HptThmProtDis	HptOCProtDis
0x0D	HptUnlock[7:0]	–	–	–	–	–	–	–	HptFltUnlock
Haptic Configuration									
0x11	HPTCfg0[7:0]	–	AutoBrkPeakMeas	AutoBrkCmpSatStop	AutoBrkDis	EmfEn	HptSel	AlcEn	ZccHysEn
0x12	HPTCfg1[7:0]	Vfs[7:0]							
0x13	HPTCfg2[7:0]	HDINDisTh[7:0]							
0x14	HPTCfg3[7:0]	–	EmfSkipTh[6:0]						
0x15	HPTCfg4[7:0]	IniGssResDis	–	–	IniDly[4:0]				
0x16	HPTCfg5[7:0]	–	–	–	WidWdw[4:0]				
0x17	HPTCfg6[7:0]	NarWdw[3:0]				–	EmfSkipCyc[2:0]		

ADDRESS	NAME	MSB							LSB
0x18	HPTCfg7[7:0]	–	–	BlankWdw[5:0]					
0x19	HPTCfg8[7:0]	–	–	–	BrkCyc[4:0]				
0x1A	HPTCfg9[7:0]	AutoBrkMeasWdw[3:0]				AutoBrkMeasTh[1:0]		AutoBrkMeasEnd[1:0]	
0x1B	HPTCfgA[7:0]	–	BrkLpGain[1:0]		–	BrkWdw[3:0]			
0x1C	HPTCfgB[7:0]	ZccSlowEn	FltrCntrEn	–	DrvTmo[4:0]				
0x1D	HPTCfgC[7:0]	IniGss[7:0][7:0]							
0x1E	HPTCfgD[7:0]	–	–	–	–	IniGss[11:8][3:0]			
0x1F	HPTCfgE[7:0]	–	–	NarCntLck[5:0]					
0x20	HPTCfgF[7:0]	–	NarLpGain[2:0]			–	WidLpGain[2:0]		
Haptic Autotune									
0x22	HptAutoTune[7:0]	–	–	–	–	–	–	AutoTuneGood	AutoTuneRun
0x23	BEMFPeriod0[7:0]	BEMFPeriod[7:0][7:0]							
0x24	BEMFPeriod1[7:0]	–	–	–	–	BEMFPeriod[11:8][3:0]			
Haptic Patterns									
0x30	HptETRGOdAmp[7:0]	ETRGOdAmp[7:0]							
0x31	HptETRGOdDur[7:0]	ETRGOdDur[7:0]							
0x32	HptETRGActAmp[7:0]	ETRGActAmp[7:0]							
0x33	HptETRGActDur[7:0]	ETRGActDur[7:0]							
0x34	HptETRGBrkAmp[7:0]	ETRGBrkAmp[7:0]							
0x35	HptETRGBrkDur[7:0]	ETRGBrkDur[7:0]							
RAM Interface									
0x40	HptRAMAdd[7:0]	HptRAMAdd[7:0]							
0x41	HptRAMDataH[7:0]	HptRAMDataH[7:0]							
0x42	HptRAMDataM[7:0]	HptRAMDataM[7:0]							
0x43	HptRAMDataL[7:0]	HptRAMDataL[7:0]							
ADC/MON Interface									
0x50	ADCEn[7:0]	–	–	–	–	–	–	–	ADCConvLaunch
0x51	ADCCfg[7:0]	–	–	ADCAvgSiz[2:0]			ADCSel[2:0]		
0x53	ADCDatAvg[7:0]	ADCAvg[7:0]							
0x54	ADCDatMin[7:0]	ADCMin[7:0]							
0x55	ADCDatMax[7:0]	ADCMax[7:0]							

Register Details

HptStatus0 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	HptHDINDis	HptDRPOCPLow	HptDRNOCPLow	HptDRPOCPHigh	HptDRNOCPHigh	HptThm	HptClkOn	HptFrqLock
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HptHDINDis	7	Status of the haptic driver HDIN voltage disable threshold.	0: V_{HDIN} greater than HDINDisTh[7:0] threshold. 1: Fault condition. Haptic driver locked and disabled due to V_{HDIN} falling below the HDINDisTh[7:0] threshold.
HptDRPOCPLow	6	Status of the haptic driver overcurrent protection on the DRP low-side switch.	0: No overcurrent detected on the DRP low-side switch. 1: Fault condition. Haptic driver locked and disabled due to current on the DRP low-side switch rising above thr I_{HD_OCP} threshold.
HptDRNOCPLow	5	Status of the haptic driver overcurrent protection on the DRN low-side switch.	0: No overcurrent detected on the DRN low-side switch. 1: Fault condition. Haptic driver locked and disabled due to current on the DRN low-side switch rising above the I_{HD_OCP} threshold.
HptDRPOCPHigh	4	Status of the haptic driver overcurrent protection on the DRP high-side switch.	0: No overcurrent detected on the DRP high-side switch. 1: Fault condition, haptic driver locked and disabled due to the current on the DRP high-side switch rising above the I_{HD_OCP} threshold.
HptDRNOCPHigh	3	Status of the haptic driver overcurrent protection on the DRN high-side switch.	0: No overcurrent detected on the DRN high-side switch. 1: Fault condition. Haptic driver locked and disabled due to current on the DRN high-side switch rising above the I_{HD_OCP} threshold.
HptThm	2	Status of the haptic driver thermal protection.	0: No overtemperature condition detected. 1: Fault condition. Haptic driver locked and disabled due to the die temperature rising above the T_{HD_SHDN} threshold.
HptClkOn	1	Status of the haptic driver clock.	0: Haptic driver clock disabled 1: Haptic driver clock enabled
HptFrqLock	0	Status of the haptic driver BEMF resonant frequency locking.	0: BEMF resonant frequency not locked 1: BEMF resonant frequency locked

HptStatus1 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	HptFlt
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HptFlt	0	Status of the haptic driver fault condition.	0: No haptic driver fault condition detected 1: Haptic driver locked and disabled due to one or more fault conditions detected

HptStatus2 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	ADCBusy	–
Access Type	–	–	–	–	–	–	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
ADCBusy	1	Status of ADC operation.	0: ADC disabled 1: ADC enabled and conversion running

HptInt0 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	HptHDINDisInt	HptDRPOCPLowInt	HptDRNOCPLowInt	HptDRPOCPHighInt	HptDRNOCPHighInt	HptThmInt	HptClkOnInt	HptFrqLockInt
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
HptHDINDisInt	7	Change in HptHDINDis caused an interrupt.
HptDRPOCPLowInt	6	Change in HptDRPOCPLow caused an interrupt.
HptDRNOCPLowInt	5	Change in HptDRNOCPLow caused an interrupt.
HptDRPOCPHighInt	4	Change in HptDRPOCPHigh caused an interrupt.
HptDRNOCPHighInt	3	Change in HptDRNOCPHigh caused an interrupt.
HptThmInt	2	Change in HptThm caused an interrupt.
HptClkOnInt	1	Change in HptClkOn caused an interrupt.
HptFrqLockInt	0	Change in HptFrqLock caused an interrupt.

HptInt1 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HptAutoTuneDoneInt	HptTmoInt	HptHDINUVLOInt	HptFltInt
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HptAutoTuneDoneInt	3	Haptic driver auto-tune procedure completion interrupt.	Set to 1 when haptic auto tune is complete.
HptTmoInt	2	Haptic driver vibration timeout interrupt.	0: Haptic driver vibration timeout not expired. 1: Fault condition. Haptic driver locked and disabled due to vibration timeout being expired.
HptHDINUVLOInt	1	Haptic driver HDIN UVLO interrupt.	0: $V_{HDIN} > V_{HDIN\_UVLO}$. 1: Fault condition. Haptic driver locked and disabled due to $V_{HDIN} < V_{HDIN\_UVLO}$.
HptFltInt	0	Change in HptFlt caused an interrupt.	Set to 1 when there is change in the HptFlt bit.

HptInt2 (0x05)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	ADCBusyInt	ADCEOCInt
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
ADCBusyInt	1	Change in ADCBusy caused an interrupt.
ADCEOCInt	0	ADC end of conversion interrupt.

HptIntMask0 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	HptHDINDisIntM	HptDRPOCPLowIntM	HptDRNOCPLowIntM	HptDRPOCPHighIntM	HptDRNOCPHighIntM	HptThmIntM	HptClkOnIntM	HptFrqLockIntM
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HptHDINDisIntM	7	HptHDINDisIntM masks the HptHDINDisInt interrupt in the HptInt0 register (0x03).	0: Masked 1: Not masked
HptDRPOCPLowIntM	6	HptDRPOCPLowIntM masks the HptDRPOCPLowInt interrupt in the HptInt0 register (0x03).	0: Masked 1: Not masked
HptDRNOCPLowIntM	5	HptDRNOCPLowIntM masks the HptDRNOCPLowInt interrupt in the HptInt0 register (0x03).	0: Masked 1: Not masked
HptDRPOCPHighIntM	4	HptDRPOCPHighIntM masks the HptDRPOCPHighInt interrupt in the HptInt0 register (0x03).	0: Masked 1: Not masked
HptDRNOCPHighIntM	3	HptDRNOCPHighIntM masks the HptDRNOCPHighInt interrupt in the HptInt0 register (0x03).	0: Masked 1: Not masked
HptThmIntM	2	HptThmIntM masks the HptThmInt interrupt in the HptInt0 register (0x03).	0: Masked 1: Not masked
HptClkOnIntM	1	HptClkOnIntM masks the HptClkOnInt interrupt in the HptInt0 register (0x03).	0: Masked 1: Not masked
HptFrqLockIntM	0	HptFrqLockIntM masks the HptFrqLockInt interrupt in the HptInt0 register (0x03).	0: Masked 1: Not masked

HptIntMask1 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HptAutoTuneDoneIntM	HptTmoIntM	HptHDINUVLOIntM	HptFltIntM
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HptAutoTuneDoneIntM	3	HptAutoTuneDoneIntM masks the HptAutoTuneDoneInt interrupt in the HptInt1 register (0x04).	0: Masked 1: Not masked

BITFIELD	BITS	DESCRIPTION	DECODE
HptTmoIntM	2	HptTmoIntM masks the HptTmoInt interrupt in the HptInt1 register (0x04).	0: Masked 1: Not masked
HptHDINUVLOIntM	1	HptHDINUVLOIntM masks the HptHDINUVLOInt interrupt in the HptInt1 register (0x04).	0: Masked 1: Not masked
HptFltIntM	0	HptFltIntM masks the HptFltInt interrupt in the HptInt1 register (0x04).	0: Masked 1: Not masked

HptIntMask2 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	ADCBusyIntM	ADCEOCIntM
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ADCBusyIntM	1	ADCBusyIntM masks the ADCBusyInt interrupt in the HptInt2 register (0x05).	0: Masked 1: Not masked
ADCEOCIntM	0	ADCEOCIntM masks the ADCEOCInt interrupt in the HptInt2 register (0x05).	0: Masked 1: Not masked

HptControl (0x09)

BIT	7	6	5	4	3	2	1	0
Field	HptExtTrig	HptRamEn	HptDrvClkEn	HptDrvMode[4:0]				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
HptExtTrig	7	Haptic driver external trigger for ETRGI and RAMHPI driver mode (HptDrvMod[4:0] = "01100" and HptDrvMod[4:0] = "10010," respectively)	0: No vibration triggered 1: Vibration triggered
HptRamEn	6	Haptic driver RAM block enable	0: RAM disabled 1: RAM enabled
HptDrvClkEn	5	Haptic driver clock enable. In all interface modes, HptDrvClkEn must be set to 1 at the same time or before providing the desired mode in HptDrvMod[4:0]. The HptDrvClkEn bit must remain set to 1 during the vibration. Once vibration finishes, HptDrvMod[4:0] must be set to “00000” before the haptic driver can be disabled through HptDrvClkEn = 0 for power savings	0: Haptic driver clock disabled 1: Haptic driver clock enabled

BITFIELD	BITS	DESCRIPTION	DECODE
HptDrvMode	4:0	Haptic driver interface mode selection.	00000: Disable haptic driver. 00001: Enable PPWM0 mode and provide amplitude based on PWM duty cycle on MPC0 00010: Enable PPWM1 mode and provide amplitude based on PWM duty cycle on MPC1 00011: Enable PPWM2 mode and provide amplitude based on PWM duty cycle on MPC2 00100: Enable PPWM3 mode and provide amplitude based on PWM duty cycle on MPC3 00101: Enable PPWM4 mode and provide amplitude based on PWM duty cycle on MPC4 00110: Enable RTI2C mode and provide current output amplitude based on the contents of HptRTI2CPat(0x0A) 00111: Enable ETRG0 mode. Provide a pulse on MPC0 to start vibration (see the External Triggered Stored Pattern (ETRG) section for details). 01000: Enable ETRG1 mode. Provide a pulse on MPC1 to start vibration (see the External Triggered Stored Pattern (ETRG) section for details). 01001: Enable ETRG2 mode. Provide a pulse on MPC2 to start vibration (see the External Triggered Stored Pattern (ETRG) section for details). 01010: Enable ETRG3 mode. Provide a pulse on MPC3 to start vibration (see the External Triggered Stored Pattern (ETRG) section for details). 01011: Enable ETRG4 mode. Provide a pulse on MPC4 to start vibration (see the External Triggered Stored Pattern (ETRG) section for details). 01100: Enable ETRGI mode using I^2C. Set HptExtTrg(0x09[7]) bit to start vibration (see the External Triggered Stored Pattern (ETRG) section for details). 01101: Enable RAMHP0 mode. Provide a pulse on MPC0 to start vibration (see the RAM Stored Haptic Pattern (RAMHP) section for details). 01110: Enable RAMHP1 mode. Provide a pulse on MPC1 to start vibration (see the RAM Stored Haptic Pattern (RAMHP) section for details). 01111: Enable RAMHP2 mode. Provide a pulse on MPC2 to start vibration (see the RAM Stored Haptic Pattern (RAMHP) section for details). 10000: Enable RAMHP3 mode. Provide a pulse on MPC3 to start vibration (see the RAM Stored Haptic Pattern (RAMHP) section for details). 10001: Enable RAMHP4 mode. Provide a pulse on MPC4 to start vibration (see the RAM Stored Haptic Pattern (RAMHP) section for details). 10010: Enable RAMHPI mode using I^2C. Set HptExtTrg(0x09[7]) bit to start vibration (see the RAM Stored Haptic Pattern (RAMHP) section for details). >10010: Reserved

HptRTI2CPat (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	HptRTI2CPat[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HptRTI2CPat	7:0	Haptic driver programmed output amplitude as a percentage of V_{FS} in RTI2C mode (HptDrvMod = "00110"). LSB = 0.78%V_{FS}. Note that the MSB represents the sign of the amplitude to be driven. Patterns must always begin with driving in the positive direction (0 as the MSB).

HptRAMPatAdd (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	HptRAMPatAdd[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HptRAMPatAdd	7:0	Address of first sample in haptic driver vibration pattern to be run in RAMHP_ mode (HptDrvMod = "01101," "01110," "01111," "10000," "10001," "10010").

HptProt (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	HptOffImp	HptThmProt Dis	HptOCProt Dis
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HptOffImp	2	Haptic driver output off-state impedance.	0: When haptic driver is disabled, outputs are strongly shorted to GND through low-side switches 1: When haptic driver is disabled, outputs are shorted to GND with 15kΩ pull-down
HptThmProt Dis	1	Haptic driver thermal protection disable. If HptThmProtDis = 0 and the haptic driver is locked and disabled due to an overtemperature condition, HptThmInt interrupt is issued and HptFlt is set to 1. Set HptFltUnlock = 1 to allow a restart of the haptic driver.	0: Thermal protection enabled, haptic driver shuts down if die temperature rises above T_{HD_SHDN} threshold 1: Thermal protection disabled
HptOCProtDis	0	Haptic driver overcurrent protection disable. If HptOCProtDis = 0 and the haptic driver is locked and disabled due to an overcurrent condition, HptDRPOCPLowInt and/or HptDRNOCPLowInt and/or HptDRPOCPHighInt and/or HptDRNOCPHighInt interrupt is issued and HptFlt is set to 1. Set HptFltUnlock = 1 to allow a restart of the haptic driver.	0: Overcurrent protection enabled. Haptic driver shuts down if current through any of DRP/DRN high/low-side switches exceeds the I_{HD_OCP} threshold 1: Overcurrent protection disabled

HptUnlock (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	HptFltUnlock
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
HptFltUnlock	0	Haptic driver unlock control. When a fault condition causes the haptic driver to be locked and disabled, HptFlt is set to 1 and it can only be cleared by manually writing HptFltUnlock to 1. After the unlock, HptFltUnlock also goes to 0 automatically.

HPTCfg0 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	–	AutoBrkPeakMeas	AutoBrkCmpSatStop	AutoBrkDis	EmfEn	HptSel	AlcEn	ZccHysEn
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AutoBrkPeakMeas	6	Haptic driver BEMF amplitude detection sample points. Determines if two or four BEMF sample points are used during automatic braking.	0: Four sample points are used to measure the BEMF amplitude 1: Two sample points are used to measure the BEMF amplitude
AutoBrkCmpSatStop	5	Haptic driver BEMF zero crossing comparator counter saturation. If enabled, the automatic braking function exits when the counter on the zero crossing comparator is saturated during a braking window within one of the BrkCyc[4:0] half periods.	0: Do not exit braking when the zero crossing comparator counter is saturated 1: Exit braking when the zero crossing comparator counter is saturated
AutoBrkDis	4	Haptic driver automatic braking disable.	0: Automatic braking enabled 1: Automatic braking disabled
EmfEn	3	Haptic driver BEMF resonance detection control.	0: Disabled 1: Enabled
HptSel	2	Haptic driver mode select.	0: ERM mode 1: LRA mode
AlcEn	1	Haptic driver automatic level compensation (ALC) control.	0: Disabled 1: Enabled
ZccHysEn	0	Haptic driver BEMF zero crossing comparator hysteresis control.	0: Disabled 1: Enabled (6mV typ)

HPTCfg1 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	Vfs[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Vfs	7:0	Haptic drive full-scale voltage (V_{FS}). Stores the voltage V_{FS} to which the desired percentage output amplitude is referred. The actual V_{FS} is the minimum between the value programmed on Vfs[7:0] and the current V_{HDIN} value. LSB = 5.5V/255 = 21.57mV.

HPTCfg2 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	HDINDisTh[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HDINDisTh	7:0	Haptic driver HDIN voltage disable threshold. If V_{HDIN} falls below this threshold, the haptic driver is locked and disabled, HptHDINDisInt interrupt is issued and HptFlt is set to 1. Set HptFltUnlock = 1 to allow a restart of the haptic driver. LSB = 5.5V/255 = 21.57mV.

HPTCfg3 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	–	EmfSkipTh[6:0]						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
EmfSkipTh	6:0	Haptic driver BEMF detection skip threshold. If the absolute (lower 7 bits) programmed output amplitude as a percentage of V_{FS} is lower than EmfSkipTh, BEMF detection is skipped as the returned BEMF voltage would be too small to be reliably detected. LSB = 0.78%V_{FS}.

HPTCfg4 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	IniGssResDis	–	–	IniDly[4:0]				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
IniGssResDis	7	Haptic driver initial guess restore disable.	0: Haptic driver uses IniGss[11:0] as the driving frequency after the end of BrkCyc[4:0] sinewave half periods 1: Haptic driver does not use IniGss[11:0] as the driving frequency after the end of BrkCyc[4:0] sinewave half periods

BITFIELD	BITS	DESCRIPTION	DECODE
IniDly	4:0	Haptic driver number of sinewave half periods to be skipped before (re)starting BEMF measurement after: 1) start of vibration pattern 2) change of output polarity (e.g., braking) 3) programmed percentage output amplitude (with respect to V_{FS}) becoming again higher than EmfSkipTh[6:0] after having previously gone below it	

HPTCfg5 (0x16)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	WidWdw[4:0]				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
WidWdw	4:0	Haptic driver wide window duration for BEMF zero-crossing detection. LSB = 1/32nd of currently imposed sinewave period.

HPTCfg6 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	NarWdw[3:0]				–	EmfSkipCyc[2:0]		
Access Type	Write, Read				–	Write, Read		

BITFIELD	BITS	DESCRIPTION
NarWdw	7:4	Haptic driver narrow window duration for BEMF zero-crossing detection. LSB = 1/32nd of currently imposed sinewave period.
EmfSkipCyc	2:0	Haptic driver number of consecutive sinewave half periods during which BEMF detection is skipped after a BEMF detection completes.

HPTCfg7 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BlankWdw[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BlankWdw	5:0	Haptic driver zero-crossing comparator blanking time applied after entering or prior to exiting the wide, narrow, and braking windows. The blanking window duration cannot exceed 1/64th of the current sinewave period unless AutoBrkPeakMeas = 1 and the driver is in the automatic braking state. LSB = 128/25.6MHz.

HPTCfg8 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BrkCyc[4:0]				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
BrkCyc	4:0	Haptic driver number of consecutive sinewave half periods during which active braking is applied after a change in driving polarity. During these half periods, the gain used becomes BrkLpGain[1:0], the window duration becomes BrkWdw[4:0], and the effects of IniDly[4:0], EmfSkipCyc[2:0], and NarCntLck[5:0] are masked.

HPTCfg9 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	AutoBrkMeasWdw[3:0]				AutoBrkMeasTh[1:0]		AutoBrkMeasEnd[1:0]	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
AutoBrkMeasWdw	7:4	Haptic driver BEMF amplitude detection window duration during automatic braking. LSB = 128/25.6MHz.	
AutoBrkMeasTh	3:2	Haptic driver BEMF absolute amplitude detection threshold during automatic braking.	00: 2.5mV 01: 5.0mV 10: 7.5mV 11: 10.0mV
AutoBrkMeasEnd	1:0	Haptic driver BEMF amplitude detection end counter during automatic braking. Sets the number of consecutive BEMF amplitude detections in which the absolute amplitude of the BEMF must be less than AutoBrkMeasTh[1:0] for more than half of AutoBrkMeasWdw[3:0] in order to stop automatic braking.	00: 1 01: 2 10: 3 11: 4

HPTCfgA (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	–	BrkLpGain[1:0]		–	BrkWdw[3:0]			
Access Type	–	Write, Read		–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
BrkLpGain	6:5	Haptic driver braking window gain. Sets gain by which the phase delay found by the zero-crossing comparator is multiplied to calculate the shift for the new sinewave half period with respect to the previously imposed sinewave. This value is used when the braking window is active.	00: 1 01: 1/2 10: 1/4 11: 1/8
BrkWdw	3:0	Haptic driver braking window duration for BEMF zero-crossing detection. LSB = 1/32nd of currently imposed sinewave period.	

HPTCfgB (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	ZccSlowEn	FltrCntrEn	–	DrvTmo[4:0]				
Access Type	Write, Read	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ZccSlowEn	7	Haptic driver zero-crossing comparator slow-down enable.	0: Zero-crossing comparator operates in normal mode 1: Slows down the zero-crossing comparator by 2X for stronger antialiasing filtering
FltrCntrEn	6	Haptic driver zero-crossing event capturing filter enable.	0: Zero-crossing measured using single comparator/transition 1: Zero-crossing measured using an up/down counter that samples (at 25.6MHz) the output of the comparator for the whole duration of the enabled window (wide, narrow, or braking). The counter starts at zero (mid-code) and ends at a positive or negative code depending on whether the average zero-crossing event occurs before or after than the expected time. The closer the zero-crossing is on average to the expected time, the closer to zero code returned at the end of the window is. Phase error (in 25.6MHz period units) can be calculated by dividing the resulting code at the end of the window by 2. The usage of the up/down counter enables filtering/noise rejection that could otherwise cause a systematic shift in the phase error detected.
DrvTmo	4:0	Haptic driver vibration timeout. If vibration timeout is reached, the haptic driver is locked and disabled, HptTmoInt interrupt is issued and HptFlt is set to 1. Set HptFltUnlock = 1 to allow a restart of the haptic driver. LSB = 1s. Timeout is disabled if DrvTmo[4:0] = "00000."	

HPTCfgC (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	IniGss[7:0][7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
IniGss[7:0]	7:0	Haptic driver initial guess frequency. Initial estimate for BEMF frequency = ((25.6MHz/64) / IniGss[11:0]).

HPTCfgD (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	IniGss[11:8][3:0]			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
IniGss[11:8]	3:0	Haptic driver initial guess frequency. Initial estimate for BEMF frequency = ((25.6MHz/64) / IniGss[11:0]).

HPTCfgE (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	NarCntLck[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
NarCntLck	5:0	Haptic driver number of consecutive sinewave half periods where the BEMF is detected and where the phase delay must fall within the narrow window before detection window is reduced from wide to narrow.

HPTCfgF (0x20)

BIT	7	6	5	4	3	2	1	0
Field	–	NarLpGain[2:0]			–	WidLpGain[2:0]		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
NarLpGain	6:4	Haptic driver narrow window gain. Sets gain by which the phase delay found by the zero-crossing comparator is multiplied to calculate the shift for the new sinewave half period with respect to the previously imposed sinewave. This value is used when the narrow window is active.	000: 1 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64 111: 1/128
WidLpGain	2:0	Haptic driver wide window gain. Sets gain by which the phase delay found by the zero-crossing comparator is multiplied to calculate the shift for the new sinewave half period with respect to the previously imposed sinewave. This value is used when the wide window is active.	000: 1 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64 111: 1/128

HptAutoTune (0x22)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AutoTuneGood	AutoTuneRun
Access Type	–	–	–	–	–	–	Read Only	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AutoTuneGood	1	Haptic driver auto-tune procedure result.	0: BEMF resonant frequency locking was not achieved with the auto-tune procedure 1: BEMF resonant frequency locking was achieved with the auto-tune procedure

BITFIELD	BITS	DESCRIPTION	DECODE
AutoTuneRun	0	Haptic driver auto-tune command. Set AutoTuneRun to 1 to launch the auto-tune procedure. AutoTuneRun is automatically cleared to 0 once auto-tune procedure is complete.	

BEMFPeriod0 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	BEMFPeriod[7:0][7:0]							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BEMFPeriod[7:0]	7:0	Haptic driver resonant frequency resolved by autotune function = ((25.6MHz / 64) / BEMFPeriod[11:0]).

BEMFPeriod1 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BEMFPeriod[11:8][3:0]			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
BEMFPeriod[11:8]	3:0	Haptic driver resonant frequency resolved by autotune function = ((25.6MHz / 64) / BEMFPeriod[11:0]).

HptETRGOdAmp (0x30)

BIT	7	6	5	4	3	2	1	0
Field	ETRGOdAmp[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ETRGOdAmp	7:0	Haptic driver programmed output amplitude of the overdrive period as a percentage of V_{FS} in ETRG mode. LSB = 0.78%V_{FS}. Note that the MSB represents the sign of the amplitude to be driven and must always be set to 0.

HptETRGOdDur (0x31)

BIT	7	6	5	4	3	2	1	0
Field	ETRGOdDur[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ETRGOdDur	7:0	Haptic driver duration of the overdrive period in ETRG mode. LSB = 5ms.

HptETRGActAmp (0x32)

BIT	7	6	5	4	3	2	1	0
Field	ETRGActAmp[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ETRGActAmp	7:0	Haptic driver programmed output amplitude of the normal drive period as a percentage of V_{FS} in ETRG mode. LSB = 0.78%V_{FS}. Note that the MSB represents the sign of the amplitude to be driven and must always be set to 0.

HptETRGActDur (0x33)

BIT	7	6	5	4	3	2	1	0
Field	ETRGActDur[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ETRGActDur	7:0	Haptic driver duration of the normal drive period in ETRG mode. LSB = 10ms.

HptETRGBrkAmp (0x34)

BIT	7	6	5	4	3	2	1	0
Field	ETRGBrkAmp[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ETRGBrkAmp	7:0	Haptic driver programmed output amplitude of the braking period is a percentage of V_{FS} in ETRG mode. LSB = 0.78%V_{FS}. Note that the MSB represents the sign of the amplitude to be driven and must always be set to 1.

HptETRGBrkDur (0x35)

BIT	7	6	5	4	3	2	1	0
Field	ETRGBrkDur[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ETRGBrkDur	7:0	Haptic driver duration of the braking period in ETRG mode is LSB = 5ms. If AutoBrkDis = 0, the automatic braking process is triggered with a maximum braking time of ETRGBrkDur[7:0]. If AutoBrkDis = 1, ETRGBrkDur[7:0] must be adjusted to achieve the desired optimal braking efficiency.

HptRAMAdd (0x40)

BIT	7	6	5	4	3	2	1	0
Field	HptRAMAdd[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HptRAMAdd	7:0	Haptic driver RAM address. The pattern sample is stored in these bits.

HptRAMDataH (0x41)

BIT	7	6	5	4	3	2	1	0
Field	HptRAMDataH[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HptRAMDataH	7:0	Bits 7-6: nLSx Bit 5: AmpSign Bits 4-0: Amp[6:2]	nLSx: Sets the behavior of a sample in the pattern. 00 = Current sample is the last sample in the pattern 01 = Current sample is not the last sample in the pattern 10 = Interpolate current sample with next sample 11 = Current sample is the last sample in the pattern. Repeat the entire pattern RPTx[3:0] times AmpSign: Sign of haptic amplitude in current sample 0 = Positive 1 = Negative Amp: Sets the amplitude of pattern sample x as a 7-bit percentage of V_{FS} and a 1-bit direction.

HptRAMDataM (0x42)

BIT	7	6	5	4	3	2	1	0
Field	HptRAMDataM[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HptRAMDataM	7:0	Bits 7-6: Amp[1:0] Bits 5-1: Dur[4:0] Bit 0: Wait[4]	Amp: Sets the amplitude of pattern sample x as a 7-bit percentage of V_{FS} and a 1-bit direction. Dur: Sets the duration of time the driver outputs the amplitude of the current sample in increments of 5ms 00000 = 0ms 00001 = 5ms ... 11110 = 150ms 11111 = 155ms Wait: Sets the duration of time the driver waits at zero amplitude before the next sample in increments of 5ms 00000 = 0ms 00001 = 5ms ... 11110 = 150ms 11111 = 155ms

HptRAMDataL (0x43)

BIT	7	6	5	4	3	2	1	0
Field	HptRAMDataL[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HptRAMData L	7:0	Bits 7-4: Wait[3:0] Bits 3-0: RPTx[3:0]	Wait: Sets the duration of time the driver waits at zero amplitude before the next sample in increments of 5ms 00000 = 0ms 00001 = 5ms ... 11110 = 150ms 11111 = 155ms RPTx: Sets the number of times to repeat the sample before moving to the next sample in the pattern. If nLSx[1:0] = 11, this sets the number of times to repeat the whole pattern. 0000 = Repeat 0 times. If nLSx = 00, automatic braking is performed on this sample with a maximum braking time equal to Wait[4:0]. 0001 = Repeat 1 time … 1110 = Repeat 14 times 1111 = Repeat 15 timesMAX20353Wearable

ADCEn (0x50)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ADCConvL aunch
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
ADCConvLaunch	0	ADC conversion launch command. Set ADCConvLaunch = 1 to launch an ADC conversion. ADCConvLaunch is automatically cleared to 0 once the conversion is complete.

ADCCfg (0x51)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ADCAvgSiz[2:0]			ADCSel[2:0]		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ADCAvgSiz	5:3	ADC averaging size. ADC performs $2^{ADCAvgSiz[2:0]}$ consecutive averaged measurements.	000: No averaging (1 measurement) 001: Average 2 measurements 010: Average 4 measurements 011: Average 8 measurements 100: Average 16 measurements 101: Average 32 measurements 110: Average 64 measurements 111: Average 128 measurements
ADCSel	2:0	ADC channel selection.	000: V_{HDIN} 001: V_{IVMON} (use IVMONRatioConfig[1:0] = "00") 010: Reserved 011: V_{CHGIN} 100: V_{CPOUT} 101: V_{BSTOUT} 110: Reserved 111: Reserved

ADCDatAvg (0x53)

BIT	7	6	5	4	3	2	1	0
Field	ADCAvg[7:0]							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ADCAvg	7:0	ADC conversion average value. Contains the average value of the $2^{ADCAvgSiz[2:0]}$ ADC measurements.

ADCDatMin (0x54)

BIT	7	6	5	4	3	2	1	0
Field	ADCMin[7:0]							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ADCMin	7:0	ADC conversion minimum value. Contains the minimum value among the $2^{ADCAvgSiz[2:0]}$ ADC measurements.

ADCDatMax (0x55)

BIT	7	6	5	4	3	2	1	0
Field	ADCMax[7:0]							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ADCMax	7:0	ADC conversion maximum value. Contains the maximum value among the $2^{ADCAvgSiz[2:0]}$ ADC measurements.

PMIC Registers - SlaveID: 0x50/0x51

ADDRESS	NAME	MSB							LSB
PMIC Interrupts and Status									
0x00	ChipID[7:0]	ChipRev[7:0]							
0x01	Status0[7:0]	–	–	ThmStat[2:0]			ChgStat[2:0]		
0x02	Status1[7:0]	–	–	ILim	UsbOVP	UsbOk	ChgJEITASD	ChgJEITAReg	ChgTmo
0x03	Status2[7:0]	ChgThmSD	–	ThmLDO_LSW	UVLOLDO2	UVLOLDO1	–	LSW1Tmo	LSW2Tmo
0x04	Status3[7:0]	BBstFault	HrvBatCmp	SysBatLim	ChgSysLim	ChgStep	ThmBk1	ThmBk2	ThmBk3
0x05	Status4[7:0]	BatGood	BatRegDone	BstFault	–	–	–	–	–
0x06	Int0[7:0]	ThmStatInt	ChgStatInt	ILimInt	UsbOVPInt	UsbOkInt	ChgJEITASDInt	ChgJEITARegInt	ChgTmoInt
0x07	Int1[7:0]	ChgThmSDInt	–	ThmLDO_LSWInt	UVLOLDO2Int	UVLOLDO1Int	–	LSW1TmoInt	LSW2TmoInt
0x08	Int2[7:0]	BBstFaultInt	HrvBatCmpInt	SysBatLimInt	ChgSysLimInt	ChgStepInt	ThmBk1Int	ThmBk2Int	ThmBk3Int
0x09	Int3[7:0]	BatGoodInt	BatRegDoneInt	BstFaultInt	–	I2cCrcFailInt	I2cTmoInt	HptStatInt	ADCStatInt
0x0A	IntMask0[7:0]	ThmStatIntM	ChgStatIntM	ILimIntM	UsbOVPIntM	UsbOkIntM	ChgJEITASDIntM	ChgJEITARegIntM	ChgTmoIntM
0x0B	IntMask1[7:0]	ChgThmSDIntM	–	ThmLDO_LSWIntM	UVLOLDO2IntM	UVLOLDO1IntM	–	LSW1TmoIntM	LSW2TmoIntM
0x0C	IntMask2[7:0]	BBstFaultIntM	HrvBatCmpIntM	SysBatLimIntM	ChgSysLimIntM	ChgStepIntM	ThmBk1IntM	ThmBk2IntM	ThmBk3IntM
0x0D	IntMask3[7:0]	BatGoodIntM	BatRegDoneIntM	BstFaultIntM	–	I2cCrcFailIntM	I2cTmoIntM	HptStatIntM	ADCStatIntM
Charger									
0x0F	ILimCntl[7:0]	SysMinVlt[2:0]			ILimBlank[1:0]		ILimCntl[2:0]		
0x10	ChgCntl0[7:0]	FrcPChg	ChgBatReChg[1:0]		ChgBatReg[3:0]				ChgEn
0x11	ChgCntl1[7:0]	BatPD	VPChg[2:0]			IPChg[1:0]		IChgDone[1:0]	
0x12	ChgTmr[7:0]	ChgAutoStop	ChgAutoReSta	MtChgTmr[1:0]		FChgTmr[1:0]		PChgTmr[1:0]	
0x13	StepChgCfg0[7:0]	–	ChgStepHys[2:0]			ChgStepRise[3:0]			
0x14	StepChgCfg1[7:0]	–	–	–	VSysUvlo[1:0]		ChgIStep[2:0]		
0x15	ThmCfg0[7:0]	–	ChgThmEn[1:0]		ChgCoolBatReg[1:0]		ChgCoolFChg[2:0]		
0x16	ThmCfg1[7:0]	–	–	–	ChgRoomBatReg[1:0]		ChgRoomIFChg[2:0]		
0x17	ThmCfg2[7:0]	HrvThmEn[1:0]		–	ChgWarmBatReg[1:0]		ChgWarmIFChg[2:0]		
0x18	HrvCfg0[7:0]	HrvBatSys[1:0]		HrvBatReChg[1:0]		HrvBatReg[3:0]			
0x19	HrvCfg1[7:0]	–	HrvThmDis	HrvWarmBatReg[1:0]		HrvRoomBatReg[1:0]		HrvCoolBatReg[1:0]	

ADDRESS	NAME	MSB							LSB
MON Mux									
0x1A	IVMONCfg[7:0]	–	IVMONRatioConfig[1:0]		IVMONOffHiZ	IVMONCntl[3:0]			
Buck1									
0x1B	Buck1Ena[7:0]	Buck1Seq[2:0]			–	–	–	Buck1En[1:0]	
0x1C	Buck1Cfg0[7:0]	Buck1IntegDis	Buck1PGOODEn	Buck1Fast	Buck1PsvDsc	Buck1ActDsc	Buck1LowEMI	Buck1FETScale	Buck1EnLXSns
0x1D	Buck1Cfg1[7:0]	–	–	Buck1MPC2Fast	Buck1FPWM	Buck1IAdptDis	–	–	–
0x1E	Buck1Iset[7:0]	Buck1ISetLookUpDis	–	–	–	Buck1ISet[3:0]			
0x1F	Buck1VSet[7:0]	–	–	Buck1VSet[5:0]					
0x20	Buck1Ctr[7:0]	Buck1MPC7	Buck1MPC6	Buck1MPC5	Buck1MPC4	Buck1MPC3	Buck1MPC2	Buck1MPC1	Buck1MPC0
0x21	Buck1DvsCfg0[7:0]	–	–	–	Buck1DVSCfg[4:0]				
0x22	Buck1DvsCfg1[7:0]	–	–	Buck1DVSVlt0[5:0]					
0x23	Buck1DvsCfg2[7:0]	–	–	Buck1DVSVlt1[5:0]					
0x24	Buck1DvsCfg3[7:0]	–	–	Buck1DVSVlt2[5:0]					
0x25	Buck1DvsCfg4[7:0]	–	–	Buck1DVSVlt3[5:0]					
0x26	Buck1DvsSpi[7:0]	–	–	Buck1SPIVlt[5:0]					
Buck2									
0x27	Buck2Ena[7:0]	Buck2Seq[2:0]			–	–	–	Buck2En[1:0]	
0x28	Buck2Cfg[7:0]	Buck2EnbINTGR	Buck2PGOODena	Buck2Fast	Buck2PsvDsc	Buck2ActDsc	Buck2LowEMI	Buck2FETScale	Buck2EnLxSns
0x29	Buck2Cfg1[7:0]	–	–	Buck2MPCFast	Buck2FPWM	Buck2IAdptDis	–	–	–
0x2A	Buck2Iset[7:0]	Buck2ISetLookUpDis	–	–	–	Buck2ISet[3:0]			
0x2B	Buck2VSet[7:0]	–	–	Buck2VSet[5:0]					
0x2C	Buck2Ctr[7:0]	Buck2MPC7	Buck2MPC6	Buck2MPC5	Buck2MPC4	Buck2MPC3	Buck2MPC2	Buck2MPC1	Buck2MPC0
0x2D	Buck2DvsCfg0[7:0]	–	–	–	Buck2DvsCfg[4:0]				
0x2E	Buck2DvsCfg1[7:0]	–	–	Buck2DvsVlt0[5:0]					
0x2F	Buck2DvsCfg2[7:0]	–	–	Buck2DvsVlt1[5:0]					
0x30	Buck2DvsCfg3[7:0]	–	–	Buck2DvsVlt2[5:0]					
0x31	Buck2DvsCfg4[7:0]	–	–	Buck2DvsVlt3[5:0]					
0x32	Buck2DvsSpi[7:0]	–	–	Buck2SPIVlt[5:0]					
Buck3									
0x34	Buck3Ena[7:0]	Buck3Seq[2:0]			–	–	–	Buck3En[1:0]	

ADDRESS	NAME	MSB							LSB
0x35	Buck3Cfg[7:0]	Buck3EnbINTGR	Buck3PGOODena	Buck3Fast	Buck3PsvDsc	Buck3ActDsc	Buck3LowEMI	Buck3FETScale	Buck3EnLxSns
0x36	Buck3Cfg1[7:0]	–	Buck3DisLDO	Buck3MPCFast	Buck3FPWM	Buck3IAdptDis	–	–	–
0x37	Buck3Iset[7:0]	Buck3ISetLookUpDis	–	–	–	Buck3ISet[3:0]			
0x38	Buck3VSet[7:0]	–	–	Buck3VSet[5:0]					
0x39	Buck3Ctr[7:0]	Buck3MPC7	Buck3MPC6	Buck3MPC5	Buck3MPC4	Buck3MPC3	Buck3MPC2	Buck3MPC1	Buck3MPC0
0x3A	Buck3DvsCfg0[7:0]	–	–	–	Buck3DvsCfg[4:0]				
0x3B	Buck3DvsCfg1[7:0]	–	–	Buck3DvsVlt0[5:0]					
0x3C	Buck3DvsCfg2[7:0]	–	–	Buck3DvsVlt1[5:0]					
0x3D	Buck3DvsCfg3[7:0]	–	–	Buck3DvsVlt2[5:0]					
0x3E	Buck3DvsCfg4[7:0]	–	–	Buck3DvsVlt3[5:0]					
0x3F	Buck3DvsSpi[7:0]	–	–	Buck3SPIVlt[5:0]					
Buck-Boost									
0x40	BBstEna[7:0]	BBstSeq[2:0]			–	–	–	BBstEn[1:0]	
0x41	BBstCfg[7:0]	BBstISetLookUpDis	–	–	BBstLowEMI	BBstActDsc	BBstRampEn	BBstMode	BBstPsvDisc
0x42	BBstVSet[7:0]	–	–	BBstVSet[5:0]					
0x43	BBstISet[7:0]	BBstIPSet2[3:0]				BBstIPSet1[3:0]			
0x44	BBstCfg1[7:0]	–	BBstIAdptDis	BBstFast	BBstZCCmpDis	BBstFETScale	BBstMPC1FastCntl	BBFHighSh[1:0]	
0x45	BBstCtr0[7:0]	BBstMPC7	BBstMPC6	BBstMPC5	BBstMPC4	BBstMPC3	BBstMPC2	BBstMPC1	BBstMPC0
0x46	BBstCtr1[7:0]	–	–	–	BBstDvsCfg[4:0]				
0x47	BBstDvsCfg0[7:0]	–	–	BBstDvsVlt0[5:0]					
0x48	BBstDvsCfg1[7:0]	–	–	BBstDvsVlt1[5:0]					
0x49	BBstDvsCfg2[7:0]	–	–	BBstDvsVlt2[5:0]					
0x4A	BBstDvsCfg3[7:0]	–	–	BBstDvsVlt3[5:0]					
0x4B	BBstDvsSpi[7:0]	–	–	BBstSPIVlt[5:0]					
LDO1									
0x51	LDO1Ena[7:0]	LDO1Seq[2:0]			–	–	–	LDO1En[1:0]	
0x52	LDO1Cfg[7:0]	–	–	–	LDO1_MPC0CNF	LDO1_MPC0CNT	LDO1ActDsc	LDO1Mode	LDO1PsvDsc
0x53	LDO1VSet[7:0]	–	–	LDO1VSet[5:0]					
0x54	LDO1Ctr[7:0]	LDO1MPC7	LDO1MPC6	LDO1MPC5	LDO1MPC4	LDO1MPC3	LDO1MPC2	LDO1MPC1	LDO1MPC0
LDO2									
0x55	LDO2Ena[7:0]	LDO2Seq[2:0]			–	–	–	LDO2En[1:0]	

ADDRESS	NAME	MSB							LSB
0x56	LDO2Cfg[7:0]	–	–	–	–	LDO2Supply	LDO2ActDsc	LDO2Mode	LDO2PsvDsc
0x57	LDO2VSet[7:0]	–	–	–	LDO2VSet[4:0]				
0x58	LDO2Ctr[7:0]	LDO2MPC7	LDO2MPC6	LDO2MPC5	LDO2MPC4	LDO2MPC3	LDO2MPC2	LDO2MPC1	LDO2MPC0
Load Switch 1									
0x59	LSW1Ena[7:0]	LSW1Seq[2:0]			–	–	–	LSW1En[1:0]	
0x5A	LSW1Cfg[7:0]	–	–	–	–	–	LSW1ActDsc	LSW1Lowlq	LSW1PsvDsc
0x5B	LSW1Ctr[7:0]	LSW1MPC7	LSW1MPC6	LSW1MPC5	LSW1MPC4	LSW1MPC3	LSW1MPC2	LSW1MPC1	LSW1MPC0
Load Switch 2									
0x5C	LSW2Ena[7:0]	LSW2Seq[2:0]			–	–	–	LSW2En[1:0]	
0x5D	LSW2Cfg[7:0]	–	–	–	–	–	LSW2ActDsc	LSW2Lowlq	LSW2PsvDsc
0x5E	LSW2Ctr[7:0]	LSW2MPC7	LSW2MPC6	LSW2MPC5	LSW2MPC4	LSW2MPC3	LSW2MPC2	LSW2MPC1	LSW2MPC0
Charge Pump									
0x5F	ChgPmpEna[7:0]	ChgPmpSeq[2:0]			–	–	–	ChgPmpEn[1:0]	
0x60	ChgPmpCfg[7:0]	–	–	–	–	–	–	CPVSet	ChgPmpPsv
0x61	ChgPmpCtr[7:0]	CHGPMPMPC7	CHGPMPMPC6	CHGPMPMPC5	CHGPMPMPC4	CHGPMPMPC3	CHGPMPMPC2	CHGPMPMPC1	CHGPMPMPC0
Boost									
0x62	BoostEna[7:0]	BoostSeq[2:0]			–	–	–	BstEn[1:0]	
0x63	BoostCfg[7:0]	–	–	–	–	BstPsvDsc	BstIAdptEn	BstFastStrt	BstFETScale
0x64	BoostISet[7:0]	BstISetLookUpDis	–	–	–	BstISet[3:0]			
0x65	BoostVSet[7:0]	–	–	BstVSet[5:0]					
0x66	BoostCtr[7:0]	BstMPC7	BstMPC6	BstMPC5	BstMPC4	BstMPC3	BstMPC2	BstMPC1	BstMPC0
MPC Control									
0x67	MPC0Cfg[7:0]	MPC0Read	–	–	MPC0Out	MPC0OD	MPC0HiZB	MPC0Res	MPC0Pup
0x68	MPC1Cfg[7:0]	MPC1Read	–	–	MPC1Out	MPC1OD	MPC1HiZB	MPC1Res	MPC1Pup
0x69	MPC2Cfg[7:0]	MPC2Read	–	–	MPC2Out	MPC2OD	MPC2HiZB	MPC2Res	MPC2Pup
0x6A	MPC3Cfg[7:0]	MPC3Read	–	–	MPC3Out	MPC3OD	MPC3HiZB	MPC3Res	MPC3Pup
0x6B	MPC4Cfg[7:0]	MPC4Read	–	–	MPC4Out	MPC4OD	MPC4HiZB	MPC4Res	MPC4Pup
0x6C	MPC5Cfg[7:0]	MPC5Read	–	–	MPC5Out	MPC5OD	MPC5HiZB	MPC5Res	MPC5Pup

ADDRESS	NAME	MSB							LSB
0x6D	MPC6Cfg[7:0]	MPC6Read	–	–	MPC6Out	MPC6OD	MPC6HiZB	MPC6Res	MPC6Pup
0x6E	MPC7Cfg[7:0]	MPC7Read	–	–	MPC7Out	MPC7OD	MPC7HiZB	MPC7Res	MPC7Pup
0x6F	MPCItrSts[7:0]	–	–	USBOkMPCSts	–	–	BK3PgMPCSts	BK2PgMPCSts	BK1PgMPCSts
0x70	BK1DedIntCfg[7:0]	BK1PGMPCInt	BK1MPC6Sel	BK1MPC5Sel	BK1MPC4Sel	BK1MPC3Sel	BK1MPC2Sel	BK1MPC1Sel	BK1MPC0Sel
0x71	BK2DedIntCfg[7:0]	BK2PGMPCInt	BK2MPC6Sel	BK2MPC5Sel	BK2MPC4Sel	BK2MPC3Sel	BK2MPC2Sel	BK2MPC1Sel	BK2MPC0Sel
0x72	BK3DedIntCfg[7:0]	BK3PGMPCInt	BK3MPC6Sel	BK3MPC5Sel	BK3MPC4Sel	BK3MPC3Sel	BK3MPC2Sel	BK3MPC1Sel	BK3MPC0Sel
0x73	HptDedIntCfg[7:0]	HptStatDedInt	HPTMPC6Sel	HPTMPC5Sel	HPTMPC4Sel	HPTMPC3Sel	HPTMPC2Sel	HPTMPC1Sel	HPTMPC0Sel
0x74	ADCDedIntCfg[7:0]	ADCStatMPCInt	ADCMPC6Sel	ADCMPC5Sel	ADCMPC4Sel	ADCMPC3Sel	ADCMPC2Sel	ADCMPC1Sel	ADCMPC0Sel
0x75	USBOkDedIntCfg[7:0]	USBOkMPCInt	USBOkMPC6Sel	USBOkMPC5Sel	USBOkMPC4Sel	USBOkMPC3Sel	USBOkMPC2Sel	USBOkMPC1Sel	USBOkMPC0Sel
LED Current Sinks									
0x78	LEDCommon[7:0]	LED_BoostLoop	–	–	LED_Open[2:0]			LEDIStep[1:0]	
0x79	LED0Ref[7:0]	–	–	–	–	–	–	LED0_REFSEL[1:0]	
0x7A	LED0Ctr[7:0]	LED0En[2:0]			LED0ISet[4:0]				
0x7B	LED1Ctr[7:0]	LED1En[2:0]			LED1ISet[4:0]				
0x7C	LED2Ctr[7:0]	LED2En[2:0]			LED2ISet[4:0]				
Boot Behavior and PFNx status									
0x7D	PFN[7:0]	–	–	–	–	–	–	PFN2Pin	PFN1Pin
0x7E	BootCfg[7:0]	PwrRstCfg[3:0]				SftRstCfg	BootDly[1:0]		ChgAlwTry
Power Commands and Lock Function									
0x7F	PwrCfg[7:0]	–	–	–	–	–	–	–	StayOn
0x80	PwrCmd[7:0]	PwrCmd[7:0]							
0x81	BuckCfg[7:0]	Bk2FrcDCM	Bk1FrcDCM	Bk3DVSCur	Bk2DVSCur	Bk1DVSCur	Bk3LowBW	Bk2LowBW	Bk1LowBW
0x83	LockMsk[7:0]	LD2Lck	LD1Lck	BBLck	BstLck	BK3Lck	BK2Lck	BK1Lck	ChgLck
0x84	LockUnlock[7:0]	PASSWD[7:0]							
SFOUT									
0x86	SFOUTCtr[7:0]	SFOUTVSet	–	–	–	–	–	SFOUTEn[1:0]	
0x87	SFOUTMPC[7:0]	SFOUTMPC7	SFOUTMPC6	SFOUTMPC5	SFOUTMPC4	SFOUTMPC3	SFOUTMPC2	SFOUTMPC1	SFOUTMPC0
OTP Readback									
0x88	I2C_OTP ADD[7:0]	OTPDIG__ADD[7:0]							
0x89	I2C_OTP DAT[7:0]	OTPDIG__DAT[7:0]							

Register Details

ChipID (0x00)

BIT	7	6	5	4	3	2	1	0
Field	ChipRev[7:0]							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ChipRev	7:0	ChipRev[7:0] bits show information about the hardware revision of the MAX20360.

Status0 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ThmStat[2:0]			ChgStat[2:0]		
Access Type	–	–	Read Only			Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
ThmStat	5:3	Status of thermistor monitoring.	000: Cold zone ($V_{THM\_COLD} < V_{THM} < V_{THM\_DIS}$) 001: Cool zone($V_{THM\_COOL} < V_{THM} < V_{THM\_COLD}$) 010: Room zone ($V_{THM\_WARM} < V_{THM} < V_{THM\_COOL}$) 011: Warm zone ($V_{THM\_HOT} < V_{THM} < V_{THM\_WARM}$) 100: Hot zone ($V_{THM} < V_{THM\_HOT}$) 101: No thermistor detected ($V_{THM} > V_{THM\_DIS}$) 110: Thermistor monitoring disabled because CHGIN input voltage is present and ChgThmEn[1:0] = "00" or because CHGIN input voltage is not present and ChgThmEn[1:0] = HrvThmEn[1:0] = "00". 111: Thermistor monitoring disabled because CHGIN input voltage is not present, ChgThmEn[1:0] is not equal to "00" and HrvThmEn[1:0] = "00".
ChgStat	2:0	Status of charger	000: Charger off 001: Charging suspended due to temperature (see Figure 32, the Battery Charger-State Diagram) 010: Precharge in progress 011: Fast-charge constant current in progress 100: Fast-charge constant voltage in progress 101: Maintain charge in progress 110: Maintain charger timer done 111: Charger fault condition (see Figure 32, the Battery Charger-State Diagram)

Status1 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ILim	UsbOVP	UsbOk	ChgJEITASD	ChgJEITAReg	ChgTmo
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
ILim	5	Status of CHGIN input current limit. Valid only when CHGIN input voltage is present and [UsbOVP,UsbOk] = "01".	0: CHGIN input current below limit 1: CHGIN input current limit active
UsbOVP	4	Status of CHGIN overvoltage protection (OVP).	0: CHGIN overvoltage not detected 1: CHGIN overvoltage detected
UsbOk	3	Status of CHGIN input voltage.	0: CHGIN input voltage not present or outside of valid range 1: CHGIN input voltage present and valid
ChgJEITASD	2	Status of battery charger shutdown due to JEITA. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = "01" and charger is enabled.	0: Charger operating normally or disabled 1: Charger disabled due to JEITA
ChgJEITAReg	1	Status of battery charger current or voltage reduction due to JEITA. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = "01" and charger is enabled.	0: Charger operating normally or disabled. 1: Charger current or voltage being actively reduced due to JEITA.
ChgTmo	0	Status of charger time-out condition. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = "01" and charger is enabled.	0: Charger operating normally or disabled 1: Charger has reached a time-out condition

Status2 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	ChgThmSD	–	ThmLDO_LSW	UVLOLDO2	UVLOLDO1	–	LSW1Tmo	LSW2Tmo
Access Type	Read Only	–	Read Only	Read Only	Read Only	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
ChgThmSD	7	Status of input limiter and charger thermal shutdown. Valid only when CHGIN input voltage is present.	0: Input limiter and charger operating normally 1: Input limiter and charger in thermal shutdown
ThmLDO_LSW	5	Status of LDO1, LDO2, LSW1, LSW2 Thermal Shutdown	0: All the above blocks are operating normally 1: One of the above blocks is in thermal shutdown
UVLOLDO2	4	Status of LDO2 UVLO	0: LDO2 operating normally 1: LDO2 UVLO active
UVLOLDO1	3	Status of LDO1 UVLO	0: LDO1 operating normally 1: LDO1 UVLO active
LSW1Tmo	1	LSW1 failed to startup during the timeout period.	

BITFIELD	BITS	DESCRIPTION	DECODE
LSW2Tmo	0	LSW2 failed to startup during the timeout period.	

Status3 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	BBstFault	HrvBatCmp	SysBatLim	ChgSysLim	ChgStep	ThmBk1	ThmBk2	ThmBk3
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BBstFault	7	Status of Buck-Boost Fault	0: Buck-Boost operating normally 1: Buck-Boost under fault condition
HrvBatCmp	6	Status of harvester BAT comparator. Valid only when harvester interaction is enabled when HrvEn=1.	0: V_{BAT} < $V_{HARV\_BAT\_REG}$ (with $V_{HARV\_BAT\_RECHG}$ hysteresis) 1: V_{BAT} > $V_{HARV\_BAT\_REG}$ (with $V_{HARV\_BAT\_RECHG}$ hysteresis)
SysBatLim	5	Status of charger regulation due to SYS voltage. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = "01" and charger is enabled.	0: Charge current is not being actively reduced to regulate V_{SYS} 1: Charge current actively being reduced to regulate V_{SYS} collapse
ChgSysLim	4	Status of input limiter regulation due to CHGIN voltage. Valid only when CHGIN input voltage is present and [UsbOVP,UsbOk] = "01".	0: Input limiter current is not being actively reduced to regulate V_{CHGIN} 1: Input limiter current is actively being reduced to regulate V_{CHGIN} collapse
ChgStep	3	Status of charger step-charge current reduction. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = "01" and charger is enabled.	0: Charger step-charge current reduction not active 1: Charger step-charge current reduction active
ThmBk1	2	Status of Buck1 Thermal Shutdown	0: Buck1 operating normally 1: Buck1 in thermal shutdown
ThmBk2	1	Status of Buck2 Thermal Shutdown	0: Buck2 operating normally 1: Buck2 in thermal shutdown
ThmBk3	0	Status of Buck3 Thermal Shutdown	0: Buck3 operating normally 1: Buck3 in thermal shutdown

Status4 (0x05)

BIT	7	6	5	4	3	2	1	0
Field	BatGood	BatRegDone	BstFault	–	–	–	–	–
Access Type	Read Only	Read Only	Read Only	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
BatGood	7	Status of charger BatGood comparator. Valid only when CHGIN input voltage is present and [UsbOVP,UsbOk] = "01".	0: V_{BAT} < V_{BAT_UVLO} 1: V_{BAT} > V_{BAT_UVLO} or CHGIN input voltage not present

BITFIELD	BITS	DESCRIPTION	DECODE
BatRegDone	6	Status of charger BAT voltage regulation. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = "01", charger is enabled and SysBatLim = 0.	0: $V_{BAT} < V_{BAT\_REG}$ 1: $V_{BAT} \geq V_{BAT\_REG}$
BstFault	5	Status of Buck-Boost Fault	0: Buck-Boost operating normally 1: Buck-Boost under fault condition

Int0 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	ThmStatInt	ChgStatInt	ILimInt	UsbOVPInt	UsbOkInt	ChgJEITASDInt	ChgJEITARegInt	ChgTmoInt
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
ThmStatInt	7	Change in ThmStat[2:0] caused an interrupt.
ChgStatInt	6	Change in ChgStat[2:0] caused an interrupt.
ILimInt	5	Change in ILim caused an interrupt.
UsbOVPInt	4	Change in UsbOVP caused an interrupt.
UsbOkInt	3	Change in UsbOk caused an interrupt.
ChgJEITASDInt	2	Change in ChgJEITASD caused an interrupt.
ChgJEITARegInt	1	Change in ChgJEITAReg caused an interrupt.
ChgTmoInt	0	Change in ChgTmo caused an interrupt.

Int1 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	ChgThmSDInt	–	ThmLDO_LSWInt	UVLOLDO2Int	UVLOLDO1Int	–	LSW1TmoInt	LSW2TmoInt
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
ChgThmSDInt	7	Change in ChgThmSD caused an interrupt.
ThmLDO_LSWInt	5	Change in ThmLDO_LSW caused an interrupt.
UVLOLDO2Int	4	Change in UVLOLDO2 caused an interrupt.
UVLOLDO1Int	3	Change in UVLOLDO1 caused an interrupt.
LSW1TmoInt	1	Change in LSW1Tmo caused an interrupt.
LSW2TmoInt	0	Change in LSW2Tmo caused an interrupt.

Int2 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	BBstFaultInt	HrvBatCmplnt	SysBatLimInt	ChgSysLimInt	ChgStepInt	ThmBk1Int	ThmBk2Int	ThmBk3Int
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BBstFaultInt	7	Change in BBstFault caused an interrupt.
HrvBatCmpInt	6	Change in HrvBatCmp caused an interrupt.
SysBatLimInt	5	Change in SysBatLim caused an interrupt.
ChgSysLimInt	4	Change in ChgSysLim caused an interrupt.
ChgStepInt	3	Change in ChgStep caused an interrupt.
ThmBk1Int	2	Change in ThmBk1 caused an interrupt.
ThmBk2Int	1	Change in ThmBk2 caused an interrupt.
ThmBk3Int	0	Change in ThmBk3 caused an interrupt.

Int3 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	BatGoodInt	BatRegDoneInt	BstFaultInt	–	I2cCrcFailInt	I2cTmoInt	HptStatInt	ADCStatInt
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
BatGoodInt	7	Change in BatGood caused an interrupt.
BatRegDoneInt	6	Change in BatRegDone caused an interrupt.
BstFaultInt	5	Change in BstFault caused an interrupt.
I2cCrcFailInt	3	CRC Failure - I^2C write not performed
I2cTmoInt	2	I^2C Watchdog Timer Expired due to 100ms bus inactivity between START and STOP conditions.
HptStatInt	1	Haptic driver general status interrupt. HptStatInt is issued in case any other haptic driver related interrupt is issued.
ADCStatInt	0	ADC general status interrupt. ADCStatInt is issued in case any other ADC related interrupt is issued.

IntMask0 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	ThmStatIntM	ChgStatIntM	ILimIntM	UsbOVPIntM	UsbOkIntM	ChgJEITASDIntM	ChgJEITARegIntM	ChgTmoIntM
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ThmStatIntM	7	ThmStatIntM masks the ThmStatInt interrupt in the Int0 register (0x06).	0: Masked 1: Not masked
ChgStatIntM	6	ChgStatIntM masks the ChgStatInt interrupt in the Int0 register (0x06).	0: Masked 1: Not masked
ILimIntM	5	ILimIntM masks the ILimInt interrupt in the Int0 register (0x06).	0: Masked 1: Not masked
UsbOVPIntM	4	UsbOVPIntM masks the UsbOVPInt interrupt in the Int0 register (0x06).	0: Masked 1: Not masked
UsbOkIntM	3	UsbOkIntM masks the UsbOkInt interrupt in the Int0 register (0x06).	0: Masked 1: Not masked

BITFIELD	BITS	DESCRIPTION	DECODE
ChgJEITASDIntM	2	ChgJEITASDIntM masks the ChgJEITASDInt interrupt in the Int0 register (0x06).	0: Masked 1: Not masked
ChgJEITARegIntM	1	ChgJEITARegIntM masks the ChgJEITARegInt interrupt in the Int0 register (0x06).	0: Masked 1: Not masked
ChgTmoIntM	0	ChgTmoIntM masks the ChgTmoInt interrupt in the Int0 register (0x06).	0: Masked 1: Not masked

IntMask1 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	ChgThmSDIntM	–	ThmLDO_LSWIntM	UVLOLDO2IntM	UVLOLDO1IntM	–	LSW1TmoIntM	LSW2TmoIntM
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ChgThmSDIntM	7	ChgThmSDIntM masks the ChgThmSDInt interrupt in the Int1 register (0x07).	0: Masked 1: Not masked
ThmLDO_LSWIntM	5	ThmLDO_LSWIntM masks the ThmLDO_LSWInt interrupt in the Int1 register (0x07).	0: Masked 1: Not masked
UVLOLDO2IntM	4	UVLOLDO2IntM masks the UVLOLDO2Int interrupt in the Int1 register (0x07).	0: Masked 1: Not masked
UVLOLDO1IntM	3	UVLOLDO1IntM masks the UVLOLDO1Int interrupt in the Int1 register (0x07).	0: Masked 1: Not masked
LSW1TmoIntM	1	LSW1TmoIntM masks the LSW1TmoInt interrupt in the Int1 register (0x07).	0: Masked 1: Not masked
LSW2TmoIntM	0	LSW2TmoIntM masks the LSW2TmoInt interrupt in the Int1 register (0x07).	0: Masked 1: Not masked

IntMask2 (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	BBstFaultIntM	HrvBatCmplntM	SysBatLimIntM	ChgSysLimIntM	ChgStepIntM	ThmBk1IntM	ThmBk2IntM	ThmBk3IntM
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBstFaultIntM	7	BBstFaultIntM masks the BBstFaultInt interrupt in the Int2 register (0x08).	0: Masked 1: Not masked
HrvBatCmpIntM	6	HrvBatCmpIntM masks the HrvBatCmpInt interrupt in the Int2 register (0x08).	0: Masked 1: Not masked
SysBatLimIntM	5	SysBatLimIntM masks the SysBatLimInt interrupt in the Int2 register (0x08).	0: Masked 1: Not masked
ChgSysLimIntM	4	ChgSysLimIntM masks the ChgSysLimInt interrupt in the Int2 register (0x08).	0: Masked 1: Not masked
ChgStepIntM	3	ChgStepIntM masks the ChgStepInt interrupt in the Int2 register (0x08).	0: Masked 1: Not masked

BITFIELD	BITS	DESCRIPTION	DECODE
ThmBk1IntM	2	ThmBk1IntM masks the ThmBk1Int interrupt in the Int2 register (0x08).	0: Masked 1: Not masked
ThmBk2IntM	1	ThmBk2IntM masks the ThmBk2Int interrupt in the Int2 register (0x08).	0: Masked 1: Not masked
ThmBk3IntM	0	ThmBk3IntM masks the ThmBk3Int interrupt in the Int2 register (0x08).	0: Masked 1: Not masked

IntMask3 (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	BatGoodIntM	BatRegDoneIntM	BstFaultIntM	–	I2cCrcFailIntM	I2cTmoIntM	HptStatIntM	ADCStatIntM
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BatGoodIntM	7	BatGoodIntM masks the BatGoodInt interrupt in the Int3 register (0x09).	0: Masked 1: Not masked
BatRegDoneIntM	6	BatRegDoneIntM masks the BatRegDoneInt interrupt in the Int3 register (0x09).	0: Masked 1: Not masked
BstFaultIntM	5	BstFaultIntM masks the BstFaultInt interrupt in the Int3 register (0x09).	0: Masked 1: Not masked
I2cCrcFailIntM	3	I2CCRCFailIntM masks the I2CCRCFailInt interrupt in the Int3 register (0x09).	0: Masked 1: Not masked
I2cTmoIntM	2	I2CTmoIntM masks the I2CTmoInt interrupt in the Int3 register (0x09).	0: Masked 1: Not masked
HptStatIntM	1	HptStatIntM masks the HptStatInt interrupt in the Int3 register (0x09).	0: Masked 1: Not masked
ADCStatIntM	0	ADCStatIntM masks the ADCStatInt interrupt in the Int3 register (0x09).	0: Masked 1: Not masked

ILimCntl (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	SysMinVlt[2:0]			ILimBlank[1:0]		ILimCntl[2:0]		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SysMinVlt	7:5	System (SYS) voltage minimum threshold. SYS voltage below which charging current is reduced to prevent V_{SYS} from collapsing.	000: 3.6V 001: 3.7V 010: 3.8V 011: 3.9V 100: 4.0V 101: 4.1V 110: 4.2V 111: 4.3V
ILimBlank	4:3	CHGIN input current limiter blanking time (during which the current is limited to I_{LIM_MAX}).	00: No debounce (allow a few clock cycles for resampling) 01: 0.5ms 10: 1.0ms 11: 10.0ms

BITFIELD	BITS	DESCRIPTION	DECODE
ILimCntl	2:0	CHGIN programmable input current limit.	000: 50mA 001: 90mA 010: 150mA 011: 200mA 100: 300mA 101: 400mA 110: 450mA 111: 1000mA

ChgCntl0 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	FrcPChg	ChgBatReChg[1:0]		ChgBatReg[3:0]				ChgEn
Access Type	Write, Read	Write, Read		Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FrcPChg	7	Charger forced precharge mode. Valid only if ChgEn = 1.	0: Charger operating normally 1: Charger current is forced to precharge value
ChgBatReChg	6:5	Charger recharge threshold in relation to ChgBatReg[3:0].	00: ChgBatReg[3:0] -70mV 01: ChgBatReg[3:0] -120mV 10: ChgBatReg[3:0] -170mV 11: ChgBatReg[3:0] -220mV
ChgBatReg	4:1	Charger battery regulation voltage.	0000: 4.05V 0001: 4.10V 0010: 4.15V 0011: 4.20V 0100: 4.25V 0101: 4.30V 0110: 4.35V 0111: 4.40V 1000: 4.45V 1001: 4.50V 1010: 4.55V 1011: 4.60V 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved
ChgEn	0	Charger on/off control. Does not affect input limiter and SYS node.	0: Charger disabled 1: Charger enabled

ChgCntl1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	BatPD	VPChg[2:0]			IPChg[1:0]		IChgDone[1:0]	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
BatPD	7	Pulldown resistor enable on BAT.	0: Pulldown resistor disabled 1: Pulldown resistor enabled

BITFIELD	BITS	DESCRIPTION	DECODE
VPChg	6:4	Charger precharge voltage rising threshold.	000: 2.10V 001: 2.25V 010: 2.40V 011: 2.55V 100: 2.70V 101: 2.85V 110: 3.00V 111: 3.15V
IPChg	3:2	Charger precharge current.	00: 0.05 x I_{FCHG} 01: 0.10 x I_{FCHG} 10: 0.20 x I_{FCHG} 11: 0.30 x I_{FCHG}
IChgDone	1:0	Charger charge-done current threshold.	00: 0.05 x I_{FCHG} 01: 0.10 x I_{FCHG} 10: 0.20 x I_{FCHG} 11: 0.30 x I_{FCHG}

ChgTmr (0x12)

BIT	7	6	5	4	3	2	1	0
Field	ChgAutoStop	ChgAutoReSta	MtChgTmr[1:0]		FChgTmr[1:0]		PChgTmr[1:0]	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ChgAutoStop	7	Charger auto-stop control. Controls the transition from maintain-charge to maintain-charge done. See Figure 32, the Battery Charger-State Diagram.	0: Auto-stop disabled 1: Auto-stop enabled
ChgAutoReSta	6	Charger auto-restart control. See Figure 32, the Battery Charger-State Diagram.	0: Charger remains in maintain-charge done even when V_{BAT} is less than recharge threshold. 1: Charger automatically restarts when V_{BAT} drops below recharge threshold.
MtChgTmr	5:4	Charger maintain-charge timer.	00: 0min 01: 15min 10: 30min 11: 60min
FChgTmr	3:2	Charger fast-charge timer.	00: 75min 01: 150min 10: 300min 11: 600min
PChgTmr	1:0	Charger precharge timer.	00: 30min 01: 60min 10: 120min 11: 240min

StepChgCfg0 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	–	ChgStepHys[2:0]			ChgStepRise[3:0]			
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ChgStepHys	6:4	Charger step-charge voltage threshold hysteresis.	000: 100mV 001: 200mV 010: 300mV 011: 400mV 100: 500mV 101: 600mV 110: Reserved 111: Reserved
ChgStepRise	3:0	Charger step-charge voltage rising threshold.	0000: 3.80V 0001: 3.85V 0010: 3.90V 0011: 3.95V 0100: 4.00V 0101: 4.05V 0110: 4.10V 0111: 4.15V 1000: 4.20V 1001: 4.25V 1010: 4.30V 1011: 4.35V 1100: 4.40V 1101: 4.45V 1110: 4.50V 1111: 4.55V

StepChgCfg1 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	VSysUvlo[1:0]		ChgIStep[2:0]		
Access Type	–	–	–	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VSysUvlo	4:3	SYS UVLO falling voltage threshold selector.	00: 2.7V 01: 2.9V 10: 3.0V 11: 3.2V
ChgIStep	2:0	Charger step-charge current reduction. Sets the modified fast-charge current once ChgStepRise[3:0] threshold is exceeded. The fast-charge current is the minimum of the value set by ChgIStep[2:0] and the applicable charger current reduction related to thermistor monitoring (see ChgCoolIFchg[2:0], ChgRoomIFchg[2:0], ChgWarmIFchg[2:0]).	000: 0.2 x I_{FCHG} 001: 0.3 x I_{FCHG} 010: 0.4 x I_{FCHG} 011: 0.5 x I_{FCHG} 100: 0.6 x I_{FCHG} 101: 0.7 x I_{FCHG} 110: 0.8 x I_{FCHG} 111: 1.0 x I_{FCHG}

ThmCfg0 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	–	ChgThmEn[1:0]		ChgCoolBatReg[1:0]		ChgCoolFChg[2:0]		
Access Type	–	Write, Read		Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgThmEn	6:5	Charger thermistor monitoring related control. Valid only when CHGIN input voltage is present.	00: Thermistor monitoring disabled 01: Thermistor monitoring permanently enabled and charger enabled in the cool and room temperature zones 10: Thermistor monitoring permanently enabled and charger enabled in the room and warm temperature zones 11: Thermistor monitoring permanently enabled and charger enabled in the cool, room, and warm temperature zones
ChgCoolBatReg	4:3	Charger cool zone battery regulation voltage reduction. Sets the modified battery regulation voltage when the cool temperature zone is entered according to thermistor monitoring.	00: ChgBatReg[3:0] -150mV 01: ChgBatReg[3:0] -100mV 10: ChgBatReg[3:0] -50mV 11: ChgBatReg[3:0]
ChgCoolFChg	2:0	Charger cool zone fast-charge current reduction. Sets the modified fast-charge current when the cool temperature zone is entered according to thermistor monitoring.	000: 0.2 x I_{FCHG} 001: 0.3 x I_{FCHG} 010: 0.4 x I_{FCHG} 011: 0.5 x I_{FCHG} 100: 0.6 x I_{FCHG} 101: 0.7 x I_{FCHG} 110: 0.8 x I_{FCHG} 111: 1.0 x I_{FCHG}

ThmCfg1 (0x16)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ChgRoomBatReg[1:0]		ChgRoomIFChg[2:0]		
Access Type	–	–	–	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgRoomBatReg	4:3	Charger room zone battery regulation voltage reduction. Sets the modified battery regulation voltage when the room temperature zone is entered according to thermistor monitoring.	00: ChgBatReg[3:0] -150mV 01: ChgBatReg[3:0] -100mV 10: ChgBatReg[3:0] -50mV 11: ChgBatReg[3:0]
ChgRoomIFChg	2:0	Charger room zone fast-charge current reduction. Sets the modified fast-charge current when the room temperature zone is entered according to thermistor monitoring.	000: 0.2 x I_{FCHG} 001: 0.3 x I_{FCHG} 010: 0.4 x I_{FCHG} 011: 0.5 x I_{FCHG} 100: 0.6 x I_{FCHG} 101: 0.7 x I_{FCHG} 110: 0.8 x I_{FCHG} 111: 1.0 x I_{FCHG}

ThmCfg2 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	HrvThmEn[1:0]		–	ChgWarmBatReg[1:0]		ChgWarmIFChg[2:0]		
Access Type	Write, Read		–	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
HrvThmEn	7:6	Periodic thermistor monitoring related control. Valid when CHGIN input voltage is not present and interaction with harvester is enabled when HrvEn = 1. If HrvThmEn[1:0] is different from "00", thermistor (V_{THM}) is periodically monitored by exploiting Fuel Gauge periodic measurements timing.	00: Periodic thermistor monitoring disabled. 01: Periodic thermistor monitoring enabled and harvester charging enabled in the cool and room temperature zones. 10: Periodic thermistor monitoring enabled and harvester charging enabled in the room and warm temperature zones. 11: Periodic thermistor monitoring enabled and harvester charging enabled in the cool, room, and warm temperature zones.
ChgWarmBatReg	4:3	Charger warm zone battery regulation voltage reduction. Sets the modified battery regulation voltage when the warm temperature zone is entered according to thermistor monitoring.	00: ChgBatReg[3:0] -150mV 01: ChgBatReg[3:0] -100mV 10: ChgBatReg[3:0] -50mV 11: ChgBatReg[3:0]
ChgWarmIFChg	2:0	Charger warm zone fast-charge current reduction. Sets the modified fast-charge current when the warm temperature zone is entered according to thermistor monitoring.	000: 0.2 x I_{FCHG} 001: 0.3 x I_{FCHG} 010: 0.4 x I_{FCHG} 011: 0.5 x I_{FCHG} 100: 0.6 x I_{FCHG} 101: 0.7 x I_{FCHG} 110: 0.8 x I_{FCHG} 111: 1.0 x I_{FCHG}

HrvCfg0 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	HrvBatSys[1:0]		HrvBatReChg[1:0]		HrvBatReg[3:0]			
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
HrvBatSys	7:6	Harvester BAT-SYS FET control. Valid when CHGIN input voltage is not present and interaction with harvester is enabled when HrvEn = 1. If HrvEn = 0 and CHGIN input voltage is not present, the BAT-SYS FET is fully on (direct-path). If CHGIN input voltage is present, the BAT-SYS FET is controlled by the charger.	00: Direct-path (BAT-SYS FET fully on) forced active 01: Direct-path active if V_{BAT} < HrvBatReg[3:0] and ideal BAT-to-SYS diode active if V_{BAT} > HrvBatReg[3:0]. Once ideal diode has been activated, an hysteresis equal to HrvBatReChg[1:0] is applied on HrvBatReg[3:0] threshold. 10: Ideal BAT-to-SYS diode (BAT-SYS FET controlled in order to allow current flowing from BAT to SYS with a low drop and to not allow current flowing from SYS to BAT) forced active 11: Reserved
HrvBatReChg	5:4	Harvester recharge threshold in relation to HrvBatReg[3:0].	00: HrvBatReg[3:0] -70mV 01: HrvBatReg[3:0] -120mV 10: HrvBatReg[3:0] -170mV 11: HrvBatReg[3:0] -220mV

BITFIELD	BITS	DESCRIPTION	DECODE
HrvBatReg	3:0	Harvester battery-regulation voltage threshold.	0000: 4.05V 0001: 4.10V 0010: 4.15V 0011: 4.20V 0100: 4.25V 0101: 4.30V 0110: 4.35V 0111: 4.40V 1000: 4.45V 1001: 4.50V 1010: 4.55V 1011: 4.60V 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved

HrvCfg1 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	–	HrvThmDis	HrvWarmBatReg[1:0]		HrvRoomBatReg[1:0]		HrvCoolBatReg[1:0]	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HrvThmDis	6	Harvester charging disabled condition control. Valid when CHGIN input voltage is not present, interaction with harvester is enabled via HrvEn = 1, HrvThmEn[1:0] is different from "00" and the temperature is in a zone where charging from harvester is inhibited. If HrvEn = 1 and CHGIN input voltage is present, the harvester is permanently disabled through the MPC6 output.	0: Harvester is disabled through the MPC6 output and the BAT-SYS FET is controlled through HrvBatSys[1:0]. 1: Harvester is not disabled through the MPC6 output and ideal BAT-to-SYS diode is forced active regardless of HrvBatSys[1:0].
HrvWarmBatReg	5:4	Harvester warm zone battery regulation voltage threshold reduction. Sets the modified harvester battery regulation voltage threshold when the warm temperature zone is entered according to thermistor monitoring.	00: HrvBatReg[3:0] -150mV 01: HrvBatReg[3:0] -100mV 10: HrvBatReg[3:0] -50mV 11: HrvBatReg[3:0]
HrvRoomBatReg	3:2	Harvester room zone battery regulation voltage threshold reduction. Sets the modified harvester battery regulation voltage threshold when the room temperature zone is entered according to thermistor monitoring.	00: HrvBatReg[3:0] -150mV 01: HrvBatReg[3:0] -100mV 10: HrvBatReg[3:0] -50mV 11: HrvBatReg[3:0]
HrvCoolBatReg	1:0	Harvester cool zone battery regulation voltage threshold reduction. Sets the modified harvester battery regulation voltage threshold when the cool temperature zone is entered according to thermistor monitoring.	00: HrvBatReg[3:0] -150mV 01: HrvBatReg[3:0] -100mV 10: HrvBatReg[3:0] -50mV 11: HrvBatReg[3:0]

IVMONCfg (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	–	IVMONRatioConfig[1:0]		IVMONOffHiZ	IVMONCntl[3:0]			
Access Type	–	Write, Read		Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
IVMONRatioConfig	6:5	IVMON multiplexer resistive partition selector.	00: 1:1 01: 2:1 10: 3:1 11: 4:1
IVMONOffHiZ	4	IVMON multiplexer disabled condition. Valid when IVMONCntl = "0000".	0: IVMON is pulled low by a 59kΩ (typ) resistor. 1: IVMON is Hi-Z.
IVMONCntl	3:0	IVMON multiplexer input channel selector.	0000: IVMON multiplexer disabled. 0001: Charger current (buffered version of V_{ISET}). 0010: BAT 0011: SYS 0100: BK1OUT 0101: BK2OUT 0110: BK3OUT 0111: L1OUT 1000: L2OUT 1001: SFOUT 1010: BBOUT 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved

Buck1Ena (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	Buck1Seq[2:0]			–	–	–	Buck1En[1:0]	
Access Type	Read Only			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1Seq	7:5	Buck1 Enable Configuration	000: Disabled 001: Reserved 010: Enabled at 0% of Boot/POR Process Delay Control 011: Enabled at 25% of Boot/POR Process Delay Control 100: Enabled at 50% of Boot/POR Process Delay Control 101: Reserved 110: Reserved 111: Controlled by Buck1En [1:0] after 100% of Boot/POR Process Delay Control

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1En	1:0	Buck1 Enable Configuration (effective only when Buck1Seq = 111)	00: Disabled: BK1OUT not actively discharged unless Hard-Reset/Shutdown/Off mode 01: Enabled 10: Controlled by MPC_ (See Buck1MPC_ bits) 11: Reserved

Buck1Cfg0 (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	Buck1IntegDis	Buck1PGOODEn	Buck1Fast	Buck1PsvDsc	Buck1ActDsc	Buck1LowEMI	Buck1FETScale	Buck1EnLXSns
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1IntegDis	7	Buck1 integrator feedback disable	0: Integrator enabled 1: Integrator disabled–proportional control only
Buck1PGOODEn	6	Buck1 PGOOD comparator control	0: PGOOD comparator disabled during voltage transition after startup 1: PGOOD comparator enabled during voltage transition after startup
Buck1Fast	5	Buck1 pretrigger mode setting	0: Normal, low quiescent current operation 1: Increased quiescent mode for fast load transient response. Quiescent current increased to 30μA.
Buck1PsvDsc	4	Buck1 passive discharge control	0: Buck1 passively discharged only in Hard-Reset 1: Buck1 passively discharged in Hard-Reset or Enable Low.
Buck1ActDsc	3	Buck1 active discharge control	0: Buck1 actively discharged only in Hard-Reset 1: Buck1 actively discharged in Hard-Reset or Enable Low
Buck1LowEMI	2	Buck1 low EMI mode	0: Normal operation 1: Slow rise/fall edges on BK1LX by 3x
Buck1FETScale	1	Buck1 Force FET Scaling Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck1ISet must be < 100mA (e.g., to mitigate noise at low frequencies).	0: FET scaling disabled 1: FET scaling enabled
Buck1EnLXSns	0	Buck1 LX Sense Control Selects the condition to turn-on frewheeling FET. Keep it to 0 for Buck1Vset ≤ 1.6V	0: Enter freewheeling mode after inductor current zero-crossing 1: Enter freewheeling mode on V_{LX} high detection after inductor current zero-crossing

Buck1Cfg1 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1MPC2Fast	Buck1FPWM	Buck1IAdptDis	–	–	–
Access Type	–	–	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1MPC2Fast	5	Buck1 FAST mode by MPC2 control	0: Buck1 fast mode control by MPC2 disabled 1: Buck1 fast mode control by MPC2 enabled

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1FPWM	4	Buck1 forced PWM mode control	0: Normal operation 1: Forced PWM mode enabled
Buck1IAdptDis	3	Buck1 adaptive peak current mode control	0: Adaptive peak current mode enabled 1: Peak current fixed at value set in Buck1ISet

Buck1Iset (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	Buck1ISetLookUpDis	–	–	–	Buck1ISet[3:0]			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1ISetLookUpDis	7	Buck1 Peak Current Set by Lookup Table Disable	0: Inductor current setting is set according to look-up table 1: Inductor current setting is set by Buck1ISet
Buck1ISet	3:0	Buck1 Inductor Peak Current Setting. Valid only if Buck1ISetLookUpDis is high. For the best efficiency, use between 150mA and 200mA. Linear scale, 25mA increments, settings below 75mA can be limited by the minimum t_{ON}	0000: 0mA 0001: 25mA 0010: 50mA 0011: 75mA 0100: 100mA 0101: 125mA 0110: 150mA 0111: 175mA 1000: 200mA 1001: 225mA 1010: 250mA 1011: 275mA 1100: 300mA 1101: 325mA 1110: 350mA 1111: 375mA

Buck1VSet (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1VSet[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1VSet	5:0	Buck1 Output Voltage Setting 0.55V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.55V 000001 = 0.56V … 111111 = 1.18V

Buck1Ctr (0x20)

BIT	7	6	5	4	3	2	1	0
Field	Buck1MPC7	Buck1MPC6	Buck1MPC5	Buck1MPC4	Buck1MPC3	Buck1MPC2	Buck1MPC1	Buck1MPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1MPC7	7	Buck1 MPC7 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs	0: Buck1 not controlled by MPC7 1: Buck1 controlled by MPC7
Buck1MPC6	6	Buck1 MPC6 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs	0: Buck1 not controlled by MPC6 1: Buck1 controlled by MPC6
Buck1MPC5	5	Buck1 MPC5 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs	0: Buck1 not controlled by MPC5 1: Buck1 controlled by MPC5
Buck1MPC4	4	Buck1 MPC4 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs	0: Buck1 not controlled by MPC4 1: Buck1 controlled by MPC4
Buck1MPC3	3	Buck1 MPC3 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs	0: Buck1 not controlled by MPC3 1: Buck1 controlled by MPC3
Buck1MPC2	2	Buck1 MPC2 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs	0: Buck1 not controlled by MPC2 1: Buck1 controlled by MPC2
Buck1MPC1	1	Buck1 MPC1 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs	0: Buck1 cot controlled by MPC1 1: Buck1 controlled by MPC1
Buck1MPC0	0	Buck1 MPC0 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs	0: Buck1 not controlled by MPC0 1: Buck1 controlled by MPC0

Buck1DvsCfg0 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	Buck1DVSCfg[4:0]				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1DVSCfg	4:0		00000: DVS Modes Disabled 00001: MPC0/MPC1 00010: MPC0/MPC2 00011: MPC0/MPC3 00100: MPC0/MPC4 00101: MPC0/MPC5 00110: MPC0/MPC6 00111: MPC0/MPC7 01000: MPC1/MPC2 01001: MPC1/MPC3 01010: MPC1/MPC4 01011: MPC1/MPC5 01100: MPC1/MPC6 01101: MPC1/MPC7 01110: MPC2/MPC3 01111: MPC2/MPC4 10000: MPC2/MPC5 10001: MPC2/MPC6 10010: MPC2/MPC7 10011: MPC3/MPC4 10100: MPC3/MPC5 10101: MPC3/MPC6 10110: MPC3/MPC7 10111: MPC4/MPC5 11000: MPC4/MPC6 11001: MPC4/MPC7 11010: MPC5/MPC6 11011: MPC5/MPC7 11100: MPC6/MPC7 11101: SPI Mode >11101: RESERVED

Buck1DvsCfg1 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DVSVlt0[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DVSVlt0	5:0	Buck1 alternate output voltage setting 0 (Controlling MPCs = 00) 0.55V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.55V 000001 = 0.56V … 111111 = 1.18V

Buck1DvsCfg2 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DVSVlt1[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DVSVlt1	5:0	Buck1 alternate output voltage setting 1 (Controlling MPCs = 01) 0.55V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.55V 000001 = 0.56V … 111111 = 1.18V

Buck1DvsCfg3 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DVSVlt2[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DVSVlt2	5:0	Buck1 alternate output voltage setting 2 (Controlling MPCs = 10) 0.55V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.55V 000001 = 0.56V … 111111 = 1.18V

Buck1DvsCfg4 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DVSVlt3[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DVSVlt3	5:0	Buck1 alternate output voltage setting 3 (Controlling MPCs = 11) 0.55V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.55V 000001 = 0.56V … 111111 = 1.18V

Buck1DvsSpi (0x26)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1SPIVlt[5:0]					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
Buck1SPIVlt	5:0	Buck1 SPI DVS Readback 0.55V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.55V 000001 = 0.56V … 111111 = 1.18V

Buck2Ena (0x27)

BIT	7	6	5	4	3	2	1	0
Field	Buck2Seq[2:0]			–	–	–	Buck2En[1:0]	
Access Type	Read Only			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2Seq	7:5	Buck2 Enable Configuration	000: Disabled 001: Reserved 010: Enabled at 0% of Boot/POR Process Delay Control 011: Enabled at 25% of Boot/POR Process Delay Control 100: Enabled at 50% of Boot/POR Process Delay Control 101: Reserved 110: Reserved 111: Controlled by Buck2En [1:0] after 100% of Boot/POR Process Delay Control
Buck2En	1:0	Buck2 Enable Configuration (effective only when Buck2Seq = 111)	00: Disabled: BK2OUT not actively discharged unless Hard-Reset/Shutdown/Off mode 01: Enabled 10: Controlled by MPC_ (See Buck2MPC_ bits) 11: Reserved

Buck2Cfg (0x28)

BIT	7	6	5	4	3	2	1	0
Field	Buck2EnblNTGR	Buck2PGOODena	Buck2Fast	Buck2PsvDsc	Buck2ActDsc	Buck2LowEMI	Buck2FETScale	Buck2EnLxSns
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2EnblNTGR	7	Buck2 integrator feedback disable	0: Integrator enabled 1: Integrator disabled–proportional control only
Buck2PGOODena	6	Buck2 PGOOD comparator control	0: PGOOD comparator disabled during voltage transition after startup 1: PGOOD comparator enabled during voltage transition after startup
Buck2Fast	5	Buck2 pretrigger mode setting	0: Normal, low quiescent current operation 1: Increased quiescent mode for fast load transient response. Quiescent current increased to 30μA.

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2PsvDsc	4	Buck2 passive discharge control	0: Buck2 passively discharged only in Hard-Reset 1: Buck2 passively discharged in Hard-Reset or Enable Low.
Buck2ActDsc	3	Buck2 active discharge control	0: Buck2 actively discharged only in Hard-Reset 1: Buck2 actively discharged in Hard-Reset or Enable Low
Buck2LowEMI	2	Buck2 low EMI mode	0: Normal operation 1: Slow rise/fall edges on BK2LX by 3x
Buck2FETScale	1	Buck2 FET Scaling Control. Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck1ISet must be < 100mA (e.g., to mitigate noise at low frequencies).	0: FET scaling disabled 1: FET scaling enabled
Buck2EnLxSns	0	Buck2 LX Sense Control Selects the condition to turn-on frewheeling FET. Keep it to 0 for Buck2Vset ≤ 1.6V	0: Enter freewheeling mode after inductor current zero-crossing 1: Enter freewheeling mode on V_{LX} high detection after inductor current zero-crossing

Buck2Cfg1 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2MPCFast	Buck2FPWM	Buck2IAdptDis	–	–	–
Access Type	–	–	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2MPCFast	5	Buck2 FAST mode by MPC3 control	0: Buck2 FAST mode control by MPC3 disabled 1: Buck2 FAST mode control by MPC3 enabled
Buck2FPWM	4	Buck2 forced PWM mode control	0: Normal operation 1: Forced PWM mode enabled
Buck2IAdptDis	3	Buck2 adaptive peak current mode control	0: Adaptive peak current mode enabled 1: Peak current fixed at value set in Buck2ISet

Buck2Iset (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	Buck2ISetLookUpDis	–	–	–	Buck2ISet[3:0]			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2ISetLookUpDis	7	Buck2 peak current set by lookup table disabled	0: Inductor current setting is set according to lookup table 1: Inductor current setting is set by Buck2ISet

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2ISet	3:0	Buck2 Inductor Peak Current Setting. Valid only if Buck2ISetLookUpDis is high. For the best efficiency, use between 150mA and 200mA. Linear scale, 25mA increments, settings below 75mA can be limited by the minimum t_{ON}	0000: 0mA 0001: 25mA 0010: 50mA 0011: 75mA 0100: 100mA 0101: 125mA 0110: 150mA 0111: 175mA 1000: 200mA 1001: 225mA 1010: 250mA 1011: 275mA 1100: 300mA 1101: 325mA 1110: 350mA 1111: 375mA

Buck2VSet (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2VSet[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2VSet	5:0	Buck2 Output Voltage Setting 0.55V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.55V 000001 = 0.575V … 111111 = 2.125V

Buck2Ctr (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	Buck2MPC7	Buck2MPC6	Buck2MPC5	Buck2MPC4	Buck2MPC3	Buck2MPC2	Buck2MPC1	Buck2MPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2MPC7	7	Buck2 MPC7 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs	0: Buck2 not controlled by MPC7 1: Buck2 Controlled by MPC7
Buck2MPC6	6	Buck2 MPC6 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs	0: Buck2 not controlled by MPC6 1: Buck2 controlled by MPC6

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2MPC5	5	Buck2 MPC5 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs	0: Buck2 not controlled by MPC5 1: Buck2 controlled by MPC5
Buck2MPC4	4	Buck2 MPC4 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs	0: Buck2 not controlled by MPC4 1: Buck2 controlled by MPC4
Buck2MPC3	3	Buck2 MPC3 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs	0: Buck2 not controlled by MPC3 1: Buck2 controlled by MPC3
Buck2MPC2	2	Buck2 MPC2 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs	0: Buck2 not controlled by MPC2 1: Buck2 controlled by MPC2
Buck2MPC1	1	Buck2 MPC1 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs	0: Buck2 not controlled by MPC1 1: Buck2 controlled by MPC1
Buck2MPC0	0	Buck2 MPC0 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs	0: Buck2 not controlled by MPC0 1: Buck2 controlled by MPC0

Buck2DvsCfg0 (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	Buck2DvsCfg[4:0]				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2DvsCfg	4:0		00000: DVS Modes Disabled 00001: MPC0/MPC1 00010: MPC0/MPC2 00011: MPC0/MPC3 00100: MPC0/MPC4 00101: MPC0/MPC5 00110: MPC0/MPC6 00111: MPC0/MPC7 01000: MPC1/MPC2 01001: MPC1/MPC3 01010: MPC1/MPC4 01011: MPC1/MPC5 01100: MPC1/MPC6 01101: MPC1/MPC7 01110: MPC2/MPC3 01111: MPC2/MPC4 10000: MPC2/MPC5 10001: MPC2/MPC6 10010: MPC2/MPC7 10011: MPC3/MPC4 10100: MPC3/MPC5 10101: MPC3/MPC6 10110: MPC3/MPC7 10111: MPC4/MPC5 11000: MPC4/MPC6 11001: MPC4/MPC7 11010: MPC5/MPC6 11011: MPC5/MPC7 11100: MPC6/MPC7 11101: SPI Mode >11101: RESERVED

Buck2DvsCfg1 (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DvsVlt0[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DvsVlt0	5:0	Buck2 alternate output voltage setting 0 (Controlling MPCs = 00) 0.55V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.55V 000001 = 0.575V … 111111 = 2.125V

Buck2DvsCfg2 (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DvsVlt1[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DvsVlt1	5:0	Buck2 alternate output voltage setting 1 (Controlling MPCs = 01) 0.55V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.55V 000001 = 0.575V … 111111 = 2.125V

Buck2DvsCfg3 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DvsVlt2[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DvsVlt2	5:0	Buck2 alternate output voltage setting 2 (Controlling MPCs = 10) 0.55V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.55V 000001 = 0.575V … 111111 = 2.125V

Buck2DvsCfg4 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DvsVlt3[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DvsVlt3	5:0	Buck2 alternate output voltage setting 3 (Controlling MPCs = 11) 0.55V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.55V 000001 = 0.575V … 111111 = 2.125V

Buck2DvsSpi (0x32)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2SPIVlt[5:0]					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
Buck2SPIVlt	5:0	Buck2 SPI DVS Readback. 0.55V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.550V 000001 = 0.525V … 111111 = 2.125V

Buck3Ena (0x34)

BIT	7	6	5	4	3	2	1	0
Field	Buck3Seq[2:0]			–	–	–	Buck3En[1:0]	
Access Type	Read Only			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3Seq	7:5	Buck3 enable configuration	000: Disabled 001: Reserved 010: Enabled at 0% of Boot/POR process delay control 011: Enabled at 25% of Boot/POR process delay control 100: Enabled at 50% of Boot/POR process delay control 101: Reserved 110: Reserved 111: Controlled by Buck3En [1:0] after 100% of Boot/POR process delay control
Buck3En	1:0	Buck3 enable configuration (effective only when Buck3Seq = 111)	00: Disabled: BK1OUT not actively discharged unless Hard-Reset/Shutdown/Off mode 01: Enabled 10: Controlled by MPC_ (See Buck3MPC_ bits) 11: Reserved

Buck3Cfg (0x35)

BIT	7	6	5	4	3	2	1	0
Field	Buck3EnblNTGR	Buck3PGOODena	Buck3Fast	Buck3PsvDsc	Buck3ActDsc	Buck3LowEMI	Buck3FETScale	Buck3EnLxSns
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3EnblNTGR	7	Buck3 integrator feedback disable	0: Integrator enabled 1: Integrator disabled–proportional control only
Buck3PGOODena	6	Buck3 PGOOD Comparator Control	0: PGOOD comparator disabled during voltage transition after startup 1: PGOOD comparator enabled during voltage transition after startup
Buck3Fast	5	Buck3 pretrigger mode setting	0: Normal, low quiescent current operation 1: Increased quiescent mode for fast load transient response. Quiescent current increased to 30μA.
Buck3PsvDsc	4	Buck3 Passive Discharge Control	0: Buck3 passively discharged only in Hard-Reset 1: Buck3 passively discharged in Hard-Reset or Enable Low.
Buck3ActDsc	3	Buck3 Active Discharge Control	0: Buck3 actively discharged only in Hard-Reset 1: Buck3 actively discharged in Hard-Reset or Enable Low
Buck3LowEMI	2	Buck3 Low EMI Mode	0: Normal operation 1: Slow rise/fall edges on BK3LX by 3x

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3FETScale	1	Buck3 Force FET Scaling Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck1ISet must be < 100mA (e.g., to mitigate noise at low frequencies).	0: FET scaling disabled 1: FET scaling enabled
Buck3EnLxSns	0	Buck3 LX Sense Control Selects the condition to turn-on frewheeling FET. Keep it to 0 for Buck3Vset ≤ 1.6V	0: Enter freewheeling mode after inductor current zero-crossing 1: Enter freewheeling mode on V_{LX} high detection after inductor current zero-crossing

Buck3Cfg1 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	–	Buck3DisLDO	Buck3MPCFast	Buck3FPWM	Buck3IAdptDis	–	–	–
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3DisLDO	6	LDO mode control	0: Enable low dropout mode with LDO at low buck ratios 1: Disable LDO mode at low buck ratios
Buck3MPCFast	5	Buck3 FAST mode by MPC4 control	0: Buck3 FAST mode control by MPC4 disabled 1: Buck3 FAST mode control by MPC4 enabled
Buck3FPWM	4	Buck3 forced PWM mode control	0: Normal operation 1: Forced PWM mode enabled
Buck3IAdptDis	3	Buck3 adaptive peak current mode control	0: Adaptive peak current mode enabled 1: Peak current fixed at value set in Buck3ISet

Buck3Iset (0x37)

BIT	7	6	5	4	3	2	1	0
Field	Buck3ISetLookUpDis	–	–	–	Buck3ISet[3:0]			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3ISetLookUpDis	7	Buck3 peak current set by lookup table disabled	0: Inductor current setting is set according to lookup table 1: Inductor current setting is set by Buck3ISet

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3ISet	3:0	Buck3 Inductor Peak Current Setting. Valid only if Buck3ISetLookUpDis is high. For the best efficiency, use between 150mA and 200mA. Linear scale, 25mA increments, settings below 75mA can be limited by the minimum t_{ON}	0000: 0mA 0001: 25mA 0010: 50mA 0011: 75mA 0100: 100mA 0101: 125mA 0110: 150mA 0111: 175mA 1000: 200mA 1001: 225mA 1010: 250mA 1011: 275mA 1100: 300mA 1101: 325mA 1110: 350mA 1111: 375mA

Buck3VSet (0x38)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3VSet[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3VSet	5:0	Buck3 Output Voltage Setting. 0.55V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.55V 000001 = 0.6V … 111111 = 3.7V

Buck3Ctr (0x39)

BIT	7	6	5	4	3	2	1	0
Field	Buck3MPC7	Buck3MPC6	Buck3MPC5	Buck3MPC4	Buck3MPC3	Buck3MPC2	Buck3MPC1	Buck3MPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3MPC7	7	Buck3 MPC7 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs	0: Buck3 not controlled by MPC7 1: Buck3 controlled by MPC7
Buck3MPC6	6	Buck3 MPC6 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs	0: Buck3 not controlled by MPC6 1: Buck3 controlled by MPC6

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3MPC5	5	Buck3 MPC5 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs	0: Buck3 not controlled by MPC5 1: Buck3 controlled by MPC5
Buck3MPC4	4	Buck3 MPC4 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs	0: Buck3 not controlled by MPC4 1: Buck3 controlled by MPC4
Buck3MPC3	3	Buck3 MPC3 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs	0: Buck3 not controlled by MPC3 1: Buck3 controlled by MPC3
Buck3MPC2	2	Buck3 MPC2 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs	0: Buck3 not controlled by MPC2 1: Buck3 controlled by MPC2
Buck3MPC1	1	Buck3 MPC1 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs	0: Buck3 not controlled by MPC1 1: Buck3 controlled by MPC1
Buck3MPC0	0	Buck3 MPC0 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs	0: Buck3 not controlled by MPC0 1: Buck3 controlled by MPC0

Buck3DvsCfg0 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	Buck3DvsCfg[4:0]				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3DvsCfg	4:0		00000: DVS modes disabled 00001: MPC0/MPC1 00010: MPC0/MPC2 00011: MPC0/MPC3 00100: MPC0/MPC4 00101: MPC0/MPC5 00110: MPC0/MPC6 00111: MPC0/MPC7 01000: MPC1/MPC2 01001: MPC1/MPC3 01010: MPC1/MPC4 01011: MPC1/MPC5 01100: MPC1/MPC6 01101: MPC1/MPC7 01110: MPC2/MPC3 01111: MPC2/MPC4 10000: MPC2/MPC5 10001: MPC2/MPC6 10010: MPC2/MPC7 10011: MPC3/MPC4 10100: MPC3/MPC5 10101: MPC3/MPC6 10110: MPC3/MPC7 10111: MPC4/MPC5 11000: MPC4/MPC6 11001: MPC4/MPC7 11010: MPC5/MPC6 11011: MPC5/MPC7 11100: MPC6/MPC7 11101: SPI Mode >11101: RESERVED

Buck3DvsCfg1 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DvsVlt0[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DvsVlt0	5:0	Buck3 alternate output voltage setting 0 (Controlling MPCs = 00) 0.55V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.55V 000001 = 0.6V … 111111 = 3.7V

Buck3DvsCfg2 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DvsVlt1[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DvsVlt1	5:0	Buck3 alternate output voltage setting 1 (Controlling MPCs = 01) 0.55V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.55V 000001 = 0.6V … 111111 = 3.7V

Buck3DvsCfg3 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DvsVlt2[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DvsVlt2	5:0	Buck3 alternate output voltage setting 2 (Controlling MPCs = 10) 0.55V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.55V 000001 = 0.6V … 111111 = 3.7V

Buck3DvsCfg4 (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DvsVlt3[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DvsVlt3	5:0	Buck3 alternate output voltage setting 3 (Controlling MPCs = 11) 0.55V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.55V 000001 = 0.6V … 111111 = 3.7V

Buck3DvsSpi (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3SPIVlt[5:0]					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
Buck3SPIVlt	5:0	Buck3 SPI DVS Readback. 0.55V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.55V 000001 = 0.6V … 111111 = 3.7V

BBstEna (0x40)

BIT	7	6	5	4	3	2	1	0
Field	BBstSeq[2:0]			–	–	–	BBstEn[1:0]	
Access Type	Read Only			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
BBstSeq	7:5	Buck-Boost enable configuration	000: Disabled 001: Reserved 010: Enabled at 0% of Boot/POR process delay control 011: Enabled at 25% of Boot/POR process delay control 100: Enabled at 50% of Boot/POR process delay control 101: Reserved 110: Reserved 111: Controlled by BBstEn[1:0] after 100% of Boot/POR process delay control
BBstEn	1:0	Buck-Boost enable configuration (effective only when BBstSeq = 111)	00: Disabled: BBOUT not actively discharged unless Hard-Reset/Shutdown/Off mode 01: Enabled 10: Controlled by MPC_ (See BBstMPC_ bits) 11: Reserved

BBstCfg (0x41)

BIT	7	6	5	4	3	2	1	0
Field	BBstISetLookUpDis	–	–	BBstLowEMI	BBstActDsc	BBstRampEn	BBstMode	BBstPsvDisc
Access Type	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBstISetLookUpDis	7	Buck-Boost peak current set by lookup table disable	0: Inductor current setting is set according to look-up table 1: Inductor current setting is set by BBstIPSet2 and BBstIPSet1
BBstLowEMI	4	Buck-Boost low EMI mode	0: Normal operation 1: Slow rise/fall edges on HVLX/LVLX by 3x
BBstActDsc	3	Buck-Boost active discharge control	0: Buck-Boost actively discharged only in Hard-Reset 1: Buck-Boost actively discharged in Hard-Reset or Enable Low
BBstRampEn	2	Buck-Boost ramp enable	0: Voltage setting transition is performed without intermediate steps 1: Voltage setting transition to a higher value is performed with incremental steps every 20µs
BBstMode	1	Buck-Boost operating mode	0: Buck-Boost 1: Buck Only
BBstPsvDisc	0	Buck-Boost passive discharge control	0: Buck-Boost passively discharged only in Hard-Reset 1: Buck-Boost passively discharged in Hard-Reset or Enable Low.

BBstVSet (0x42)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstVSet[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstVSet	5:0	Buck-Boost Output Voltage Setting. 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

BBstISet (0x43)

BIT	7	6	5	4	3	2	1	0
Field	BBstIPSet2[3:0]				BBstIPSet1[3:0]			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
BBstIPSet2	7:4	Buck-Boost nominal maximum peak current setting. Valid only if BBstISetLookUpDis is high. See Buck-Boost Regulator section for a description of the peak current settings. 0mA to 375mA, linear scale, 25mA increments, settings below 75mA can be limited by the minimum t_{ON}. Recommended settings: V_{BBOUT} ≤ 2.65V: 250mA 2.7V < V_{BBOUT} ≤ 3.05V: 225mA 3.1V < V_{BBOUT} ≤ 3.6V: 200mA 3.65V < V_{BBOUT} ≤ 4.35V: 175mA V_{BBOUT} > 4.4V: 150mA	0000: BBstIPSet1 + 0mA 0001: BBstIPSet1 + 25mA 0010: BBstIPSet1 + 50mA 0011: BBstIPSet1 + 75mA 0100: BBstIPSet1 + 100mA 0101: BBstIPSet1 + 125mA 0110: BBstIPSet1 + 150mA 0111: BBstIPSet1 + 175mA 1000: BBstIPSet1 + 200mA 1001: BBstIPSet1 + 225mA 1010: BBstIPSet1 + 250mA 1011: BBstIPSet1 + 275mA 1100: BBstIPSet1 + 300mA 1101: BBstIPSet1 + 325mA 1110: BBstIPSet1 + 350mA 1111: BBstIPSet1 + 375mA

BITFIELD	BITS	DESCRIPTION	DECODE
BBstIPSet1	3:0	Buck-Boost nominal peak current setting. Valid only if BBstISetLookUpDis is high. Nominal peak current when charging inductor between V_{IN} and GND. See Buck-Boost Regulator section for a description of the peak current settings. 0mA to 375mA, linear scale, 25mA increments, settings below 75mA may be limited by the minimum t_{ON} Recommended settings: V_{BBOUT} ≤ 2.65V: 50mA 2.7V < V_{BBOUT} ≤ 3.05V: 75mA 3.1V < V_{BBOUT} ≤ 3.4V: 100mA 3.45V < V_{BBOUT} ≤ 3.8V: 125mA 3.85V < V_{BBOUT} ≤ 4.15V: 150mA 4.2V < V_{BBOUT} ≤ 4.55V: 175mA 4.6V < V_{BBOUT} ≤ 4.9V: 200mA 4.95V < V_{BBOUT} ≤ 5.3V: 225mA V_{BBOUT} > 5.35V: 250mA	0000: 0mA 0001: 25mA 0010: 50mA 0011: 75mA 0100: 100mA 0101: 125mA 0110: 150mA 0111: 175mA 1000: 200mA 1001: 225mA 1010: 250mA 1011: 275mA 1100: 300mA 1101: 325mA 1110: 350mA 1111: 375mA

BBstCfg1 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	–	BBstIAdptDis	BBstFast	BBstZCCmpDis	BBstFETScale	BBstMPC1FastCntl	BBFHighSh[1:0]	
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
BBstIAdptDis	6	Adaptive peak/valley current adjustment enable	0: Enabled 1: Disabled, peak current fixed and is set by BBstIPSet1,2. Valley current is fixed to 0mA
BBstFast	5	Buck-Boost pretrigger mode setting	0: Normal, low quiescent current operation 1: Increased quiescent mode for fast load transient response. Quiescent current increased to 30µA.
BBstZCCmpDis	4	Buck-Boost zero-crossing comparator disable	0: Enable 1: Disable
BBstFETScale	3	Buck-Boost Force FET Scaling. Reduce the FET size by factor 2 to optimize the efficiency at light loads	0: FET scaling disabled 1: FET scaling enabled
BBstMPC1FastCntl	2	Buck-Boost FAST Mode Enable by MPC1. Improves interoperability with MAX86170/171. Tie MPC1 to INT2 on MAX86170/171 if this mode is used.	0: FAST status controlled by BBstFast Register 1: FAST mode controlled by MPC1. MPC1 = 0: FAST disabled MPC1 = 1: FAST enabled, IQ increased by 30µA
BBFHighSh	1:0	Buck-Boost f_{HIGH} Thresholds. Selects the switching frequency threshold f_{HIGH}. If f_{SW} > f_{HIGH} all the blocks are kept ON (I_Q is higher). A small glitch on V_{BBOUT} can be present at the f_{HIGH} crossoverover.	00: 25kHz/6.125kHz 01: 35kHz/8.25kHz 10: 50kHz/12.5kHz 11: 100kHz/25kHz

BBstCtr0 (0x45)

BIT	7	6	5	4	3	2	1	0
Field	BBstMPC7	BBstMPC6	BBstMPC5	BBstMPC4	BBstMPC3	BBstMPC2	BBstMPC1	BBstMPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBstMPC7	7	Buck-Boost MPC7 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the Buck-Boost is controlled by the logical OR of the MPCs	0: Buck-Boost not controlled by MPC7 1: Buck-Boost controlled by MPC7
BBstMPC6	6	Buck-Boost MPC6 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the Buck-Boost is controlled by the logical OR of the MPCs	0: Buck-Boost not controlled by MPC6 1: Buck-Boost controlled by MPC6
BBstMPC5	5	Buck-Boost MPC5 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the Buck-Boost is controlled by the logical OR of the MPCs	0: Buck-Boost not controlled by MPC5 1: Buck-Boost controlled by MPC5
BBstMPC4	4	Buck-Boost MPC4 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the Buck-Boost is controlled by the logical OR of the MPCs	0: Buck-Boost not controlled by MPC4 1: Buck-Boost controlled by MPC4
BBstMPC3	3	Buck-Boost MPC3 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the Buck-Boost is controlled by the logical OR of the MPCs	0: Buck-Boost not controlled by MPC3 1: Buck-Boost controlled by MPC3
BBstMPC2	2	Buck-Boost MPC2 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the Buck-Boost is controlled by the logical OR of the MPCs	0: Buck-Boost not controlled by MPC2 1: Buck-Boost controlled by MPC2
BBstMPC1	1	Buck-Boost MPC1 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the Buck-Boost is controlled by the logical OR of the MPCs	0: Buck-Boost not controlled by MPC1 1: Buck-Boost controlled by MPC1
BBstMPC0	0	Buck-Boost MPC0 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the Buck-Boost is controlled by the logical OR of the MPCs	0: Buck-Boost not controlled by MPC0 1: Buck-Boost controlled by MPC0

BBstCtr1 (0x46)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BBstDvsCfg[4:0]				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
BBstDvsCfg	4:0	Buck-Boost DVS configuration	00000: DVS modes disabled 00001: MPC0/MPC1 00010: MPC0/MPC2 00011: MPC0/MPC3 00100: MPC0/MPC4 00101: MPC0/MPC5 00110: MPC0/MPC6 00111: MPC0/MPC7 01000: MPC1/MPC2 01001: MPC1/MPC3 01010: MPC1/MPC4 01011: MPC1/MPC5 01100: MPC1/MPC6 01101: MPC1/MPC7 01110: MPC2/MPC3 01111: MPC2/MPC4 10000: MPC2/MPC5 10001: MPC2/MPC6 10010: MPC2/MPC7 10011: MPC3/MPC4 10100: MPC3/MPC5 10101: MPC3/MPC6 10110: MPC3/MPC7 10111: MPC4/MPC5 11000: MPC4/MPC6 11001: MPC4/MPC7 11010: MPC5/MPC6 11011: MPC5/MPC7 11100: MPC6/MPC7 11101: SPI Mode >11101: RESERVED

BBstDvsCfg0 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstDvsVlt0[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstDvsVlt0	5:0	Buck-Boost alternate output voltage setting 0 (Controlling MPCs = 00) 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

BBstDvsCfg1 (0x48)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstDvsVlt1[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstDvsVlt1	5:0	Buck-Boost alternate output voltage setting 1 (Controlling MPCs = 01) 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

BBstDvsCfg2 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstDvsVlt2[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstDvsVlt2	5:0	Buck-Boost alternate output voltage setting 2 (Controlling MPCs = 10) 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

BBstDvsCfg3 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstDvsVlt3[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstDvsVlt3	5:0	Buck-Boost alternate output voltage setting 3 (Controlling MPCs = 11) 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

BBstDvsSpi (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstSPIVlt[5:0]					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
BBstSPIVlt	5:0	Buck-Boost SPI DVS Readback. 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

LDO1Ena (0x51)

BIT	7	6	5	4	3	2	1	0
Field	LDO1Seq[2:0]			–	–	–	LDO1En[1:0]	
Access Type	Read Only			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LDO1Seq	7:5	LDO1 enable configuration (read only)	000: Disabled 001: Reserved 010: Enabled at 0% of Boot/POR process delay control 011: Enabled at 25% of Boot/POR process delay control 100: 100 = Enabled at 50% of Boot/POR process delay control 101: Reserved 110: Reserved 111: Controlled by LDO1En [1:0] after 100% of Boot/POR process delay control
LDO1En	1:0	LDO1 enable configuration (effective only when LDO1Seq = 111)	00: Disabled 01: Enabled 10: Controlled by MPC_ (See LDO1Ctr register 0x54) 11: Reserved

LDO1Cfg (0x52)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDO1_MPC0CNF	LDO1_MPC0CNT	LDO1ActDsc	LDO1Mode	LDO1PsvDsc
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO1_MPC0CNF	4	MPC0 configuration bit	0: MPC0 controls LDO/SW mode of LDO1 (MPC0 = 0 LDO mode, MPC0 = 1 SW mode) 1: MPC0 controls Enable of LDO1 (MPC0 = 0 disabled, MPC0 = 1 enabled in SW mode)
LDO1_MPC0CNT	3	LDO1/MPC0 control bit	0: MPC0 has no effect on the LDO 1: LDO1_MPC0CNF is valid and MPC0 function is enabled

BITFIELD	BITS	DESCRIPTION	DECODE
LDO1ActDsc	2	LDO1 active discharge control	0: LDO1 output is actively discharged only in Hard-Reset mode 1: LDO1 output is actively discharged in Hard-Reset mode and also when its Enable goes Low
LDO1Mode	1	LDO1 Mode Control. When FET is On, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled	0: Normal LDO operating mode 1: Load switch mode. FET is either fully On or Off depending on state of LDO1En.
LDO1PsvDsc	0	LDO1 passive discharge control	0: LDO1 output is discharged only entering Off and Hard-Reset modes 1: LDO1 output is discharged only entering Off and Hard-Reset modes and when the enable is Low

LDO1VSet (0x53)

BIT	7	6	5	4	3	2	1	0
Field	–	–	LDO1VSet[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
LDO1VSet	5:0	LDO1 Output Voltage Setting. Limited by input supply 0.5V to 1.95V, Linear Scale, 25mV increments 000000 = 0.5V 000001 = 0.525V … 111010 = 1.95V >111010 = Limited by input supply

LDO1Ctr (0x54)

BIT	7	6	5	4	3	2	1	0
Field	LDO1MPC7	LDO1MPC6	LDO1MPC5	LDO1MPC4	LDO1MPC3	LDO1MPC2	LDO1MPC1	LDO1MPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO1MPC7	7	LDO1 MPC7 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs	0: LDO1 not controlled by MPC7 1: LDO1 controlled by MPC7
LDO1MPC6	6	LDO1 MPC6 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs	0: LDO1 not controlled by MPC6 1: LDO1 controlled by MPC6
LDO1MPC5	5	LDO1 MPC5 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs	0: LDO1 not controlled by MPC5 1: LDO1 controlled by MPC5

BITFIELD	BITS	DESCRIPTION	DECODE
LDO1MPC4	4	LDO1 MPC4 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs	0: LDO1 not controlled by MPC4 1: LDO1 controlled by MPC4
LDO1MPC3	3	LDO1 MPC3 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs	0: LDO1 not controlled by MPC3 1: LDO1 controlled by MPC3
LDO1MPC2	2	LDO1 MPC2 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs	0: LDO1 not controlled by MPC2 1: LDO1 controlled by MPC2
LDO1MPC1	1	LDO1 MPC1 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs	0: LDO1 not controlled by MPC1 1: LDO1 controlled by MPC1
LDO1MPC0	0	LDO1 MPC0 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs	0: LDO1 not controlled by MPC0 1: LDO1 controlled by MPC0

LDO2Ena (0x55)

BIT	7	6	5	4	3	2	1	0
Field	LDO2Seq[2:0]			–	–	–	LDO2En[1:0]	
Access Type	Read Only			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LDO2Seq	7:5	LDO2 Enable Configuration (Read only)	000: 000 = Disabled 001: Enabled always when BAT/SYS is present 010: Enabled at 0% of Boot/POR process delay control 011: Enabled at 25% of Boot/POR process delay control 100: Enabled at 50% of Boot/POR process delay control 101: Reserved 110: Reserved 111: Controlled by LDO2En [1:0] after 100% of Boot/POR process delay control
LDO2En	1:0	LDO2 Enable Configuration (effective only when LDO2Seq = 111)	00: Disabled 01: Enabled 10: Controlled by MPC_ (See LDO2Ctr register 0x58) 11: Reserved

LDO2Cfg (0x56)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LDO2Supply	LDO2ActDsc	LDO2Mode	LDO2PsvDsc
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO2Supply	3	AON LDO internal switchover supply control	0: L2IN must be provided externally 1: L2IN is internally connected to V_{CCINT} with a TYP 15kΩ resistor. Bypass L2IN with 1µF
LDO2ActDsc	2	LDO2 active discharge control	0: LDO2 output is actively discharged only in Hard-Reset mode 1: LDO2 output is actively discharged in Hard-Reset mode and also when its Enable goes Low
LDO2Mode	1	LDO2 Mode Control. When FET is On, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.	0: LDO2 output is actively discharged only in Hard-Reset mode 1: LDO2 output is actively discharged in Hard-Reset mode and also when its Enable goes Low
LDO2PsvDsc	0	LDO2 passive discharge control	0: LDO2 output is passively discharged only in Hard-Reset mode 1: LDO2 output is passively discharged in Hard-Reset mode and also when its Enable goes Low

LDO2VSet (0x57)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDO2VSet[4:0]				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
LDO2VSet	4:0	LDO2 Output Voltage Setting. Limited by input supply. 0.9V to 4V, Linear Scale, 100mV increments 000000 = 0.9V 000001 = 1V … 11110 = 3.9V 11111 = 4V

LDO2Ctr (0x58)

BIT	7	6	5	4	3	2	1	0
Field	LDO2MPC7	LDO2MPC6	LDO2MPC5	LDO2MPC4	LDO2MPC3	LDO2MPC2	LDO2MPC1	LDO2MPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO2MPC7	7	LDO2 MPC7 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs	0: LDO2 not controlled by MPC7 1: LDO2 controlled by MPC7
LDO2MPC6	6	LDO2 MPC6 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs	0: LDO2 not controlled by MPC6 1: LDO2 controlled by MPC6
LDO2MPC5	5	LDO2 MPC5 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs	0: LDO2 not controlled by MPC5 1: LDO2 controlled by MPC5
LDO2MPC4	4	LDO2 MPC4 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs	0: LDO2 not controlled by MPC4 1: LDO2 controlled by MPC4
LDO2MPC3	3	LDO2 MPC3 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs	0: LDO2 not controlled by MPC3 1: LDO2 controlled by MPC3
LDO2MPC2	2	LDO2 MPC2 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs	0: LDO2 not controlled by MPC2 1: LDO2 controlled by MPC2
LDO2MPC1	1	LDO2 MPC1 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs	0: LDO2 not controlled by MPC1 1: LDO2 controlled by MPC1
LDO2MPC0	0	LDO2 MPC0 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs	0: LDO2 not controlled by MPC0 1: LDO2 controlled by MPC0

LSW1Ena (0x59)

BIT	7	6	5	4	3	2	1	0
Field	LSW1Seq[2:0]			–	–	–	LSW1En[1:0]	
Access Type	Read Only			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LSW1Seq	7:5	LSW1 enable configuration (read only)	000: Disabled 001: Reserved 010: Enabled at 0% of Boot/POR process delay control 011: Enabled at 25% of Boot/POR process delay control 100: Enabled at 50% of Boot/POR process delay control 101: Reserved 110: Reserved 111: Controlled by LSW1En [1:0] after 100% of Boot/POR process delay control
LSW1En	1:0	LSW1 enable configuration (effective only when LSW1Seq = 111)	00: Disabled 01: Enabled 10: Controlled by MPC_ (See LSW1MPC_ bits in register 0x5B) 11: Reserved

LSW1Cfg (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LSW1ActDsc	LSW1LowIq	LSW1PsvDsc
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW1ActDsc	2	LSW1 active discharge control	0: LSW1 output is actively discharged only in Hard-Reset mode 1: LSW1 output is actively discharged in Hard-Reset mode and also when its Enable goes Low
LSW1LowIq	1	LSW1 Low Quiescent Control. Low quiescent mode is achieved by disabling the voltage protection of LSW1	0: Voltage protection enabled. If V_{SYS} - $V_{LSW1OUT}$ exceeds V_{LSW_PROT}, the output is disabled to protect from overcurrent. 1: Voltage protection disabled and quiescent is reduced
LSW1PsvDsc	0	LSW1 passive discharge control	0: LSW1 output is discharged only entering Off and Hard-Reset modes 1: LSW1 output is discharged only entering Off and Hard-Reset modes and when the enable is Low

LSW1Ctr (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	LSW1MPC7	LSW1MPC6	LSW1MPC5	LSW1MPC4	LSW1MPC3	LSW1MPC2	LSW1MPC1	LSW1MPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW1MPC7	7	LSW1 MPC7 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs	0: LSW1 not controlled by MPC7 1: LSW1 controlled by MPC7

BITFIELD	BITS	DESCRIPTION	DECODE
LSW1MPC6	6	LSW1 MPC6 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs	0: LSW1 not controlled by MPC6 1: LSW1 controlled by MPC6
LSW1MPC5	5	LSW1 MPC5 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs	0: LSW1 not controlled by MPC5 1: LSW1 controlled by MPC5
LSW1MPC4	4	LSW1 MPC4 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs	0: LSW1 not controlled by MPC4 1: LSW1 controlled by MPC4
LSW1MPC3	3	LSW1 MPC3 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs	0: LSW1 not controlled by MPC3 1: LSW1 controlled by MPC3
LSW1MPC2	2	LSW1 MPC2 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs	0: LSW1 not controlled by MPC2 1: LSW1 controlled by MPC2
LSW1MPC1	1	LSW1 MPC1 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs	0: LSW1 not controlled by MPC1 1: LSW1 controlled by MPC1
LSW1MPC0	0	LSW1 MPC0 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs	0: LSW1 not controlled by MPC0 1: LSW1 controlled by MPC0

LSW2Ena (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	LSW2Seq[2:0]			–	–	–	LSW2En[1:0]	
Access Type	Read Only			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LSW2Seq	7:5	LSW2 enable configuration (read only)	000: Disabled 001: Reserved 010: Enabled at 0% of Boot/POR process delay control 011: Enabled at 25% of Boot/POR process delay control 100: Enabled at 50% of Boot/POR process delay control 101: Reserved 110: Reserved 111: Controlled by LSW2En [1:0] after 100% of Boot/POR process delay control
LSW2En	1:0	LSW2 enable configuration (effective only when LSW2Seq = 111)	00: Disabled 01: Enabled 10: Controlled by MPC_ (See LSW2MPC_ bits in register 0x5E) 11: Reserved

LSW2Cfg (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LSW2ActDsc	LSW2LowIq	LSW2PsvDsc
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW2ActDsc	2	LSW2 active discharge control	0: LSW2 output is actively discharged only in Hard-Reset mode 1: LSW2 output is actively discharged in Hard-Reset mode and also when its Enable goes Low
LSW2LowIq	1	LSW2 Low Quiescent Control. Low quiescent mode is achieved by disabling the voltage protection of LSW2	0: Voltage protection enabled. If V_{SYS} - $V_{LSW2OUT}$ exceeds V_{LSW_PROT}, the output is disabled to protect from overcurrent. 1: Voltage protection disabled and quiescent is reduced
LSW2PsvDsc	0	LSW2 passive discharge control	0: LSW2 output is discharged only entering Off and Hard-Reset modes 1: LSW2 output is discharged only entering Off and Hard-Reset modes and when the enable is Low

LSW2Ctr (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	LSW2MPC7	LSW2MPC6	LSW2MPC5	LSW2MPC4	LSW2MPC3	LSW2MPC2	LSW2MPC1	LSW2MPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW2MPC7	7	LSW2 MPC7 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs	0: LSW2 not controlled by MPC7 1: LSW2 controlled by MPC7

BITFIELD	BITS	DESCRIPTION	DECODE
LSW2MPC6	6	LSW2 MPC6 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs	0: LSW2 not controlled by MPC6 1: LSW2 controlled by MPC6
LSW2MPC5	5	LSW2 MPC5 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs	0: LSW2 not controlled by MPC5 1: LSW2 controlled by MPC5
LSW2MPC4	4	LSW2 MPC4 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs	0: LSW2 not controlled by MPC4 1: LSW2 controlled by MPC4
LSW2MPC3	3	LSW2 MPC3 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs	0: LSW2 not controlled by MPC3 1: LSW2 controlled by MPC3
LSW2MPC2	2	LSW2 MPC2 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs	0: LSW2 not controlled by MPC2 1: LSW2 controlled by MPC2
LSW2MPC1	1	LSW2 MPC1 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs	0: LSW2 not controlled by MPC1 1: LSW2 controlled by MPC1
LSW2MPC0	0	LSW2 MPC0 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs	0: LSW2 not controlled by MPC0 1: LSW2 controlled by MPC0

ChgPmpEna (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	ChgPmpSeq[2:0]			–	–	–	ChgPmpEn[1:0]	
Access Type	Read Only			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ChgPmpSeq	7:5	Charge pump enable configuration (read only)	000: Disabled 001: Reserved 010: Enabled at 0% of Boot/POR process delay control 011: Enabled at 25% of Boot/POR process delay control 100: Enabled at 50% of Boot/POR process delay control 101: Reserved 110: Reserved 111: Controlled by ChgPmpEn [1:0] after 100% of Boot/POR process delay control
ChgPmpEn	1:0	Charge pump enable configuration (effective only when ChgPmpSeq = 111)	00: Disabled 01: Enabled 10: Controlled by MPC_ (See ChgPmpMPC_ bits in register 0x61) 11: Reserved

ChgPmpCfg (0x60)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	CPVSet	ChgPmpPsv
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CPVSet	1	Charge pump voltage control	0: 6.6V 1: 5V
ChgPmpPsv	0	Charge pump passive discharge control	0: Charge pump passively discharged only in Hard-Reset 1: Charge pump passively discharged in Hard-Reset or Enable Low.

ChgPmpCtr (0x61)

BIT	7	6	5	4	3	2	1	0
Field	CHGPMPMPC7	CHGPMPMPC6	CHGPMPMPC5	CHGPMPMPC4	CHGPMPMPC3	CHGPMPMPC2	CHGPMPMPC1	CHGPMPMPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CHGPMPMPC7	7	Charge Pump MPC7 Enable Control. Only valid when ChgPmpSeq = 111 and ChgPmpEn = 10. If multiple MPCs are selected, ChgPmp is controlled by the logical OR of the MPCs	0: Charge pump not controlled by MPC7 1: Charge pump controlled by MPC7
CHGPMPMPC6	6	Charge Pump MPC6 Enable Control. Only valid when ChgPmpSeq = 111 and ChgPmpEn = 10. If multiple MPCs are selected, ChgPmp is controlled by the logical OR of the MPCs	0: Charge pump not controlled by MPC6 1: Charge pump controlled by MPC6

BITFIELD	BITS	DESCRIPTION	DECODE
CHGPMPMP C5	5	Charge Pump MPC5 Enable Control. Only valid when ChgPmpSeq = 111 and ChgPmpEn = 10. If multiple MPCs are selected, ChgPmp is controlled by the logical OR of the MPCs	0: Charge pump not controlled by MPC5 1: Charge pump controlled by MPC5
CHGPMPMP C4	4	Charge Pump MPC4 Enable Control. Only valid when ChgPmpSeq = 111 and ChgPmpEn = 10. If multiple MPCs are selected, ChgPmp is controlled by the logical OR of the MPCs	0: Charge pump not controlled by MPC4 1: Charge pump controlled by MPC4
CHGPMPMP C3	3	Charge Pump MPC3 Enable Control. Only valid when ChgPmpSeq = 111 and ChgPmpEn = 10. If multiple MPCs are selected, ChgPmp is controlled by the logical OR of the MPCs	0: Charge pump not controlled by MPC3 1: Charge pump controlled by MPC3
CHGPMPMP C2	2	Charge Pump MPC2 Enable Control. Only valid when ChgPmpSeq = 111 and ChgPmpEn = 10. If multiple MPCs are selected, ChgPmp is controlled by the logical OR of the MPCs	0: Charge pump not controlled by MPC2 1: Charge pump not controlled by MPC2
CHGPMPMP C1	1	Charge Pump MPC1 Enable Control. Only valid when ChgPmpSeq = 111 and ChgPmpEn = 10. If multiple MPCs are selected, ChgPmp is controlled by the logical OR of the MPCs	0: Charge pump not controlled by MPC1 1: Charge pump controlled by MPC1
CHGPMPMP C0	0	Charge Pump MPC0 Enable Control. Only valid when ChgPmpSeq = 111 and ChgPmpEn = 10. If multiple MPCs are selected, ChgPmp is controlled by the logical OR of the MPCs	0: Charge pump not controlled by MPC0 1: Charge pump controlled by MPC0

BoostEna (0x62)

BIT	7	6	5	4	3	2	1	0
Field	BoostSeq[2:0]			–	–	–	BstEn[1:0]	
Access Type	Read Only			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
BoostSeq	7:5	Boost enable configuration (read only)	000: Disabled 001: Reserved 010: Enabled at 0% of Boot/POR process delay control 011: Enabled at 25% of Boot/POR process delay control 100: Enabled at 50% of Boot/POR process delay control 101: Reserved 110: Reserved 111: Controlled by BoostEn [1:0] after 100% of Boot/POR process delay control

BITFIELD	BITS	DESCRIPTION	DECODE
BstEn	1:0	Boost enable configuration (effective only when BoostSeq = 111)	00: Disabled 01: Enabled 10: Controlled by MPC_ (See BoostMPC_ bits in register 0x66) 11: Reserved

BoostCfg (0x63)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BstPsvDsc	BstIAdptEn	BstFastStrt	BstFETScal e
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BstPsvDsc	3	Boost passive discharge control	0: Boost output is discharged only when entering Off and Hard-Reset modes 1: Boost output is discharged only when entering Off and Hard-Reset modes and when BoostEn is set to 000
BstIAdptEn	2	Boost adaptive peak current control	0: Inductor peak current fixed at the programmed value by means of BstISet 1: Inductor peak current automatically increased to provide better load regulation
BstFastStrt	1	Boost fast start time	0: Time to full current capability during Startup =100ms. Precharge with fixed BstISet = 100mA 1: Time to full current capability during Startup = 50ms.
BstFETScale	0	Boost FET scaling	0: No FET scaling 1: Active boost FET size scaled down by half to optimize efficiency for low inductor peak current settings

BoostISet (0x64)

BIT	7	6	5	4	3	2	1	0
Field	BstISetLook UpDis	–	–	–	BstISet[3:0]			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
BstISetLook UpDis	7	Boost peak current set by lookup table disable	0: Inductor current setting is set according to look-up table 1: Inductor current setting is set by BstISet

BITFIELD	BITS	DESCRIPTION	DECODE
BstISet	3:0	Boost Nominal inductor Peak Current Setting. Valid only if BstISetLookUpDis is high. 25mA step resolution	0000: 100mA 0001: 125mA 0010: 150mA 0011: 175mA 0100: 200mA 0101: 225mA 0110: 250mA 0111: 275mA 1000: 300mA 1001: 325mA 1010: 350mA 1011: 375mA 1100: 400mA 1101: 425mA 1110: 450mA 1111: 475mA

BoostVSet (0x65)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BstVSet[5:0]					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BstVSet	5:0	Boost Output Voltage Setting. Linear scale from 5V to 20V in 250mV increments	000000: 5.00V 000001: 5.25V 000010: 5.50V 000011: 5.75V 000100: 6.00V 000101: 6.25V 000110: 6.50V 000111: 6.75V 001000: 7.00V 001001: 7.25V 001010: 7.50V 001011: 7.75V 001100: 8.00V 001101: 8.25V 001110: 8.50V 001111: 8.75V 010000: 9.00V 010001: 9.25V 010010: 9.50V 010011: 9.75V 010100: 10.00V 010101: 10.25V 010110: 10.50V 010111: 10.75V 011000: 11.00V 011001: 11.25V 011010: 11.50V 011011: 11.75V 011100: 12.00V 011101: 12.25V 011110: 12.50V 011111: 12.75V 100000: 13.00V 100001: 13.25V 100010: 13.50V 100011: 13.75V 100100: 14.00V 100101: 14.25V 100110: 14.50V 100111: 14.75V 101000: 15.00V 101001: 15.25V 101010: 15.50V 101011: 15.75V 101100: 16.00V 101101: 16.25V 101110: 16.50V 101111: 16.75V 110000: 17.00V 110001: 17.25V 110010: 17.50V 110011: 17.75V 110100: 18.00V 110101: 18.25V 110110: 18.50V 110111: 18.75V 111000: 19.00V

BITFIELD	BITS	DESCRIPTION	DECODE
			111001: 19.25V 111010: 19.50V 111011: 19.75V 111100: 20.00V >111100: Reserved

BoostCtr (0x66)

BIT	7	6	5	4	3	2	1	0
Field	BstMPC7	BstMPC6	BstMPC5	BstMPC4	BstMPC3	BstMPC2	BstMPC1	BstMPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BstMPC7	7	Boost MPC7 Enable Control. Only valid when BstSeq = 111 and BstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs	0: Boost not controlled by MPC7 1: Boost controlled by MPC7
BstMPC6	6	Boost MPC6 Enable Control. Only valid when BstSeq = 111 and BstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs	0: Boost not controlled by MPC6 1: Boost controlled by MPC6
BstMPC5	5	Boost MPC5 Enable Control. Only valid when BstSeq = 111 and BstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs	0: Boost not controlled by MPC5 1: Boost controlled by MPC5
BstMPC4	4	Boost MPC4 Enable Control. Only valid when BstSeq = 111 and BstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs	0: Boost not controlled by MPC4 1: Boost controlled by MPC4
BstMPC3	3	Boost MPC3 Enable Control. Only valid when BstSeq = 111 and BstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs	0: Boost not controlled by MPC3 1: Boost controlled by MPC3
BstMPC2	2	Boost MPC2 Enable Control. Only valid when BstSeq = 111 and BstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs	0: Boost not controlled by MPC2 1: Boost controlled by MPC2
BstMPC1	1	Boost MPC1 Enable Control. Only valid when BstSeq = 111 and BstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs	0: Boost not controlled by MPC1 1: Boost controlled by MPC1

BITFIELD	BITS	DESCRIPTION	DECODE
BstMPC0	0	Boost MPC0 Enable Control. Only valid when BstSeq = 111 and BstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs	0: Boost not controlled by MPC0 1: Boost controlled by MPC0

MPC0Cfg (0x67)

BIT	7	6	5	4	3	2	1	0
Field	MPC0Read	–	–	MPC0Out	MPC0OD	MPC0HiZB	MPC0Res	MPC0Pup
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC0Read	7	MPC0 State	0: MPC0 Low 1: MPC0 High (if MPC0OD = 0) or Hi-Z (if MPC0OD = 1)
MPC0Out	4	MPC0 Output Value. Valid only if MPC0 is configured as output (MPC0HiZB = 1)	0: MPC0 connected to GND 1: MPC0 open drain off (MPC0OD = 1) or connected to BK1OUT (MPC0OD = 0)
MPC0OD	3	MPC0 Output Configuration. Valid only if MPC0 is configured as output (MPC0HiZB = 1)	0: MPC0 is push-pull connected to BK1OUT 1: MPC0 is open drain
MPC0HiZB	2	MPC0 Direction	0: MPC0 is Hi-Z. Input buffer enabled. 1: MPC0 is not Hi-Z. Output buffer enabled.
MPC0Res	1	MPC0 Resistor Presence. Valid only if MPC0 is configured as input (MPC0HiZB = 0)	0: Resistor not connected to MPC0 1: Resistor connected to MPC0
MPC0Pup	0	MPC0 Resistor Configuration. Valid only if there is a resistor on MPC0 (MPC0Res = 1)	0: Pulldown connected to MPC0 1: Pullup to V_{CCINT} connected MCP0

MPC1Cfg (0x68)

BIT	7	6	5	4	3	2	1	0
Field	MPC1Read	–	–	MPC1Out	MPC1OD	MPC1HiZB	MPC1Res	MPC1Pup
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC1Read	7	MPC1 State	0: MPC1 Low 1: MPC1 High (if MPC1OD = 0) or Hi-Z (if MPC1OD = 1)
MPC1Out	4	MPC1 Output Value. Valid only if MPC1 is configured as output (MPC1HiZB = 1)	0: MPC1 connected to GND 1: MPC1 open drain off (MPC1OD = 1) or connected to BK1OUT (MPC1OD = 0)
MPC1OD	3	MPC1 OOutput Configuration. Valid only if MPC1 is configured as output (MPC1HiZB = 1)	0: MPC1 is push-pull connected to BK1OUT 1: MPC1 is open drain

BITFIELD	BITS	DESCRIPTION	DECODE
MPC1HiZB	2	MPC1 Direction	0: MPC1 is Hi-Z. Input buffer enabled. 1: MPC1 is not Hi-Z. Output buffer enabled.
MPC1Res	1	MPC1 Resistor Presence. Valid only if MPC1 is configured as input (MPC1HiZB = 0)	0: Resistor not connected to MPC1 1: Resistor connected to MPC1
MPC1Pup	0	MPC1 Resistor Configuration. Valid only if there is a resistor on MPC1 (MPC1Res = 1)	0: Pulldown connected to MPC1 1: Pullup to V_{CCINT} connected MCP1

MPC2Cfg (0x69)

BIT	7	6	5	4	3	2	1	0
Field	MPC2Read	–	–	MPC2Out	MPC2OD	MPC2HiZB	MPC2Res	MPC2Pup
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC2Read	7	MPC2 State	0: MPC2 Low 1: MPC2 High (if MPC2OD = 0) or Hi-Z (if MPC2OD = 1)
MPC2Out	4	MPC2 Output Value. Valid only if MPC2 is configured as output (MPC2HiZB = 1)	0: MPC2 connected to GND 1: MPC2 open drain off (MPC2OD = 1) or connected to BK1OUT (MPC2OD = 0)
MPC2OD	3	MPC2 Output Configuration. Valid only if MPC2 is configured as output (MPC2HiZB = 1)	0: MPC2 is push-pull connected to BK1OUT 1: MPC2 is open drain
MPC2HiZB	2	MPC2 Direction	0: MPC2 is Hi-Z. Input buffer enabled. 1: MPC2 is not Hi-Z. Output buffer enabled.
MPC2Res	1	MPC2 Resistor Presence. Valid only if MPC2 is configured as input (MPC2HiZB = 0)	0: Resistor not connected to MPC2 1: Resistor connected to MPC2
MPC2Pup	0	MPC2 Resistor Configuration. Valid only if there is a resistor on MPC2 (MPC2Res = 1)	0: Pulldown connected to MPC2 1: Pullup to V_{CCINT} connected MCP2

MPC3Cfg (0x6A)

BIT	7	6	5	4	3	2	1	0
Field	MPC3Read	–	–	MPC3Out	MPC3OD	MPC3HiZB	MPC3Res	MPC3Pup
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC3Read	7	MPC3 State	0: MPC3 Low 1: MPC3 High (if MPC3OD = 0) or Hi-Z (if MPC3OD = 1)
MPC3Out	4	MPC3 Output Value. Valid only if MPC3 is configured as output (MPC3HiZB = 1)	0: MPC3 connected to GND 1: MPC3 open drain off (MPC3OD = 1) or connected to BK1OUT (MPC3OD = 0)

BITFIELD	BITS	DESCRIPTION	DECODE
MPC3OD	3	MPC3 Output Configuration. Valid only if MPC3 is configured as output (MPC3HiZB = 1)	0: MPC3 is push-pull connected to BK1OUT 1: MPC3 is open drain
MPC3HiZB	2	MPC3 Direction	0: MPC3 is Hi-Z. Input buffer enabled. 1: MPC3 is not Hi-Z. Output buffer enabled.
MPC3Res	1	MPC3 Resistor Presence. Valid only if MPC3 is configured as input (MPC3HiZB = 0)	0: Resistor not connected to MPC3 1: Resistor connected to MPC3
MPC3Pup	0	MPC3 Resistor Configuration. Valid only if there is a resistor on MPC3 (MPC3Res = 1)	0: Pulldown connected to MPC3 1: Pullup to V_{CCINT} connected MCP3

MPC4Cfg (0x6B)

BIT	7	6	5	4	3	2	1	0
Field	MPC4Read	–	–	MPC4Out	MPC4OD	MPC4HiZB	MPC4Res	MPC4Pup
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC4Read	7	MPC4 State	0: MPC4 Low 1: MPC4 High (if MPC4OD = 0) or Hi-Z (if MPC4OD = 1)
MPC4Out	4	MPC4 Output Value. Valid only if MPC4 is configured as output (MPC4HiZB = 1)	0: MPC4 connected to GND 1: MPC4 open drain off (MPC4OD = 1) or connected to BK1OUT (MPC4OD = 0)
MPC4OD	3	MPC4 Output Configuration. Valid only if MPC4 is configured as output (MPC4HiZB = 1)	0: MPC4 is push-pull connected to BK1OUT 1: MPC4 is open drain
MPC4HiZB	2	MPC4 Direction	0: MPC4 is Hi-Z. Input buffer enabled. 1: MPC4 is not Hi-Z. Output buffer enabled.
MPC4Res	1	MPC4 Resistor Presence. Valid only if MPC4 is configured as input (MPC4HiZB = 0)	0: Resistor not connected to MPC4 1: Resistor connected to MPC4
MPC4Pup	0	MPC4 Resistor Configuration. Valid only if there is a resistor on MPC4 (MPC4Res = 1)	0: Pulldown connected to MPC4 1: Pullup to V_{CCINT} connected MCP4

MPC5Cfg (0x6C)

BIT	7	6	5	4	3	2	1	0
Field	MPC5Read	–	–	MPC5Out	MPC5OD	MPC5HiZB	MPC5Res	MPC5Pup
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC5Read	7	MPC5 State	0: MPC5 Low 1: MPC5 High (if MPC5OD = 0) or Hi-Z (if MPC5OD = 1)

BITFIELD	BITS	DESCRIPTION	DECODE
MPC5Out	4	MPC5 Output Value. Valid only if MPC5 is configured as output (MPC5HiZB = 1)	0: MPC5 connected to GND 1: MPC5 open drain off (MPC5OD = 1) or connected to BK1OUT (MPC5OD = 0)
MPC5OD	3	MPC5 Output Configuration. Valid only if MPC5 is configured as output (MPC5HiZB = 1)	0: MPC5 is push-pull connected to BK1OUT 1: MPC5 is open drain
MPC5HiZB	2	MPC5 Direction	0: MPC5 is Hi-Z. Input buffer enabled. 1: MPC5 is not Hi-Z. Output buffer enabled.
MPC5Res	1	MPC5 Resistor Presence. Valid only if MPC5 is configured as input (MPC5HiZB = 0)	0: Resistor not connected to MPC5 1: Resistor connected to MPC5
MPC5Pup	0	MPC5 Resistor Configuration Valid only if there is a resistor on MPC5 (MPC5Res = 1)	0: Pulldown connected to MPC5 1: Pullup to V_{CCINT} connected MCP5

MPC6Cfg (0x6D)

BIT	7	6	5	4	3	2	1	0
Field	MPC6Read	–	–	MPC6Out	MPC6OD	MPC6HiZB	MPC6Res	MPC6Pup
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC6Read	7	MPC6 State	0: MPC6 Low 1: MPC6 High (if MPC6OD = 0) or Hi-Z (if MPC6OD = 1)
MPC6Out	4	MPC6 Output Value. Valid only if MPC6 is configured as output (MPC6HiZB = 1)	0: MPC6 connected to GND 1: MPC6 open drain off (MPC6OD = 1) or connected to BK1OUT (MPC6OD = 0)
MPC6OD	3	MPC6 Output Configuration. Valid only if MPC6 is configured as output (MPC6HiZB = 1)	0: MPC6 is push-pull connected to BK1OUT 1: MPC6 is open drain
MPC6HiZB	2	MPC6 Direction	0: MPC6 is Hi-Z. Input buffer enabled. 1: MPC6 is not Hi-Z. Output buffer enabled.
MPC6Res	1	MPC6 Resistor Presence. Valid only if MPC6 is configured as input (MPC6HiZB = 0)	0: Resistor not connected to MPC6 1: Resistor connected to MPC6
MPC6Pup	0	MPC6 Resistor Configuration. Valid only if there is a resistor on MPC6 (MPC6Res = 1)	0: Pulldown connected to MPC6 1: Pullup to V_{CCINT} connected MCP6

MPC7Cfg (0x6E)

BIT	7	6	5	4	3	2	1	0
Field	MPC7Read	–	–	MPC7Out	MPC7OD	MPC7HiZB	MPC7Res	MPC7Pup
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC7Read	7	MPC7 State	0: MPC7 Low 1: MPC7 High (if MPC7OD = 0) or Hi-Z (if MPC7OD = 1)
MPC7Out	4	MPC7 Output Value. Valid only if MPC7 is configured as output (MPC7HiZB = 1)	0: MPC7 connected to GND 1: MPC7 open drain off (MPC7OD = 1) or connected to BK1OUT (MPC7OD = 0)
MPC7OD	3	MPC7 Output Configuration. Valid only if MPC7 is configured as output (MPC7HiZB = 1)	0: MPC7 is push-pull connected to BK1OUT 1: MPC7 is open drain
MPC7HiZB	2	MPC7 Direction	0: MPC7 is Hi-Z. Input buffer enabled. 1: MPC7 is not Hi-Z. Output buffer enabled.
MPC7Res	1	MPC7 Resistor Presence. Valid only if MPC7 is configured as input (MPC7HiZB = 0)	0: Resistor not connected to MPC7 1: Resistor connected to MPC7
MPC7Pup	0	MPC7 Resistor Configuration. Valid only if there is a resistor on MPC7 (MPC7Res = 1)	0: Pulldown connected to MPC7 1: Pullup to V_{CCINT} connected MCP7

MPCItrSts (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	USBOkMPCSts	–	–	BK3PgMPCSts	BK2PgMPCSts	BK1PgMPCSts
Access Type	–	–	Read Only	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
USBOkMPCSts	5	USBOk dedicated MPC interrupt status bit	0: USBOk MPC power good interrupt not active 1: USBOk MPC power good interrupt active
BK3PgMPCSts	2	Buck3 dedicated MPC interrupt status bit	0: Buck3 MPC power good interrupt not active 1: Buck3 MPC power good interrupt active
BK2PgMPCSts	1	Buck2 dedicated MPC interrupt status bit	0: Buck2 MPC power good interrupt not active 1: Buck2 MPC power good interrupt active
BK1PgMPCSts	0	Buck1 dedicated MPC interrupt status bit	0: Buck1 MPC power good interrupt not active 1: Buck1 MPC power good interrupt active

BK1DedIntCfg (0x70)

BIT	7	6	5	4	3	2	1	0
Field	BK1PGMPCInt	BK1MPC6Sel	BK1MPC5Sel	BK1MPC4Sel	BK1MPC3Sel	BK1MPC2Sel	BK1MPC1Sel	BK1MPC0Sel
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BK1PGMPCInt	7	Buck1 dedicated power-good interrupt	0: No power-good status change 1: Buck1 power-good status change caused interrupt
BK1MPC6Sel	6	Buck1 PGOOD Interrupt MPC6 assignment control	0: Buck1 PGOOD Interrupt not routed to MPC6 1: Buck1 PGOOD Interrupt routed to MPC6

BITFIELD	BITS	DESCRIPTION	DECODE
BK1MPC5Sel	5	Buck1 PGOOD Interrupt MPC5 assignment control	0: Buck1 PGOOD Interrupt not routed to MPC5 1: Buck1 PGOOD Interrupt routed to MPC5
BK1MPC4Sel	4	Buck1 PGOOD Interrupt MPC4 assignment control	0: Buck1 PGOOD Interrupt not routed to MPC4 1: Buck1 PGOOD Interrupt routed to MPC4
BK1MPC3Sel	3	Buck1 PGOOD Interrupt MPC3 assignment control	0: Buck1 PGOOD Interrupt not routed to MPC3 1: Buck1 PGOOD Interrupt routed to MPC3
BK1MPC2Sel	2	Buck1 PGOOD Interrupt MPC2 assignment control	0: Buck1 PGOOD Interrupt not routed to MPC2 1: Buck1 PGOOD Interrupt routed to MPC2
BK1MPC1Sel	1	Buck1 PGOOD Interrupt MPC1 assignment control	0: Buck1 PGOOD Interrupt not routed to MPC1 1: Buck1 PGOOD Interrupt routed to MPC1
BK1MPC0Sel	0	Buck1 PGOOD Interrupt MPC0 assignment control	0: Buck1 PGOOD Interrupt not routed to MPC0 1: Buck1 PGOOD Interrupt routed to MPC0

BK2DedIntCfg (0x71)

BIT	7	6	5	4	3	2	1	0
Field	BK2PGMPCInt	BK2MPC6Sel	BK2MPC5Sel	BK2MPC4Sel	BK2MPC3Sel	BK2MPC2Sel	BK2MPC1Sel	BK2MPC0Sel
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BK2PGMPCInt	7	Buck2 dedicated power-good interrupt	0: No power-good status change 1: Buck2 power-good status change caused interrupt
BK2MPC6Sel	6	Buck2 PGOOD Interrupt MPC6 assignment control	0: Buck2 PGOOD Interrupt not routed to MPC6 1: Buck2 PGOOD Interrupt routed to MPC6
BK2MPC5Sel	5	Buck2 PGOOD Interrupt MPC5 assignment control	0: Buck2 PGOOD Interrupt not routed to MPC5 1: Buck2 PGOOD Interrupt routed to MPC5
BK2MPC4Sel	4	Buck2 PGOOD Interrupt MPC4 assignment control	0: Buck2 PGOOD Interrupt not routed to MPC4 1: Buck2 PGOOD Interrupt routed to MPC4
BK2MPC3Sel	3	Buck2 PGOOD Interrupt MPC3 assignment control	0: Buck2 PGOOD Interrupt not routed to MPC3 1: Buck2 PGOOD Interrupt routed to MPC3
BK2MPC2Sel	2	Buck2 PGOOD Interrupt MPC2 assignment control	0: Buck2 PGOOD Interrupt not routed to MPC2 1: Buck2 PGOOD Interrupt routed to MPC2
BK2MPC1Sel	1	Buck2 PGOOD Interrupt MPC1 assignment control	0: Buck2 PGOOD Interrupt not routed to MPC1 1: Buck2 PGOOD Interrupt routed to MPC1
BK2MPC0Sel	0	Buck2 PGOOD Interrupt MPC0 assignment control	0: Buck2 PGOOD Interrupt not routed to MPC0 1: Buck2 PGOOD Interrupt routed to MPC0

BK3DedIntCfg (0x72)

BIT	7	6	5	4	3	2	1	0
Field	BK3PGMPCInt	BK3MPC6Sel	BK3MPC5Sel	BK3MPC4Sel	BK3MPC3Sel	BK3MPC2Sel	BK3MPC1Sel	BK3MPC0Sel
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BK3PGMPCInt	7	Buck3 dedicated power-good interrupt	0: No power-good status change 1: Buck3 power-good status change caused interrupt
BK3MPC6Sel	6	Buck3 PGOOD Interrupt MPC6 assignment control	0: Buck3 PGOOD Interrupt not routed to MPC6 1: Buck3 PGOOD Interrupt routed to MPC6
BK3MPC5Sel	5	Buck3 PGOOD Interrupt MPC5 assignment control	0: Buck3 PGOOD Interrupt not routed to MPC5 1: Buck3 PGOOD Interrupt routed to MPC5
BK3MPC4Sel	4	Buck3 PGOOD Interrupt MPC4 assignment control	0: Buck3 PGOOD Interrupt not routed to MPC4 1: Buck3 PGOOD Interrupt routed to MPC4
BK3MPC3Sel	3	Buck3 PGOOD Interrupt MPC3 assignment control	0: Buck3 PGOOD Interrupt not routed to MPC3 1: Buck3 PGOOD Interrupt routed to MPC3
BK3MPC2Sel	2	Buck3 PGOOD Interrupt MPC2 assignment control	0: Buck3 PGOOD Interrupt not routed to MPC2 1: Buck3 PGOOD Interrupt routed to MPC2
BK3MPC1Sel	1	Buck3 PGOOD Interrupt MPC1 assignment control	0: Buck3 PGOOD Interrupt not routed to MPC1 1: Buck3 PGOOD Interrupt routed to MPC1
BK3MPC0Sel	0	Buck3 PGOOD Interrupt MPC0 assignment control	0: Buck3 PGOOD Interrupt not routed to MPC0 1: Buck3 PGOOD Interrupt routed to MPC0

HptDedIntCfg (0x73)

BIT	7	6	5	4	3	2	1	0
Field	HptStatDedInt	HPTMPC6Sel	HPTMPC5Sel	HPTMPC4Sel	HPTMPC3Sel	HPTMPC2Sel	HPTMPC1Sel	HPTMPC0Sel
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HptStatDedInt	7	Haptic Driver dedicated interrupt	0: No Haptic driver status change 1: Haptic driver status change caused interrupt
HPTMPC6Sel	6	Haptic Driver Interrupt MPC6 assignment control	0: Haptic Driver Interrupt not routed to MPC6 1: Haptic Driver Interrupt routed to MPC6
HPTMPC5Sel	5	Haptic Driver Interrupt MPC5 assignment control	0: Haptic Driver Interrupt not routed to MPC5 1: Haptic Driver Interrupt routed to MPC5
HPTMPC4Sel	4	Haptic Driver Interrupt MPC4 assignment control	0: Haptic Driver Interrupt not routed to MPC4 1: Haptic Driver Interrupt routed to MPC4
HPTMPC3Sel	3	Haptic Driver Interrupt MPC3 assignment control	0: Haptic Driver Interrupt not routed to MPC3 1: Haptic Driver Interrupt routed to MPC3
HPTMPC2Sel	2	Haptic Driver Interrupt MPC2 assignment control	0: Haptic Driver Interrupt not routed to MPC2 1: Haptic Driver Interrupt routed to MPC2
HPTMPC1Sel	1	Haptic Driver Interrupt MPC1 assignment control	0: Haptic Driver Interrupt not routed to MPC1 1: Haptic Driver Interrupt routed to MPC1
HPTMPC0Sel	0	Haptic Driver Interrupt MPC0 assignment control	0: Haptic Driver Interrupt not routed to MPC0 1: Haptic Driver Interrupt routed to MPC0

ADCDedIntCfg (0x74)

BIT	7	6	5	4	3	2	1	0
Field	ADCStatMP CInt	ADCMPC6 Sel	ADCMPC5 Sel	ADCMPC4 Sel	ADCMPC3 Sel	ADCMPC2 Sel	ADCMPC1 Sel	ADCMPC0 Sel
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ADCStatMP CInt	7	ADC Conversion complete dedicated interrupt	0: No ADC end of conversion status change 1: ADC end of conversion caused interrupt
ADCMPC6S el	6	ADC End Of Conversion Interrupt MPC6 assignment control	0: ADC End of Conversion Interrupt not routed to MPC6 1: ADC End of Conversion Interrupt routed to MPC6
ADCMPC5S el	5	ADC End Of Conversion Interrupt MPC5 assignment control	0: ADC End of Conversion Interrupt not routed to MPC5 1: ADC End of Conversion Interrupt routed to MPC5
ADCMPC4S el	4	ADC End Of Conversion Interrupt MPC4 assignment control	0: ADC End of Conversion Interrupt not routed to MPC4 1: ADC End of Conversion Interrupt routed to MPC4
ADCMPC3S el	3	ADC End Of Conversion Interrupt MPC3 assignment control	0: ADC End of Conversion Interrupt not routed to MPC3 1: ADC End of Conversion Interrupt routed to MPC3
ADCMPC2S el	2	ADC End Of Conversion Interrupt MPC2 assignment control	0: ADC End of Conversion Interrupt not routed to MPC2 1: ADC End of Conversion Interrupt routed to MPC2
ADCMPC1S el	1	ADC End Of Conversion Interrupt MPC1 assignment control	0: ADC End of Conversion Interrupt not routed to MPC1 1: ADC End of Conversion Interrupt routed to MPC1
ADCMPC0S el	0	ADC End Of Conversion Interrupt MPC0 assignment control	0: ADC End of Conversion Interrupt not routed to MPC0 1: ADC End of Conversion Interrupt routed to MPC0

USBOkDedIntCfg (0x75)

BIT	7	6	5	4	3	2	1	0
Field	USBOkMP CInt	USBOkMP C6Sel	USBOkMP C5Sel	USBOkMP C4Sel	USBOkMP C3Sel	USBOkMP C2Sel	USBOkMP C1Sel	USBOkMP C0Sel
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
USBOkMPCI nt	7	USBOk dedicated Power-Good Interrupt	0: No USBOk status change 1: USBOk status change caused interrupt
USBOkMPC 6Sel	6	USBOk Dedicated Interrupt MPC6 assignment control	0: USBOk Interrupt not routed to MPC6 1: USBOk Interrupt routed to MPC6

BITFIELD	BITS	DESCRIPTION	DECODE
USBOkMPC5Sel	5	USBOk Dedicated Interrupt MPC5 assignment control	0: USBOk Interrupt not routed to MPC5 1: USBOk Interrupt routed to MPC5
USBOkMPC4Sel	4	USBOk Dedicated Interrupt MPC4 assignment control	0: USBOk Interrupt not routed to MPC4 1: USBOk Interrupt routed to MPC4
USBOkMPC3Sel	3	USBOk Dedicated Interrupt MPC3 assignment control	0: USBOk Interrupt not routed to MPC3 1: USBOk Interrupt routed to MPC3
USBOkMPC2Sel	2	USBOk Dedicated Interrupt MPC2 assignment control	0: USBOk Interrupt not routed to MPC2 1: USBOk Interrupt routed to MPC2
USBOkMPC1Sel	1	USBOk Dedicated Interrupt MPC1 assignment control	0: USBOk Interrupt not routed to MPC1 1: USBOk Interrupt routed to MPC1
USBOkMPC0Sel	0	USBOk Dedicated Interrupt MPC0 assignment control	0: USBOk Interrupt not routed to MPC0 1: USBOk Interrupt routed to MPC0

LEDCommon (0x78)

BIT	7	6	5	4	3	2	1	0
Field	LED_BoostLoop	–	–	LED_Open[2:0]			LEDIStep[1:0]	
Access Type	Write, Read	–	–	Read Only			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LED_BoostLoop	7	Boost/LED0 closed-loop operation control	0: Boost voltage is unrelated to LED0 dropout voltage. 1: Boost voltage is incresed respect to BstVSet to adjust LED0 dropout voltage according to LED0_REFSEL bits. Maximum increment is 5V.
LED_Open	4:2	LEDx open detection (Read only)	Bit 0 = 0: 0 = $V_{LED0} > V_{LED\_DET}$ or all LED disabled 1 = $V_{LED0} \leq V_{LED\_DET}$ or LED0 only disabled Bit 1 = 1: 0 = $V_{LED1} > V_{LED\_DET}$ or all LED disabled 1 = $V_{LED1} \leq V_{LED\_DET}$ or LED1 only disabled Bit 2 = 1: 0 = $V_{LED2} > V_{LED\_DET}$ or all LED disabled 1 = $V_{LED2} \leq V_{LED\_DET}$ or LED2 only disabled
LEDIStep	1:0	LED current step-size control	00: 0.6mA 01: 1.0mA 10: 1.2mA 11: RESERVED

LED0Ref (0x79)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LED0_REFSEL[1:0]	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LED0_REFSEL	1:0	LED0 dropout regulation voltage (valid only if LED_BoostLoop = 1)	00: 0.2V 01: 0.3V 10: 0.4V 11: 0.5V

LED0Ctr (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	LED0En[2:0]			LED0ISet[4:0]				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
LED0En	7:5	LED0 driver enable	000: Off 001: LED0 On 010: Controlled by internal charger status signal 011: Controlled by MPC3 100: Controlled by MPC4 101: Controlled by MPC5 110: Controlled by MPC6 111: Controlled by MPC7
LED0ISet	4:0	LED0 Direct Step Count. LED0 current in mA is given by (LED0_I[4:0] + 1) x LEDIStep[1:0]	00000: 0.6mA/1.0mA/1.2mA 00001: 1.2mA/2.0mA/2.4mA 00010: 1.8mA/3.0mA/3.6mA 00011: 2.4mA/4.0mA/4.8mA 00100: 3.0mA/5.0mA/6.0mA 00101: 3.6mA/6.0mA/7.2mA 00110: 4.2mA/7.0mA/8.4mA 00111: 4.8mA/8.0mA/9.6mA 01000: 5.4mA/9.0mA/10.8mA 01001: 6.0mA/10.0mA/12.0mA 01010: 6.6mA/11.0mA/13.2mA 01011: 7.2mA/12.0mA/14.4mA 01100: 7.8mA/13.0mA/15.6mA 01101: 8.4mA/14.0mA/16.8mA 01110: 9.0mA/15.0mA/18.0mA 01111: 9.6mA/16.0mA/19.2mA 10000: 10.2mA/17.0mA/20.4mA 10001: 10.8mA/18.0mA/21.6mA 10010: 11.4mA/19.0mA/22.8mA 10011: 12.0mA/20.0mA/24.0mA 10100: 12.6mA/21.0mA/25.2mA 10101: 13.2mA/22.0mA/26.4mA 10110: 13.8mA/23.0mA/27.6mA 10111: 14.4mA/24.0mA/28.8mA 11000: 15.0mA/25.0mA/30.0mA

LED1Ctr (0x7B)

BIT	7	6	5	4	3	2	1	0
Field	LED1En[2:0]			LED1ISet[4:0]				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
LED1En	7:5	LED1 driver enable	000: Off 001: LED1 On 010: Controlled by internal charger status signal 011: Controlled by MPC3 100: Controlled by MPC4 101: Controlled by MPC5 110: Controlled by MPC6 111: Controlled by MPC7
LED1ISet	4:0	LED1 Direct Step Count. LED1 current in mA is given by (LED1_I[4:0] + 1) x LEDIStep[1:0]	00000: 0.6mA/1.0mA/1.2mA 00001: 1.2mA/2.0mA/2.4mA 00010: 1.8mA/3.0mA/3.6mA 00011: 2.4mA/4.0mA/4.8mA 00100: 3.0mA/5.0mA/6.0mA 00101: 3.6mA/6.0mA/7.2mA 00110: 4.2mA/7.0mA/8.4mA 00111: 4.8mA/8.0mA/9.6mA 01000: 5.4mA/9.0mA/10.8mA 01001: 6.0mA/10.0mA/12.0mA 01010: 6.6mA/11.0mA/13.2mA 01011: 7.2mA/12.0mA/14.4mA 01100: 7.8mA/13.0mA/15.6mA 01101: 8.4mA/14.0mA/16.8mA 01110: 9.0mA/15.0mA/18.0mA 01111: 9.6mA/16.0mA/19.2mA 10000: 10.2mA/17.0mA/20.4mA 10001: 10.8mA/18.0mA/21.6mA 10010: 11.4mA/19.0mA/22.8mA 10011: 12.0mA/20.0mA/24.0mA 10100: 12.6mA/21.0mA/25.2mA 10101: 13.2mA/22.0mA/26.4mA 10110: 13.8mA/23.0mA/27.6mA 10111: 14.4mA/24.0mA/28.8mA 11000: 15.0mA/25.0mA/30.0mA

LED2Ctr (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	LED2En[2:0]			LED2ISet[4:0]				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
LED2En	7:5	LED2 driver enable	000: Off 001: LED2 On 010: Controlled by internal charger status signal 011: Controlled by MPC3 100: Controlled by MPC4 101: Controlled by MPC5 110: Controlled by MPC6 111: Controlled by MPC7

BITFIELD	BITS	DESCRIPTION	DECODE
LED2ISet	4:0	LED2 Direct Step Count. LED2 current in mA is given by (LED2_I[4:0] + 1) x LEDIStep[1:0]	00000: 0.6mA/1.0mA/1.2mA 00001: 1.2mA/2.0mA/2.4mA 00010: 1.8mA/3.0mA/3.6mA 00011: 2.4mA/4.0mA/4.8mA 00100: 3.0mA/5.0mA/6.0mA 00101: 3.6mA/6.0mA/7.2mA 00110: 4.2mA/7.0mA/8.4mA 00111: 4.8mA/8.0mA/9.6mA 01000: 5.4mA/9.0mA/10.8mA 01001: 6.0mA/10.0mA/12.0mA 01010: 6.6mA/11.0mA/13.2mA 01011: 7.2mA/12.0mA/14.4mA 01100: 7.8mA/13.0mA/15.6mA 01101: 8.4mA/14.0mA/16.8mA 01110: 9.0mA/15.0mA/18.0mA 01111: 9.6mA/16.0mA/19.2mA 10000: 10.2mA/17.0mA/20.4mA 10001: 10.8mA/18.0mA/21.6mA 10010: 11.4mA/19.0mA/22.8mA 10011: 12.0mA/20.0mA/24.0mA 10100: 12.6mA/21.0mA/25.2mA 10101: 13.2mA/22.0mA/26.4mA 10110: 13.8mA/23.0mA/27.6mA 10111: 14.4mA/24.0mA/28.8mA 11000: 15.0mA/25.0mA/30.0mA

PFN (0x7D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PFN2Pin	PFN1Pin
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PFN2Pin	1	Status of PFN2	0: PFN2 not active 1: PFN2 active
PFN1Pin	0	Status of PFN2	0: PFN1 not active 1: PFN1 active

BootCfg (0x7E)

BIT	7	6	5	4	3	2	1	0
Field	PwrRstCfg[3:0]				SftRstCfg	BootDly[1:0]		ChgAlwTry
Access Type	Read Only				Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PwrRstCfg	7:4	Power Reset Configuration. Determines how the device turns on, off, and enters hard-/soft-reset. See PwrRstCfg Settings (Table 4) for PwrRstCfg values and their associated behaviors.	
SftRstCfg	3	Soft-Reset Configuration. Indicates whether registers are held or reset to default during a soft-reset.	0: Hold register contents 1: Reset registers to default

BITFIELD	BITS	DESCRIPTION	DECODE
BootDly	2:1	Boot delay. The boot period when the sequencing engine turns on features with sequence bits 010, 011, and 100.	00: 80ms 01: 120ms 10: 220ms 11: 420ms
ChgAlwTry	0	SYS UVLO automatic retry. Determines what happens when a SYS UVLO event occurs during the boot process with CHGIN present.	0: Part latches off until CHGIN is removed 1: Part retries to boot after $t_{CHG\_RETRY\_TMO}$ delay if CHGIN is still present

PwrCfg (0x7F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	StayOn
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
StayOn	0	This bit is used to ensure that the processor booted correctly. This bit must be set within 5s of power-on to prevent the part from shutting down and returning to the power-off condition. This bit has no effect after being set.	0: Shut down 5s after power-on 1: Stay on

PwrCmd (0x80)

BIT	7	6	5	4	3	2	1	0
Field	PwrCmd[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PwrCmd	7:0	Power Command Register. Writing the following values issues the command listed. After the written value has been validated by the internal logic, this register is cleared automatically. Any other commands are ignored. See PwrRstCfg Settings for the available PwrCmd for each PwrRstCfg value.	0xB2: PWR_OFF_CMD: Places the part in OFF mode 0xC3: PWR_HR_CMD: Issues a hard-reset (power cycle) 0xD4: PWR_SR_CMD: Issues a soft-reset (reset pulse only) 0xE5: PWR_SEAL_CMD: Places the part in Seal mode Available only for PwrRstCfg 1011 and 1100 0xF6: PWR_BR_CMD: Places the Part in Battery Recovery Mode available only if HrvEn=1

BuckCfg (0x81)

BIT	7	6	5	4	3	2	1	0
Field	Bk2FrcDCM	Bk1FrcDCM	Bk3DVSCur	Bk2DVSCur	Bk1DVSCur	Bk3LowBW	Bk2LowBW	Bk1LowBW
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
Bk2FrcDCM	7	Buck 2 Forced Discontinuous Conduction Mode (DCM). Improves light load efficiency at the expense of load regulation error at higher loads. This should only be used if the expected maximum load is less than 50mA 0 = Normal operation 1 = Forced DCM operation
Bk1FrcDCM	6	Buck 1 Forced Discontinuous Conduction Mode (DCM). Improves light load efficiency at the expense of load regulation error at higher loads. This should only be used if the expected maximum load is less than 50mA 0 = Normal operation 1 = Forced DCM operation
Bk3DVSCur	5	Buck 3 DVS Valley Current Selection. 0 = 500mA valley current during DVS transition 1 = 1000mA valley current during DVS transition
Bk2DVSCur	4	Buck 2 DVS Valley Current Selection. 0 = 500mA valley current during DVS transition 1 = 1000mA valley current during DVS transition
Bk1DVSCur	3	Buck 1 DVS Valley Current Selection. 0 = 500mA valley current during DVS transition 1 = 1000mA valley current during DVS transition
Bk3LowBW	2	Buck 3 Low Bandwidth Mode. This mode reduces the amount of capacitance required to minimize jitter when transitioning from DCM to CCM. If this bit is enabled, the output capacitance requirement is cut in half. 0 = High bandwidth mode 1 = Low bandwidth mode
Bk2LowBW	1	Buck 2 Low Bandwidth Mode. This mode reduces the amount of capacitance required to minimize jitter when transitioning from DCM to CCM. If this bit is enabled, the output capacitance requirement is cut in half. 0 = High bandwidth mode 1 = Low bandwidth mode
Bk1LowBW	0	Buck 1 Low Bandwidth Mode. This mode reduces the amount of capacitance required to minimize jitter when transitioning from DCM to CCM. If this bit is enabled, the output capacitance requirement is cut in half. 0 = High bandwidth mode 1 = Low bandwidth mode

LockMsk (0x83)

BIT	7	6	5	4	3	2	1	0
Field	LD2Lck	LD1Lck	BBLck	BstLck	BK3Lck	BK2Lck	BK1Lck	ChgLck
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LD2Lck	7	Lock Mask for LDO2 registers	0: LDO2 registers not masked from locking/ unlocking 1: LDO2 registers masked from locking/unlocking

BITFIELD	BITS	DESCRIPTION	DECODE
LD1Lck	6	Lock Mask for LDO1 registers	0: LDO1 registers not masked from locking/ unlocking 1: LDO1 registers masked from locking/unlocking
BBLck	5	Lock Mask for buck-boost registers	0: Buck-Boost registers not masked from locking/ unlocking 1: Buck-Boost registers masked from locking/ unlocking
BstLck	4	Lock Mask for boost registers	0x0: Boost registers not masked from locking/ unlocking 0x1: Boost registers masked from locking/ unlocking
BK3Lck	3	Lock Mask for Buck3 registers	0x0: Buck3 registers not masked from locking/ unlocking 0x1: Buck3 registers masked from locking/ unlocking
BK2Lck	2	Lock Mask for Buck2 registers	0x0: Buck2 registers not masked from locking/ unlocking 0x1: Buck2 registers masked from locking/ unlocking
BK1Lck	1	Lock Mask for Buck1 registers	0x0: Buck1 registers not masked from locking/ unlocking 0x1: Buck1 registers masked from locking/ unlocking
ChgLck	0	Lock Mask for charger registers	0x0: Charger registers not masked from locking/ unlocking 0x1: Charger registers masked from locking/ unlocking

LockUnlock (0x84)

BIT	7	6	5	4	3	2	1	0
Field	PASSWD[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PASSWD	7:0	Lock/Unlock Password. Locks or unlocks all unmasked functions set in the Lock Mask register 0x83 when the correct password is written. Reading this register returns the current lock state of the functions. Locked functions return 1 and unlocked functions return 0. Functions are organized in the same order as register 0x83.	0x55: Unlock unmasked functions 0xAA: Lock unmasked functions All Other Codes: No effect

SFOUTCtr (0x86)

BIT	7	6	5	4	3	2	1	0
Field	SFOUTVSet	–	–	–	–	–	SFOUTEn[1:0]	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SFOUTVSet	7	SFOUT LDO output voltage setting.	0: 5.0V 1: 3.3V
SFOUTEn	1:0	SFOUT LDO enable configuration.	0x0: Disabled (regardless of CHGIN state). 0x1: Enabled when CHGIN input voltage is present. 0x2: Enabled when CHGIN input voltage is present and controlled by MPC_ (see SFOUTMPC_ bits in register 0x87) 0x3: Reserved.

SFOUTMPC (0x87)

BIT	7	6	5	4	3	2	1	0
Field	SFOUTMPC7	SFOUTMPC6	SFOUTMPC5	SFOUTMPC4	SFOUTMPC3	SFOUTMPC2	SFOUTMPC1	SFOUTMPC0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SFOUTMPC7	7	SFOUT MPC7 Enable Control. If multiple MPCs are selected, SFOUT is controlled by the logical OR of the MPCs.	0: SFOUT not controlled by MPC7 1: SFOUT controlled by MPC7
SFOUTMPC6	6	SFOUT MPC6 Enable Control. If multiple MPCs are selected, SFOUT is controlled by the logical OR of the MPCs.	0: SFOUT not controlled by MPC6 1: SFOUT controlled by MPC6
SFOUTMPC5	5	SFOUT MPC5 Enable Control. If multiple MPCs are selected, SFOUT is controlled by the logical OR of the MPCs.	0: SFOUT not controlled by MPC5 1: SFOUT controlled by MPC5
SFOUTMPC4	4	SFOUT MPC4 Enable Control. If multiple MPCs are selected, SFOUT is controlled by the logical OR of the MPCs.	0: SFOUT not controlled by MPC4 1: SFOUT controlled by MPC4
SFOUTMPC3	3	SFOUT MPC3 Enable Control. If multiple MPCs are selected, SFOUT is controlled by the logical OR of the MPCs.	0: SFOUT not controlled by MPC3 1: SFOUT controlled by MPC3
SFOUTMPC2	2	SFOUT MPC2 Enable Control. If multiple MPCs are selected, SFOUT is controlled by the logical OR of the MPCs.	0: SFOUT not controlled by MPC2 1: SFOUT controlled by MPC2
SFOUTMPC1	1	SFOUT MPC1 Enable Control. If multiple MPCs are selected, SFOUT is controlled by the logical OR of the MPCs.	0: SFOUT not controlled by MPC1 1: SFOUT controlled by MPC1
SFOUTMPC0	0	SFOUT MPC0 Enable Control. If multiple MPCs are selected, SFOUT is controlled by the logical OR of the MPCs.	0: SFOUT not controlled by MPC0 1: SFOUT controlled by MPC0

I2C_OTP (0x88)

BIT	7	6	5	4	3	2	1	0
Field	OTPDIG__ADD[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OTPDIG__ADD	7:0	This is the address of the OTP reg file for OTP registers read back. OTP registers are filled with data from Sidense OTP block during boot.

I2C_OTP (0x89)

BIT	7	6	5	4	3	2	1	0
Field	OTPDIG__DAT[7:0]							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTPDIG__DAT	7:0	This is the OTP data read back.

Applications Information

I²C Interface

The MAX20360 contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

Start, Stop, and Repeated Start Conditions

When writing to the MAX20360 using the I²C interface, the master sends a START condition (S) followed by the MAX20360 I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See Figure 36.

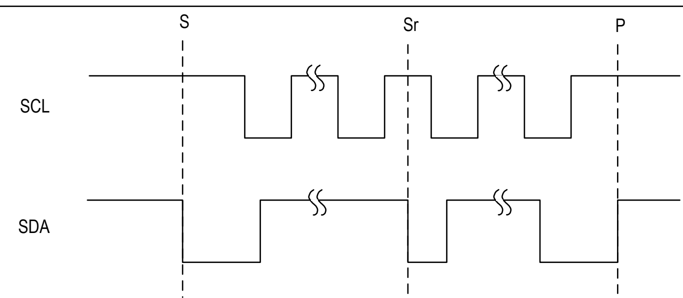


Figure 36. I²C START, STOP, and REPEATED START Conditions

Slave Address

Set the Read/$\overline{\text{Write}}$ bit high to configure the MAX20360 to read mode. Set the Read/$\overline{\text{Write}}$ bit low to configure the MAX20360 to write mode. The address is the first byte of information sent to the MAX20360 after the START condition. The MAX20360 has three slave addresses. For the ADC and haptic driver registers, the slave address is 0xA0/0xA1; for the PMIC the slave address is 0x50/0x51; and for the fuel gauge, the slave address is 0x6C/0x6D.

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *Start, Stop, and Repeated Start Conditions* section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 37). The following procedure describes the single byte write operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NAK if not).
- The master sends 8 data bits.
- The slave asserts an ACK on the data line.
- The master generates a STOP condition.

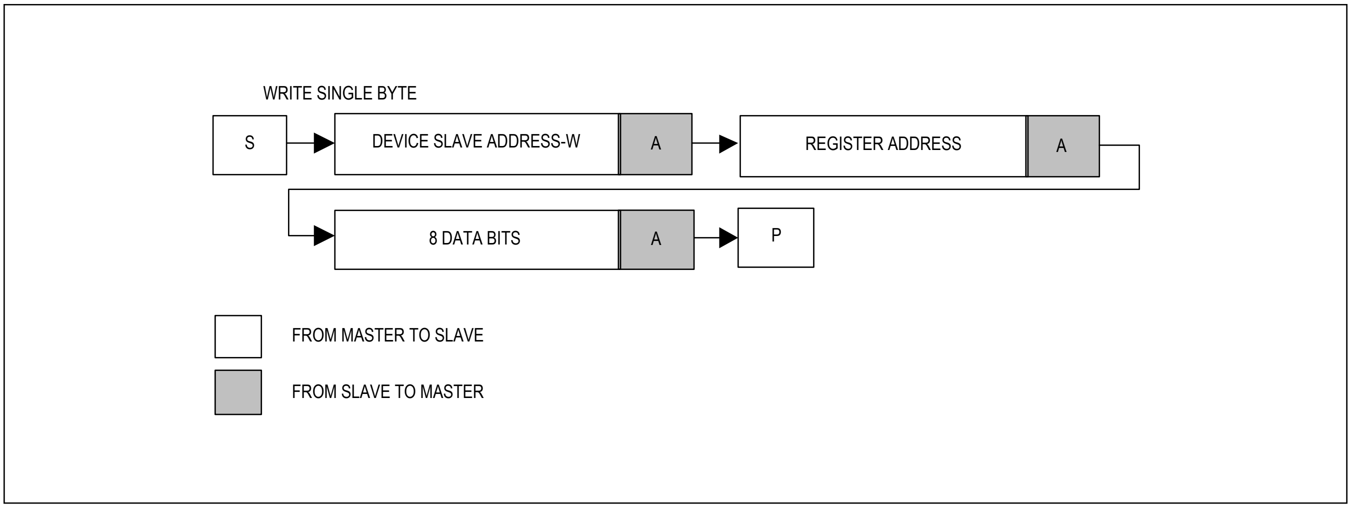


Figure 37. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 38). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NAK if not).
- The master sends 8 data bits.
- The slave asserts an ACK on the data line.
- Repeat 6 and 7 N-1 times.
- The master generates a STOP condition.

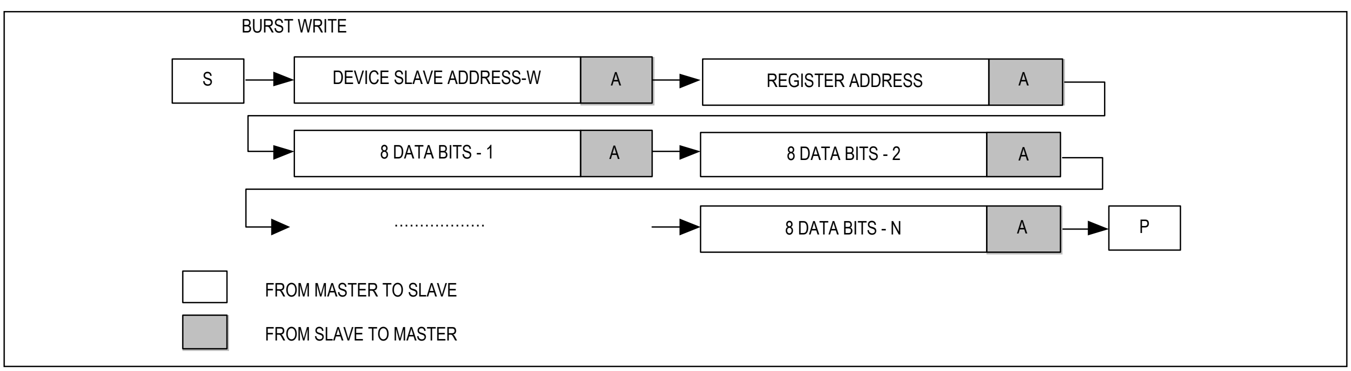


Figure 38. Burst Write Sequence

Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 39). The following procedure describes the single byte read operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NAK if not).
- The master sends a REPEATED START condition.
- The master sends the 7-bit slave address plus a read bit (high).
- The addressed slave asserts an ACK on the data line.
- The slave sends 8 data bits.
- The master asserts a NACK on the data line.
- The master generates a STOP condition.

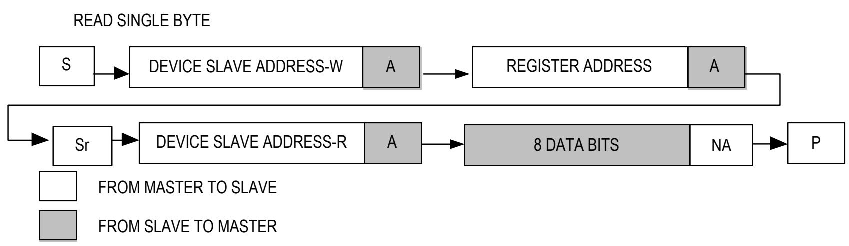


Figure 39. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 40). The following procedure describes the burst byte read operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NAK if not).
- The master sends a REPEATED START condition.
- The master sends the 7-bit slave address plus a read bit (high).
- The slave asserts an ACK on the data line.
- The slave sends 8 data bits.
- The master asserts an ACK on the data line.
- Repeat 9 and 10 N-2 times.
- The slave sends the last 8 data bits.
- The master asserts a NACK on the data line.
- The master generates a STOP condition.

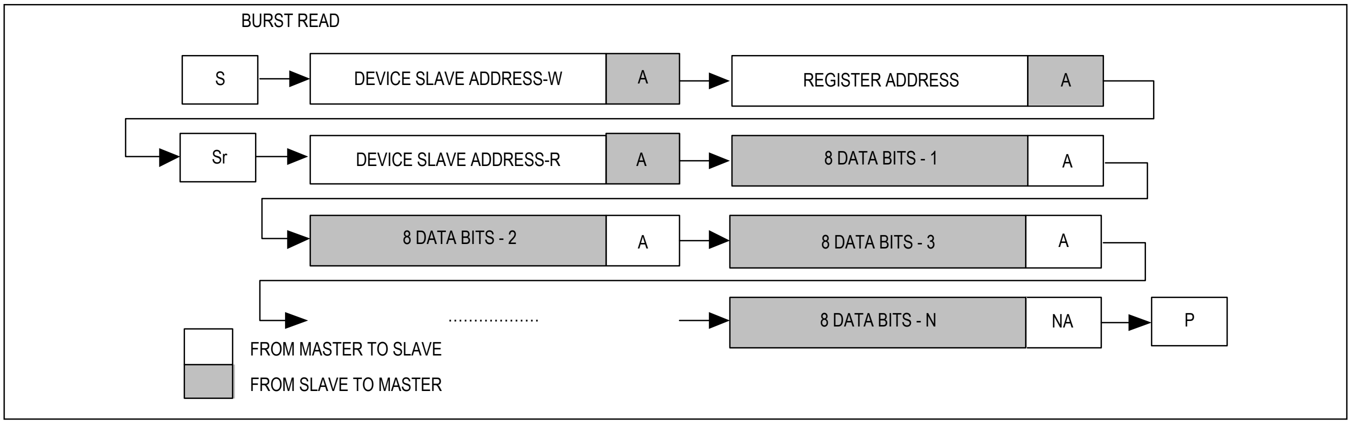


Figure 40. Burst Read Sequence

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX20360 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 41). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

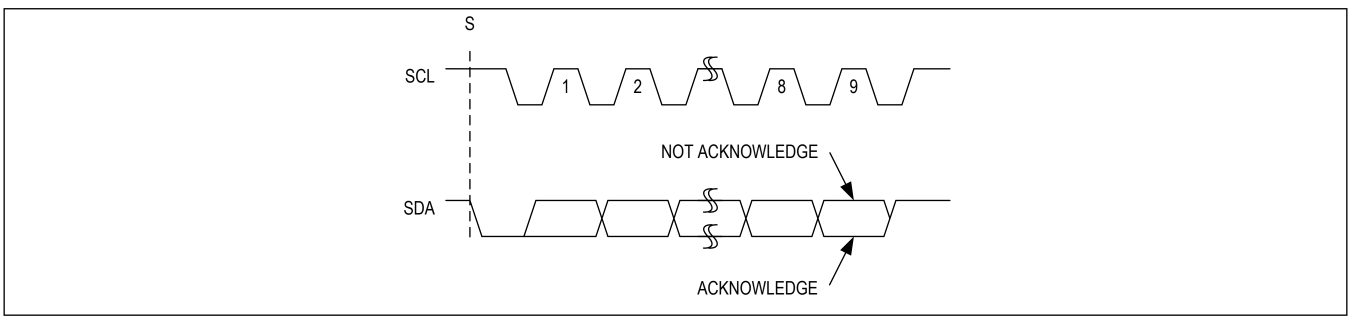


Figure 41. Acknowledge Bits

I²C Security Functions

Function Locking

All regulator voltages and the end-of-charge behavior of the charger can be locked. I²C writes to a locked bitfield have no effect. To lock a function, its lock mask must be removed in the LockMsk register (see *LockMsk*). To remove the lock mask, set the corresponding function mask bit to 0. By writing the lock password 0xAA to the LockUnlock register (see *LockUnlock*), all unmasked functions are locked. To unlock functions, repeat the mask/unmask process and write the unlock password 0x55 to the LockUnlock register (see *LockUnlock*). Registers covered by the lock functions are denoted by an asterisk in the register map.

Secure Writes with Fletcher-16 Checksum

The MAX20360 includes an optional safe I²C-write mode for the registers contained under the PMIC slave address (SLAVE_ID 0x50). When enabled, only single-byte writes are allowed on the PMIC address and each write sequence must be followed by a two-byte checksum (see Figure 42 for the write sequence). In the event that the checksum evaluation returns TRUE, the PMIC immediately writes the value of the write to the appropriate register. In the event that the checksum evaluation returns FALSE, the write is not performed and an interrupt indicating write failure is sent to the system microcontroller.

The fletcher checksum is calculated using the below equations:

CSUM1 = (SLAVE_ID + REG_ADD + DATA) ÷ 255

CSUM2 = ((3 × SLAVE_ID) + (2 × REG_ADD) + (DATA)) ÷ 255

Where SLAVE_ID = 0x50, REG_ADD is the register address being written, DATA is the byte of data to be written, and ÷ is the modulo function. The write sequence is as shown in Figure 42 below.

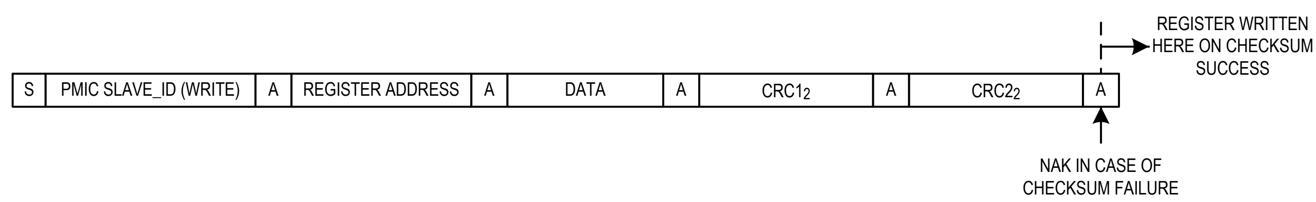


Figure 42. I²C Writes on PMIC Slave Address with Fletcher-16 Checksum

Default Bits

Table 8 shows the default settings for different versions. These default values are OTP programmable. Some bits can be changed through the I²C interface after power-up while some bits are set through OTP.

Table 8. Device Default Settings

FIELD	EV KIT	MAX20360A	MAX20360B
SysMinVlt	3.6V	4.0V	4.0V
ILimBlank	Disabled	Disabled	Disabled
ILimCntl	450mA	450mA	450mA
IChgDone	30% I_{FCHG}	10% I_{FCHG}	10% I_{FCHG}
ChgBatReChg	ChgBatReg - 70mV	ChgBatReg - 120mV	ChgBatReg - 120mV
ChgBatReg	4.35V	4.20V	4.20V
ChgEn	Enabled	Enabled	Enabled
PChgTmr	60min	30min	30min
VPChg	3.15V	3.00V	3.00V
IPChg	5% I_{FCHG}	10% I_{FCHG}	5% I_{FCHG}
ChgStepHys	400mV	400mV	400mV
ChgStepRise	3.80V	4.55V	4.55V
ChgAutoStop	Enabled	Enabled	Enabled
ChgAutoReSta	Enabled	Enabled	Enabled
MtChgTmr	60min	30min	30min
FChgTmr	600min	150min	150min
ChgIStep	100% I_{FCHG}	100% I_{FCHG}	100% I_{FCHG}
HrvBatReg	N/A	N/A	4.20V
HrvThmEn	N/A	N/A	Cool/Room/Warm
ChgThmEn	Cool/Room	Cool/Room	Cool/Room
VSysUvlo	2.7V	3.0V	3.0V

Table 8. Device Default Settings (continued)

FIELD	EV KIT	MAX20360A	MAX20360B
HrvThmDis	N/A	N/A	Force SYS-to-BAT Ideal Diode
HrvBatSys	N/A	N/A	Direct if V_{BAT} < HrvBatReg
HrvBatReChg	N/A	N/A	HrvBatReg - 120mV
Bk1Step	10mV	10mV	50mV
Buck1VSet	1.10V	0.70V	1.80V
Bk2Step	25mV	10mV	10mV
Buck2VSet	1.800V	1.05V	1.05V
Bk3Step	50mV	50mV	50mV
Buck3VSet	3.20V	1.85V	1.80V
Buck1FETScale	Disabled	Disabled	Disabled
Buck1En	Disabled	Disabled	Disabled
Buck2En	Disabled	Enabled	Enabled
Buck2FETScale	Disabled	Disabled	Disabled
Buck3FETScale	Disabled	Disabled	Disabled
Buck3En	Disabled	Enabled	Enabled
Buck3DisLDO	LDO Enabled	Buck Always	Buck Always
BBstVSet	5.00V	5.00V	5.00V
BBstMode	Buck-Boost	Buck-Boost	Buck-Boost
BBstEn	Disabled	Disabled	Disabled
LDO1Mode	LDO	Load Switch	Load Switch
LDO1En	Disabled	Disabled	Disabled
BBstFast	Low I_Q	Low I_Q	Low I_Q
BBstFETScale	Disabled	Disabled	Disabled
LDO2En	Disabled	Enabled	Enabled
LDO1VSet	0.500V	1.850V	1.800V
LSW1En	Disabled	Disabled	Disabled
LDO2VSet	0.9V	1.8V	1.8V
LDO2Supply	External	Internal	Internal
LDO2Mode	LDO	LDO	LDO
CPVSet	5.0V	5.0V	5.0V
ChgPmpEn	Disabled	Disabled	Disabled
LSW2LowIq	Low-I_Q	Protected	Protected
LSW2En	Disabled	Disabled	Disabled
LSW1LowIq	Low-I_Q	Protected	Protected
BstVSet	12.00V	20.00V	20.00V
Bk1DVSCur	1A	0.5A	0.5A
Bk1LowBW	Full BW	Full BW	Full BW

Table 8. Device Default Settings (continued)

FIELD	EV KIT	MAX20360A	MAX20360B
Bk1FrcDCM	Normal Mode	Normal Mode	Normal Mode
Bk2DVSCur	1A	0.5A	0.5A
Bk2LowBW	Full BW	Full BW	Full BW
Bk2FrcDCM	Normal Mode	Normal Mode	Normal Mode
Bk3DVSCur	1A	0.5A	0.5A
Bk3LowBW	Full BW	Full BW	Full BW
INT_MSK_DIS	$\overline{INT}$ mask until 100% Boot	$\overline{INT}$ mask until 100% Boot	$\overline{INT}$ mask until 100% Boot
BstEn	Disabled	Disabled	Disabled
PwrRstCfg	1011	1011	1011
SftRstCfg	Reset Regs	Reset Regs	Reset Regs
BootDly	80ms	80ms	80ms
ChgAlwTry	Retry	Retry	Retry
StayOn	Enabled	Enabled	Enabled
SFOUTVSet	3.3V	3.3V	3.3V
SFOUTEn	CHGIN	CHGIN	CHGIN
UsbOkselect	CHGIN Rise	CHGIN Rise	CHGIN Rise
LDO1Seq	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%
BBstSeq	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%
IBatOc	1600mA	1400mA	1400mA
Buck1Seq	Buck1En After 100%	Buck1En After 100%	Buck1En After 100%
Buck2Seq	Buck2En After 100%	50%	50%
Buck3Seq	Buck3En After 100%	25%	25%
LSW1Seq	LSW1En After 100%	LSW1En After 100%	LSW1En After 100%
BoostSeq	BstEn After 100%	BstEn After 100%	BstEn After 100%
LDO2Seq	LDO2En After 100%	0%	0%
ChgPmpSeq	ChgPmpEn After 100%	ChgPmpEn After 100%	ChgPmpEn After 100%
LSW2Seq	LSW2En After 100%	LSW2En After 100%	LSW2En After 100%
PFN1RES	Connect Resistor	Connect Resistor	Connect Resistor
PFN1PU	Pullup	Pullup	Pullup
PFN2RES	No Resistor	No Resistor	No Resistor
PFN2PU	N/A	N/A	N/A
HrvEn	Disabled	Disabled	Enabled
i2c_crc_ena	Enabled	Enabled	Enabled
i2c_tmo_ena	Enabled	Enabled	Enabled
DrvTmo	Disabled	Disabled	Disabled
HptSel	LRA	LRA	LRA
ILimMax	1000mA	450mA	450mA

Table 8. Device Default Settings (continued)

FIELD	EV KIT	MAX20360A	MAX20360B
JEITASet	T4 = 25.53%, T3 = 32.94%	T4 = 25.53%, T3 = 32.94%	T4_HARV = 14.51%, T3 = 32.94%
TShdn	120°C	120°C	120°C

Register Defaults

Table 9 shows the default values of all the registers.

Table 9. I2C Direct Register Defaults

SLAVE ADDRESS	REGISTER ADD	REGISTER NAME	EV KIT	MAX20360A	MAX20360B
0xA0	0x00	HptStatus0	0x00	0x00	0x00
0xA0	0x01	HptStatus1	0x00	0x00	0x00
0xA0	0x02	HptStatus2	0x00	0x00	0x00
0xA0	0x03	HptInt0	0x00	0x00	0x00
0xA0	0x04	HptInt1	0x00	0x00	0x00
0xA0	0x05	HptInt2	0x00	0x00	0x00
0xA0	0x06	HptIntMask0	0x00	0x00	0x00
0xA0	0x07	HptIntMask1	0x00	0x00	0x00
0xA0	0x08	HptIntMask2	0x00	0x00	0x00
0xA0	0x09	HptControl	0x00	0x00	0x00
0xA0	0x0A	HptRTI2CPat	0x00	0x00	0x00
0xA0	0x0B	HptRAMPatAdd	0x00	0x00	0x00
0xA0	0x0C	HptProt	0x04	0x04	0x04
0xA0	0x0D	HptUnlock	0x00	0x00	0x00
0xA0	0x11	HPTCfg0	0x0E	0x0E	0x0E
0xA0	0x12	HPTCfg1	0x8B	0x8B	0x8B
0xA0	0x13	HPTCfg2	0x8B	0x8B	0x8B
0xA0	0x14	HPTCfg3	0x19	0x19	0x19
0xA0	0x15	HPTCfg4	0x03	0x03	0x03
0xA0	0x16	HPTCfg5	0x05	0x05	0x05
0xA0	0x17	HPTCfg6	0x11	0x11	0x11
0xA0	0x18	HPTCfg7	0x08	0x08	0x08
0xA0	0x19	HPTCfg8	0x1F	0x1F	0x1F
0xA0	0x1A	HPTCfg9	0x84	0x84	0x84
0xA0	0x1B	HPTCfgA	0x07	0x07	0x07
0xA0	0x1C	HPTCfgB	0x40	0x40	0x40
0xA0	0x1D	HPTCfgC	0xD0	0xD0	0xD0
0xA0	0x1E	HPTCfgD	0x07	0x07	0x07
0xA0	0x1F	HPTCfgE	0x06	0x06	0x06
0xA0	0x20	HPTCfgF	0x24	0x24	0x24
0xA0	0x22	HptAutoTune	0x00	0x00	0x00
0xA0	0x23	BEMFPeriod0	0xD0	0xD0	0xD0
0xA0	0x24	BEMFPeriod1	0x07	0x07	0x07

Table 9. I²C Direct Register Defaults (continued)

SLAVE ADDRESS	REGISTER ADD	REGISTER NAME	EV KIT	MAX20360A	MAX20360B
0xA0	0x30	HptETRGOdAmp	0x7F	0x7F	0x7F
0xA0	0x31	HptETRGOdDur	0x04	0x04	0x04
0xA0	0x32	HptETRGActAmp	0x3F	0x3F	0x3F
0xA0	0x33	HptETRGActDur	0x32	0x32	0x32
0xA0	0x34	HptETRGBrkAmp	0xFF	0xFF	0xFF
0xA0	0x35	HptETRGBrkDur	0x20	0x20	0x20
0xA0	0x40	HptRAMAdd	0x00	0x00	0x00
0xA0	0x41	HptRAMDataH	-	-	-
0xA0	0x42	HptRAMDataM	-	-	-
0xA0	0x43	HptRAMDataL	-	-	-
0xA0	0x50	ADCEn	0x00	0x00	0x00
0xA0	0x51	ADCCfg	0x00	0x00	0x00
0xA0	0x53	ADCDatAvg	0x00	0x00	0x00
0xA0	0x54	ADCDatMin	0x00	0x00	0x00
0xA0	0x55	ADCDatMax	0x00	0x00	0x00
0x50	0x00	ChipID	0x02	0x02	0x02
0x50	0x01	Status0	0x38	0x38	0x10
0x50	0x02	Status1	0x20	0x20	0x20
0x50	0x03	Status2	0x00	0x00	0x00
0x50	0x04	Status3	0x00	0x00	0x00
0x50	0x05	Status4	0x80	0x80	0x80
0x50	0x06	Int0	0x00	0x00	0x00
0x50	0x07	Int1	0x00	0x00	0x00
0x50	0x08	Int2	0x00	0x00	0x00
0x50	0x09	Int3	0x00	0x00	0x00
0x50	0x0A	IntMask0	0x00	0x00	0x00
0x50	0x0B	IntMask1	0x00	0x00	0x00
0x50	0x0C	IntMask2	0x00	0x00	0x00
0x50	0x0D	IntMask3	0x00	0x00	0x00
0x50	0x0F	ILimCntl	0x06	0x86	0x86
0x50	0x10	ChgCntl0	0x0D	0x27	0x27
0x50	0x11	ChgCntl1	0x73	0x65	0x61
0x50	0x12	ChgTmr	0xFD	0xE4	0xE4
0x50	0x13	StepChgCfg0	0x30	0x3F	0x3F
0x50	0x14	StepChgCfg1	0x07	0x17	0x17
0x50	0x15	ThmCfg0	0x3F	0x3F	0x3F
0x50	0x16	ThmCfg1	0x1F	0x1F	0x1F
0x50	0x17	ThmCfg2	0x1F	0x1F	0xDF
0x50	0x18	HrvCfg0	0x00	0x00	0x53
0x50	0x19	HrvCfg1	0x3F	0x3F	0x7F

Table 9. I²C Direct Register Defaults (continued)

SLAVE ADDRESS	REGISTER ADD	REGISTER NAME	EV KIT	MAX20360A	MAX20360B
0x50	0x1A	IVMONCfg	0x10	0x10	0x10
0x50	0x1B	Buck1Ena	0xE0	0xE0	0xE0
0x50	0x1C	Buck1Cfg0	0x50	0x50	0x50
0x50	0x1D	Buck1Cfg1	0x00	0x00	0x00
0x50	0x1E	Buck1Iset	0x00	0x00	0x00
0x50	0x1F	Buck1VSet	0x37	0x0F	0x19
0x50	0x20	Buck1Ctr	0x01	0x01	0x01
0x50	0x21	Buck1DvsCfg0	0x00	0x00	0x00
0x50	0x22	Buck1DvsCfg1	0x00	0x00	0x00
0x50	0x23	Buck1DvsCfg2	0x00	0x00	0x00
0x50	0x24	Buck1DvsCfg3	0x00	0x00	0x00
0x50	0x25	Buck1DvsCfg4	0x00	0x00	0x00
0x50	0x26	Buck1DvsSpi	0x00	0x81	0x00
0x50	0x27	Buck2Ena	0xE0	0x50	0x81
0x50	0x28	Buck2Cfg	0x51	0x00	0x50
0x50	0x29	Buck2Cfg1	0x00	0x00	0x00
0x50	0x2A	Buck2Iset	0x00	0x32	0x00
0x50	0x2B	Buck2VSet	0x32	0x02	0x32
0x50	0x2C	Buck2Ctr	0x02	0x00	0x02
0x50	0x2D	Buck2DvsCfg0	0x00	0x00	0x00
0x50	0x2E	Buck2DvsCfg1	0x00	0x00	0x00
0x50	0x2F	Buck2DvsCfg2	0x00	0x00	0x00
0x50	0x30	Buck2DvsCfg3	0x00	0x00	0x00
0x50	0x31	Buck2DvsCfg4	0x00	0x00	0x00
0x50	0x32	Buck2DvsSpi	0x00	0x00	0x00
0x50	0x34	Buck3Ena	0xE0	0x61	0x61
0x50	0x35	Buck3Cfg	0x51	0x51	0x51
0x50	0x36	Buck3Cfg1	0x00	0x40	0x40
0x50	0x37	Buck3Iset	0x00	0x00	0x00
0x50	0x38	Buck3VSet	0x35	0x1A	0x19
0x50	0x39	Buck3Ctr	0x04	0x04	0x04
0x50	0x3A	Buck3DvsCfg0	0x00	0x00	0x00
0x50	0x3B	Buck3DvsCfg1	0x00	0x00	0x00
0x50	0x3C	Buck3DvsCfg2	0x00	0x00	0x00
0x50	0x3D	Buck3DvsCfg3	0x00	0x00	0x00
0x50	0x3E	Buck3DvsCfg4	0x00	0x00	0x00
0x50	0x3F	Buck3DvsSpi	0x00	0x00	0x00
0x50	0x40	BBstEna	0xE0	0xE0	0xE0
0x50	0x41	BBstCfg	0x05	0x05	0x05
0x50	0x42	BBstVSet	0x32	0x32	0x32

Table 9. I²C Direct Register Defaults (continued)

SLAVE ADDRESS	REGISTER ADD	REGISTER NAME	EV KIT	MAX20360A	MAX20360B
0x50	0x43	BBstISet	0x00	0x00	0x00
0x50	0x44	BBstCfg1	0x13	0x13	0x13
0x50	0x45	BBstCtr0	0x08	0x08	0x08
0x50	0x46	BBstCtr1	0x00	0x00	0x00
0x50	0x47	BBstDvsCfg0	0x00	0x00	0x00
0x50	0x48	BBstDvsCfg1	0x00	0x00	0x00
0x50	0x49	BBstDvsCfg2	0x00	0x00	0x00
0x50	0x4A	BBstDvsCfg3	0x00	0x00	0x00
0x50	0x4B	BBstDvsSpi	0x00	0x00	0x00
0x50	0x51	LDO1Ena	0xE0	0xE0	0xE0
0x50	0x52	LDO1Cfg	0x01	0x03	0x03
0x50	0x53	LDO1VSet	0x00	0x36	0x34
0x50	0x54	LDO1Ctr	0x00	0x00	0x00
0x50	0x55	LDO2Ena	0xE0	0x41	0x41
0x50	0x56	LDO2Cfg	0x01	0x09	0x09
0x50	0x57	LDO2VSet	0x00	0x09	0x09
0x50	0x58	LDO2Ctr	0x00	0x00	0x00
0x50	0x59	LSW1Ena	0xE0	0xE0	0xE0
0x50	0x5A	LSWCfg	0x03	0x01	0x01
0x50	0x5B	LSW1Ctr	0x00	0x00	0x00
0x50	0x5C	LSW2Ena	0xE0	0xE0	0xE0
0x50	0x5D	LSW2Cfg	0x03	0x01	0x01
0x50	0x5E	LSW2Ctr	0x00	0x00	0x00
0x50	0x5F	ChgPmpEna	0xE0	0xE0	0xE0
0x50	0x60	ChgPmpCfg	0x03	0x03	0x03
0x50	0x61	ChgPmpCtr	0x00	0x00	0x00
0x50	0x62	BoostEna	0xE0	0xE0	0xE0
0x50	0x63	BoostCfg	0x0E	0x0E	0x0E
0x50	0x64	BoostISet	0x00	0x00	0x00
0x50	0x65	BoostVSet	0x1C	0x3C	0x3C
0x50	0x66	BoostCtr	0x00	0x00	0x00
0x50	0x67	MPC0Cfg	0x00	0x00	0x00
0x50	0x68	MPC1Cfg	0x00	0x00	0x00
0x50	0x69	MPC2Cfg	0x00	0x00	0x00
0x50	0x6A	MPC3Cfg	0x00	0x00	0x00
0x50	0x6B	MPC4Cfg	0x00	0x00	0x00
0x50	0x6C	MPC5Cfg	0x00	0x00	0x00
0x50	0x6D	MPC6Cfg	0x00	0x00	0x00
0x50	0x6E	MPC7Cfg	0x00	0x00	0x00
0x50	0x6F	MPCItrSts	0x00	0x06	0x06

Table 9. I²C Direct Register Defaults (continued)

SLAVE ADDRESS	REGISTER ADD	REGISTER NAME	EV KIT	MAX20360A	MAX20360B
0x50	0x70	BK1DedIntCfg	0x00	0x00	0x00
0x50	0x71	BK2DedIntCfg	0x00	0x00	0x00
0x50	0x72	BK3DedIntCfg	0x00	0x00	0x00
0x50	0x73	HptDedIntCfg	0x00	0x00	0x00
0x50	0x74	ADCDedIntCfg	0x00	0x00	0x00
0x50	0x75	USBOkDedIntCfg	0x00	0x00	0x00
0x50	0x78	LEDCommon	0x00	0x00	0x00
0x50	0x79	LED0Ref	0x00	0x00	0x00
0x50	0x7A	LED0Ctr	0x00	0x00	0x00
0x50	0x7B	LED1Ctr	0x00	0x00	0x00
0x50	0x7C	LED2Ctr	0x00	0x00	0x00
0x50	0x7D	PFN	0x01	0x01	0x01
0x50	0x7E	BootCfg	0xB9	0xB9	0xB9
0x50	0x7F	PwrCfg	0x01	0x01	0x01
0x50	0x80	PwrCmd	0x00	0x00	0x00
0x50	0x81	BuckCfg	0x38	0x00	0x00
0x50	0x83	LockMsk	0x00	0x00	0x00
0x50	0x84	LockUnlock	0x00	0x00	0x00
0x50	0x86	SFOUTCtr	0x81	0x81	0x81
0x50	0x87	SFOUTMPC	0x00	0x00	0x00
0x50	0x88	I2C_OTP_ADD	0x00	0x00	0x00
0x50	0x89	I2C_OTP_DAT	-	-	-

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX20360AEWZ+	-40°C to +85°C	72 WLP
MAX20360AEWZ+T	-40°C to +85°C	72 WLP
MAX20360BEWZ+*	-40°C to +85°C	72 WLP
MAX20360BEWZ+T*	-40°C to +85°C	72 WLP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/20	Release for Market Intro	—