Click here for production status of specific part numbers.

MAX20094/MAX20095 Backup Battery Charger and Boost Controller

General Description

The MAX20094/MAX20095 ICs combine a configurable constant-current/constant-voltage (CC/CV) battery charger with a high-efficiency synchronous boost controller to supply critical systems in the event the primary power source is lost. In addition, diagnostic features are available to check battery state-of-health (SOH) and IC functionality. Charging thresholds and the boost output voltage are configurable to support popular battery chemistries and a wide range of cell counts. To support system integration, the ICs have an I^2C slave port through which configuration and status bits can be accessed.

Switching frequency of 2.2MHz also helps to reduce system cost by minimizing inductor size. The ICs also include a precision battery SOH check and have built-in functionality to minimize leakage current out of the backup battery (BUB).

The MAX20094/MAX20095 are available in a 28-pin (5mm x 5mm) side-wettable TQFN package and are AECQ-100 qualified.

Applications

- Automotive Telematics Battery Backup
- Single or Multicell Battery-Backup Systems

Benefits and Features

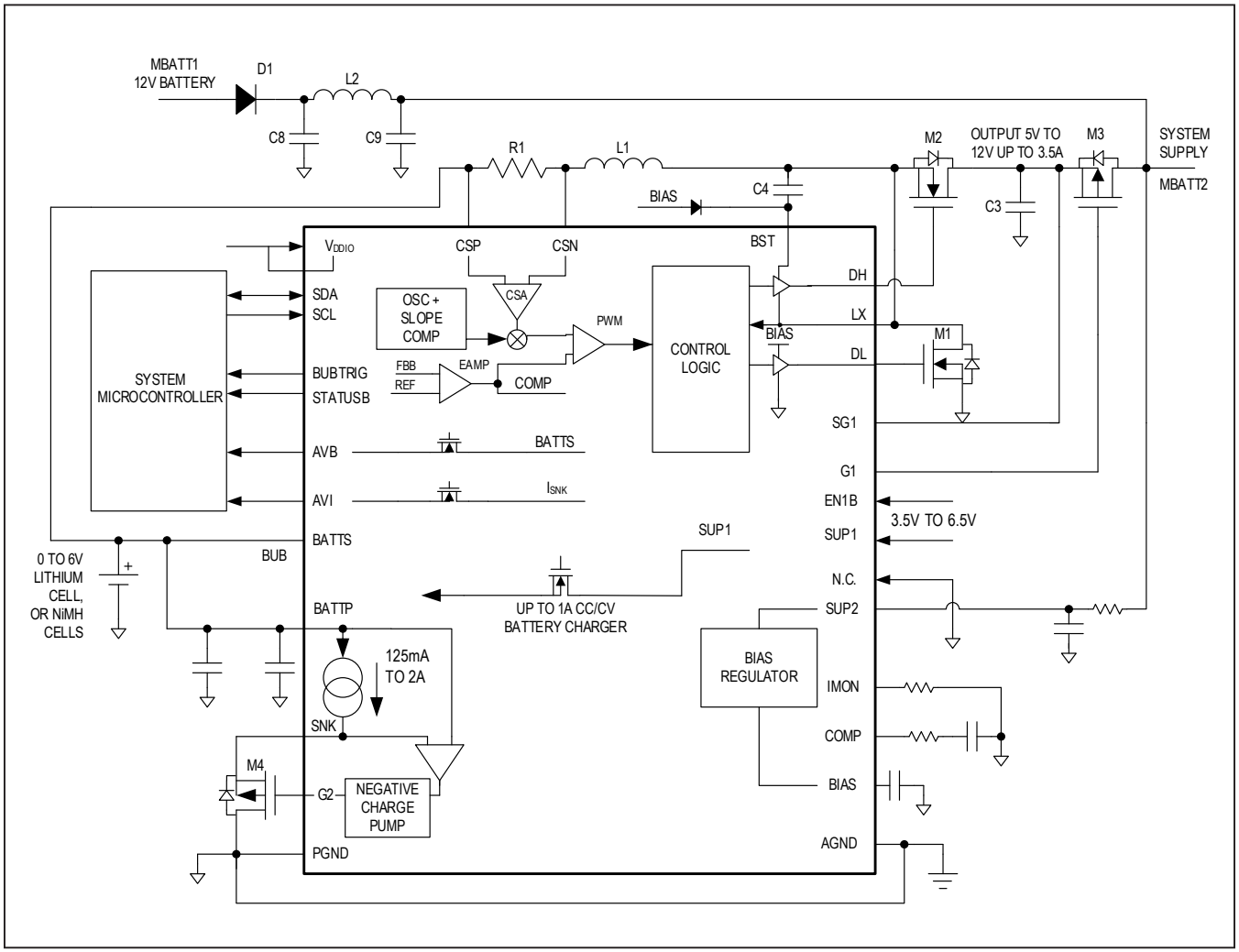
- Efficient Solution
  - Minimum 2V Sync Boost with n-Channel FET Control
  - Skip Mode Guarantees > 50% Efficiency at 1mA
- Multiple Functions to Enable Small Solution Size
  - 3V to 6V CC/CV Battery Charger
  - I^2C-Settable Charging Current Up to 1A
  - I^2C-Selectable CV Voltage and CC Current Levels
  - Gate-Driver Output for p-Channel Load Disconnect
  - Backup Battery Switchover-Trigger Signal
- State-of-Health for Backup Battery Monitoring
  - I^2C Interface Diagnostics and Control Interface
  - Accurate Internal Current Sink for Battery Impedance Measurement
  - Analog Readout of Internal Sink Current from Backup Battery
  - Remote Sense for BATT_ Voltage Measurement
- Robust for Automotive Environment
  - 3.5V to 36V V_{IN} (40V Load-Dump Tolerant)
  - < 1µA Leakage for Pins Connected to the Battery
  - -40°C to +125°C Operating Temperature Range
  - 28-Pin, Side-Wettable TQFN Package Enables Optical Inspection

***Ordering Information* appears at end of data sheet.**

19-100060; Rev 4; 1/20

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

SUP2, DH, LX, SG1, CSP, CSN to PGND.....-0.3V to +40V
G1 to SG1 .....-7.0V to +0.3V
BST to LX.....-0.3V to +6V
CSP to CSN .....-0.3V to +0.3V
AVI, BUBTRIG, DL, COMP, IMON to AGND.....-0.3V to V_{BIAS} + 0.3V
SCL, SDA to AGND..... -0.3V to V_{DDIO} + 0.3V
PGND to AGND.....-0.3V to +0.3V
EN1B, BIAS, VDDIO, STATUSB to AGND.....-0.3V to +6V
BATTP, SNK, BATTS, SUP1 to AGND.....-0.3V to +7.0V
AVB to AGND ..... -0.3V to V_{BATTS} + 0.3V
G2 to BATTP .....-6.0V to +0.3V
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -40°C to +150°C
Soldering Temperature (reflow).....+260°C
ESD Protection - Human Body Model.....±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28-Pin (5mm x 5mm x 0.75mm) Side-Wettable TQFN

PACKAGE CODE	T2855Y+5C
Outline Number	21-100130
Land Pattern Number	90-0027
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	3°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	35°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP1} = 4V, V_{SUP2} = 14V, V_{BATTP} = V_{BATTS} = 3.5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BOOST CONTROLLER						
Supply Voltage Range	V_{SUP2}	Normal operation	4.5		36	V
Supply Voltage Range		V_{SUP2} t < 1s			40	V
Undervoltage-Lockout Threshold	V_{CSP}	Contact factory for options			2	V
Shutdown Supply Current	I_{SUP2}	Boost disabled through I^2C, V_{SUP2} = 12V, V_{EN1B} = 0V			10	µA
Supply Current	I_{SUP2_STB}	BOOST I^2C bit enabled, V_{EN1B} = 0V, V_{SUP1} = 0 to 6V, V_{SUP2} = V_{SG1} = 14V, no switching		26	55	µA
Boost Mode Fixed-Output Voltage	V_{SUP2}	MAX20094ATIA	6.076	6.2	6.355	V
		MAX20094ATIB	6.37	6.5	6.663	
		MAX20094ATIC	6.664	6.8	6.97	
		MAX20094ATID	6.958	7.1	7.278	
		MAX20095ATIA	5.39	5.5	5.7	
		MAX20095ATIB	7.84	8	8.20	
		MAX20095ATIC	8.82	9	9.27	
		MAX20095ATID	9.8	10	10.25	
		MAX20095ATIE	11.76	12	12.30	
Boost Output Overvoltage-Falling Threshold (Boost Wakes Up Below this Threshold)	BOOST_OV_F		104	107	110.5	%
Boost Output Overvoltage-Falling Hysteresis				6		%
Boost Output Overvoltage-Rising Threshold (Boost Enters Sleep Mode Above this Threshold)	V_{SUP2_R}		110	113	116	%
Boost Undervoltage Lockout	BST_UVLO	Falling		65		%
		Rising		85		
Transconductance (from FBB to COMP)	g_m	V_{BIAS} = 5.5V (Note 2)		250		µS
G1 Drive Strength	G1	V_{SG1} = 6.8V, G1 not active		1.75		kΩ
G1 Activation Time		5nF MOSFET capacitance from SG1 to G1, OV falling until G1 reaches 4.5V below SG1; boost is ready to run within 10µs (typ) once BOOST_OV_F is tripped		10	50	µs
Dead Time		DL low to DH rising		20		ns
		DH low to DL rising		20		
Minimum On-Time	$t_{ON,MIN}$			120		ns
Minimum Off-Time	$t_{OFF,MIN}$			60		ns

Electrical Characteristics (continued)

(V_{SUP1} = 4V, V_{SUP2} = 14V, V_{BATTP} = V_{BATTS} = 3.5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM Switching-Frequency Range	f_{SW}		1.9	2.1	2.3	MHz
			0.36	0.4	0.44	
CS_ Current Limit	V_{LIMIT}	V_{CSP} - V_{CSN}	40	50	60	mV
LX Leakage Current		V_{LX} = V_{PGND} or V_{IN}, T_A = +25°C			1	µA
DH Pullup Resistance		V_{BIAS} = 5V, I_{DH} = -100mA		3	6	Ω
DH Pulldown Resistance		V_{BIAS} = 5V, I_{DH} = 100mA		1.5	3	Ω
DL Pullup Resistance		V_{BIAS} = 5V, I_{DL}= -100mA		3	6	Ω
DL Pulldown Resistance		V_{BIAS} = 5V, I_{DL}= 100mA		1.5	3	Ω
INTERNAL LDO BIAS						
Internal BIAS Voltage		V_{SUP2} > 6V		5		V
BIAS UVLO Threshold		V_{BIAS} rising		3.0	3.25	V
		V_{BIAS} falling	2.35	2.5		
BATTERY CHARGER						
Supply Voltage Range	V_{SUP1}		0		6.5	V
Supply Undervoltage Threshold, Falling	V_{SUP1_UV}		3.3			V
Supply Undervoltage Threshold, Rising	$V_{SUP1\_UV\_R}$				3.5	V
Supply Leakage Current	I_{SUP1}	Charger disabled, T_A = +25°C			10	µA
SUP1 to BATTP On-Resistance	R_{CHG}	V_{SUP1} = 3.5V, V_{BATTP} = 3.45V		250	500	mΩ
I²C Control BUB Voltage Setting	V_{CVTHR}	I²C control	3.0		6.0	V
BUB Voltage Range	$V_{BATT\_}$		0.0		6.0	V
Output-Voltage Accuracy	$V_{BATT\_}$	V_{CVTHR} = 3.6V	-1.2		+1	%
Fast-Charging Current Setting		I²C settable	0.05		1	A
Precharge Current		V_{BUB} = 0 to 2.0V	40	50	60	mA
Fast-Charge Current Accuracy		V_{SUP1} = 3.5V to 6.5V, 250mA < I_{FCHG} < 1A	-10		+10	%
		V_{SUP1} = 3.5V to 6.5V, 50mA < I_{FCHG} < 250mA	-20		+20	
Charger Restart-Voltage Threshold		Voltage drop below V_{CVTHR} for FAST_CHR_CC to resume		200		mV
Soft-Start Time		I²C enables the charger, fast-charge current of 90% of final value; EN1B going from high to low automatically enables the charger, as long as the I²C register is set			1	ms
BATTP Leakage Current	I_{BATTP}	Not boosting, and/or charger disabled, and/or unpowered ($V_{BATT\_}$ > V_{SUP1}), T_A = +25°C			1	µA

Electrical Characteristics (continued)

(V_{SUP1} = 4V, V_{SUP2} = 14V, V_{BATTP} = V_{BATTS} = 3.5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fast Shut-Off		V_{EN1B} = low to high, overrides I^2C, fast-charge current of < 50mA			5	µs
Minimum Charger Output Capacitance		Backup battery not present	1			µF
IMON Gain				440		A/A
Thermal-Limit Temperature	T_{LIM}	Junction temperature when the charge current is reduced, T_J rising		145		°C
THERMAL OVERLOAD						
Thermal-Shutdown Temperature		(Note 2)		170		°C
Thermal-Shutdown Hysteresis		(Note 2)		20		°C
BATTERY STATE-OF-HEALTH CURRENT SINK						
SNK Current Range	I_{SNK}	I^2C control	0		2	A
SNK Current Accuracy		I_{SNK} = 0.5A, $V_{BATT\_}$ = 3.3V	-10		+10	%
SNK Current-Measurement Accuracy	V_{AVI}	I_{SNK} = 0.5A, $V_{BATT\_}$ = 3.3V	-7.5	1	+7.5	%
Sink Current-Measurement Voltage Range	V_{AVI}	I_{SNK} = 0A to 2A	0		3	V
BUB Voltage-Measurement Range	V_{AVB}	V_{BATTS} = 0 to 6V	0		6	V
Resistance of AVB Pass Switch		BATT_ to AVB			10	Ω
G2 Drive-Current Capability	I_{G2}		7			µA
BATTS Leakage Current	I_{BATTS}	T_A = +25°C			1	µA
SNK Leakage Current	I_{SNK}	T_A = +25°C			1	µA
G2 Output Low Voltage	V_{G2_OL}	I_{G2_SINK} = 5µA			-3	V
BATTS Undervoltage Threshold, Falling					2.5	V
DIGITAL INPUT CHARACTERISTICS (SCL, SDA)						
Input High Threshold	V_{IH}	2.5V ≤ V_{DDIO} ≤ 5.5V	0.7 x V_{DDIO}			V
Input Low Threshold	V_{IL}	2.5V ≤ V_{DDIO} ≤ 5.5V			0.3 x V_{DDIO}	V
Input Threshold Hysteresis	V_{HYS}			0.15		V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DDIO}, T_A = +25°C			1	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL INPUT CHARACTERISTICS (EN1B)						
Input High Threshold	V_{IH}	2.5V ≤ V_{BIAS} ≤ 5.5V	1.4			V

Electrical Characteristics (continued)

(V_{SUP1} = 4V, V_{SUP2} = 14V, V_{BATTP} = V_{BATTS} = 3.5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Threshold	V_{IL}	2.5V ≤ V_{BIAS} ≤ 5.5V			0.5	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{BIAS}, T_A = +25°C			1	µA
DIGITAL OUTPUT CHARACTERISTICS (SDA, STATUSB, BUBTRIG)						
Output High Voltage	V_{OH}	Applies only to BUBTRIG CMOS output, I_{SOURCE} = 1mA	V_{BIAS} - 0.15	V_{BIAS} - 0.06		V
Output Low Voltage	V_{OL}	Applies to SDA, STATUSB, and BUBTRIG; I_{SNK} = 1mA			0.2	V
Output Inactive-Leakage Current	I_{OFF}	Applies only to STATUSB open-drain output (see I_{IN} for SDA)			±1	µA
Output Inactive Capacitance	C_{OFF}	Applies only to STATUSB open-drain output (see C_{IN} for SDA)			10	pF
Backup Battery-Trigger Pulse Width	$t_{BUBTRIG}$	BOOST enabled and SUP2 < BOOST_OV_F	180	200	220	ms
I²C-COMPATIBLE INTERFACE TIMING CHARACTERISTICS (SCL, SDA)						
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus-Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time for a Repeated START Condition	$t_{HD;STA}$		0.6			µs
SCL Pulse Width Low	t_{LOW}		1.3			µs
SCL Pulse Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU;STA}$		0.6			µs
Data Hold Time	$t_{HD;DAT}$		0		900	ns
Data Setup Time	$t_{SU;DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	Incoming signals (from master)	20 + C_B/10		300	ns
SDA and SCL Receiving Fall Time	t_F	Incoming signals (from master)	20 + C_B/10		300	ns
SDA Transmitting Fall Time	t_F		20 + C_B/10		250	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.6			µs
Bus Capacitance Allowed	C_B	2.5V ≤ V_{DDIO} ≤ 5.5V	0		900	pF
Pulse Width of a Suppressed Spike		Width of spikes that must be suppressed by the input filter of both SDA and SCL signals		50		ns

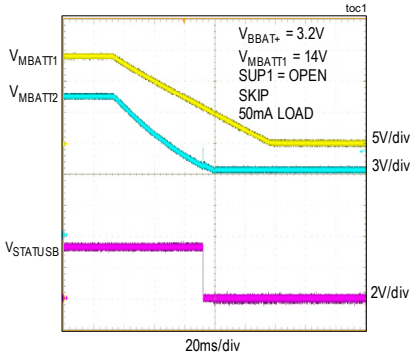
Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Guaranteed by design; not production tested.

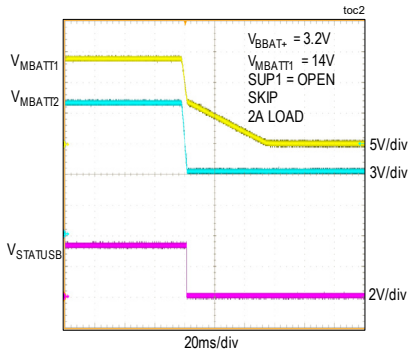
Typical Operating Characteristics

(V_{SUP1} = 4V, V_{SUP2} = 14V, V_{BATTP} = V_{BATTS} = 3.5V, T_A = +25°C, unless otherwise noted.)

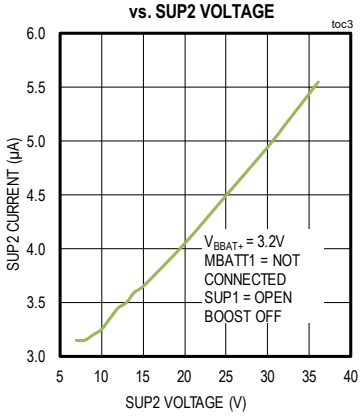
STARTUP INTO LIGHT LOAD



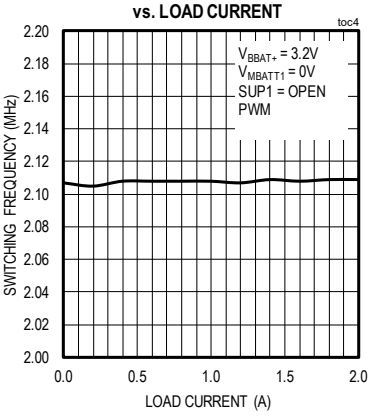
STARTUP INTO LOAD



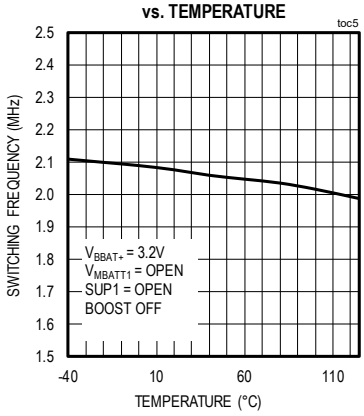
SUP2 SHUTDOWN CURRENT vs. SUP2 VOLTAGE



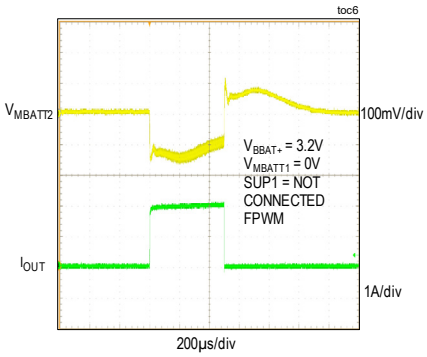
SWITCHING FREQUENCY vs. LOAD CURRENT



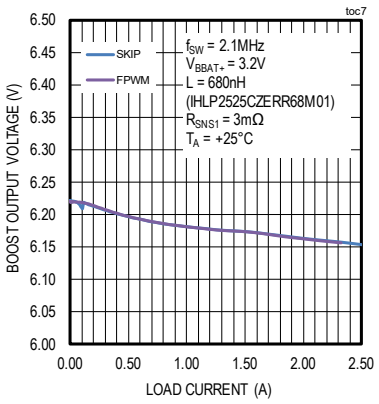
SWITCHING FREQUENCY vs. TEMPERATURE



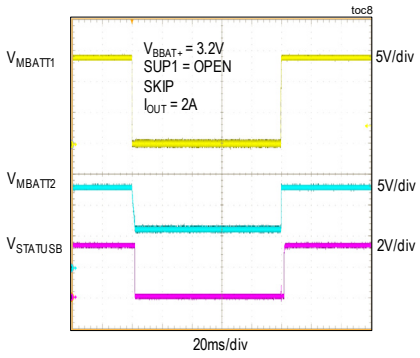
LOAD TRANSIENT



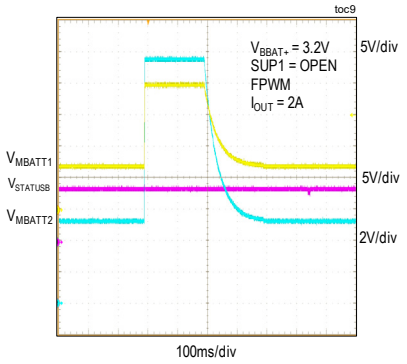
BOOST LOAD REGULATION



DIPS AND DROPS



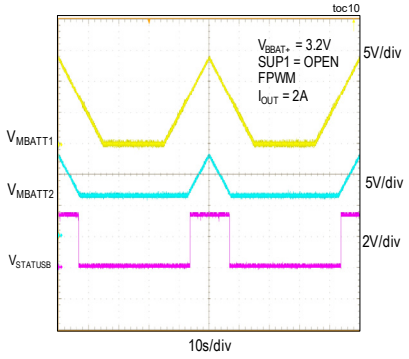
LOAD DUMP



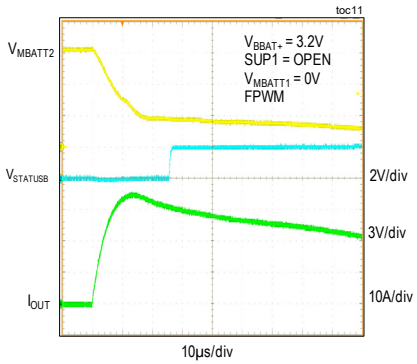
Typical Operating Characteristics (continued)

(V_{SUP1} = 4V, V_{SUP2} = 14V, V_{BATTP} = V_{BATTS} = 3.5V, T_A = +25°C, unless otherwise noted.)

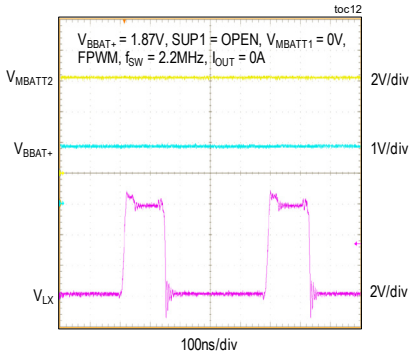
SLOW V_{IN} RAMP



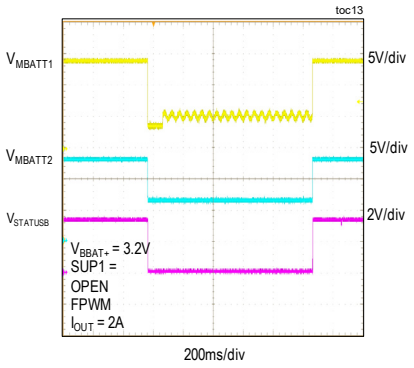
SHORT-CIRCUIT RESPONSE



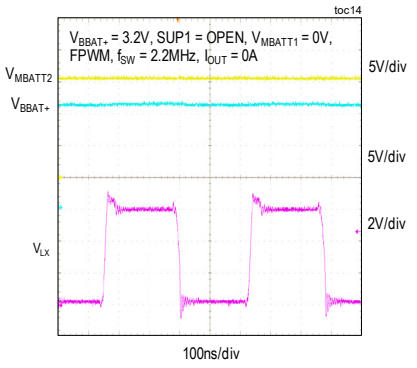
MINIMUM ON-TIME



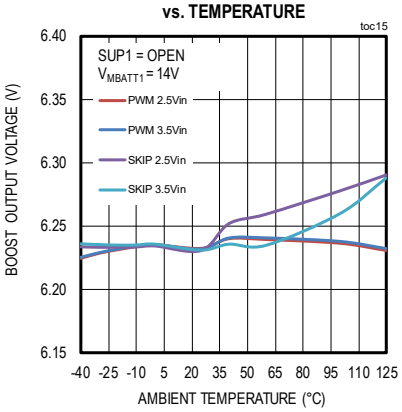
COLD CRANK



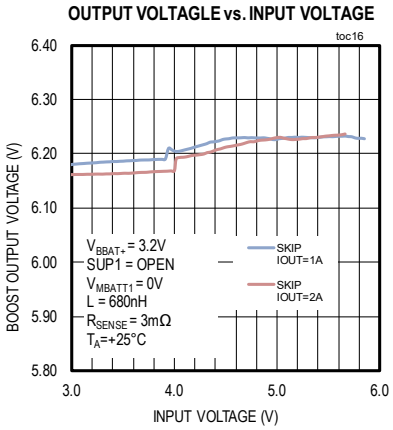
LX WAVEFORM



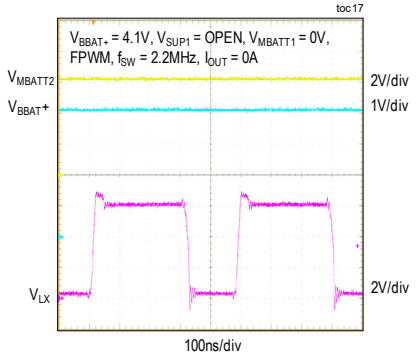
BOOST OUTPUT VOTLAGE vs. TEMPERATURE



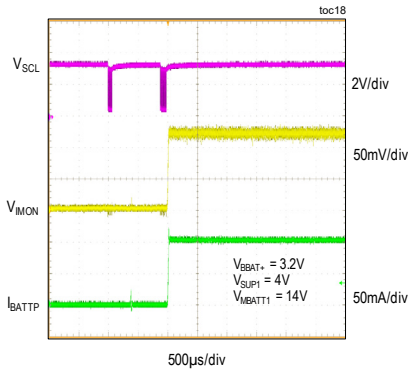
OUTPUT VOLTAGLE vs. INPUT VOLTAGE



MINIMUM OFF-TIME



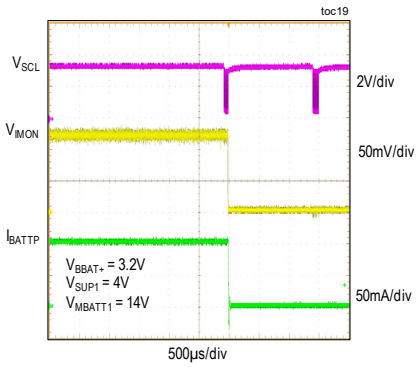
CHARGER STARTUP



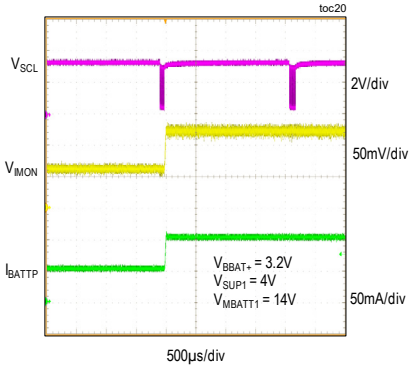
Typical Operating Characteristics (continued)

(V_{SUP1} = 4V, V_{SUP2} = 14V, V_{BATTP} = V_{BATTS} = 3.5V, T_A = +25°C, unless otherwise noted.)

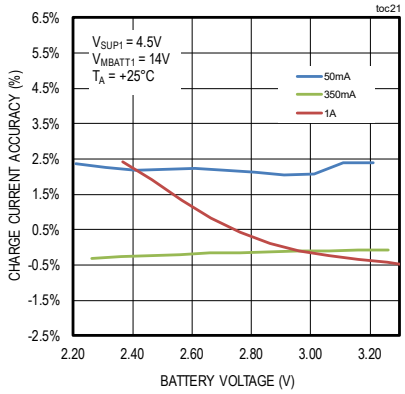
CHARGER SHUTDOWN



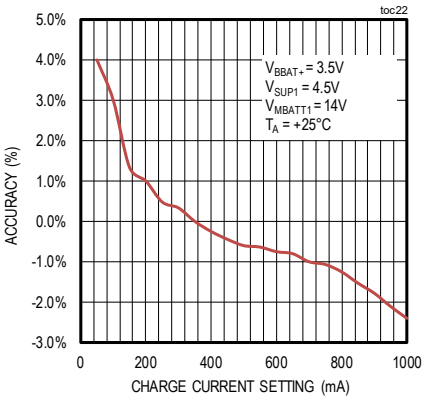
CHARGER CURRENT CHANGE



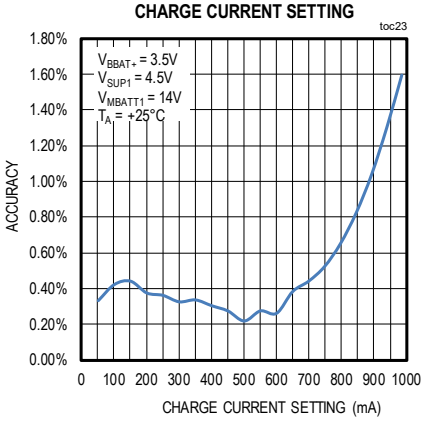
CHARGE CURRENT ACCURACY vs. BATTERY VOLTAGE



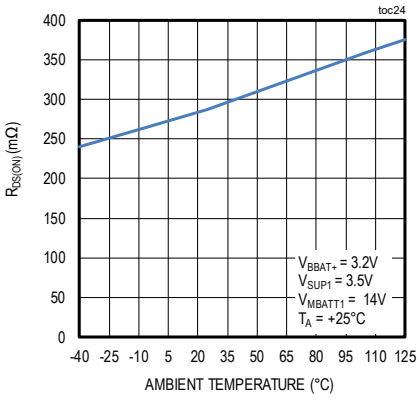
CHARGE CURRENT ACCURACY vs. SETTING



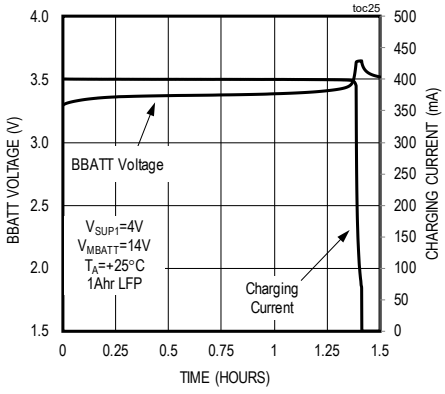
IMON ACCURACY vs. CHARGE CURRENT SETTING



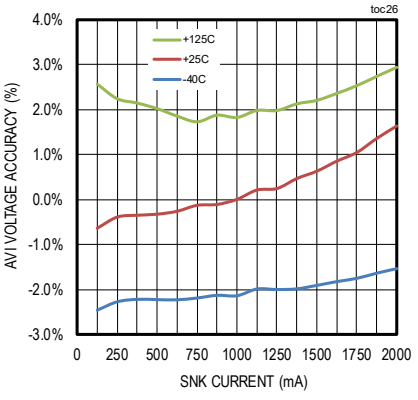
IMON VOLTAGE vs. CHARGE CURRENT



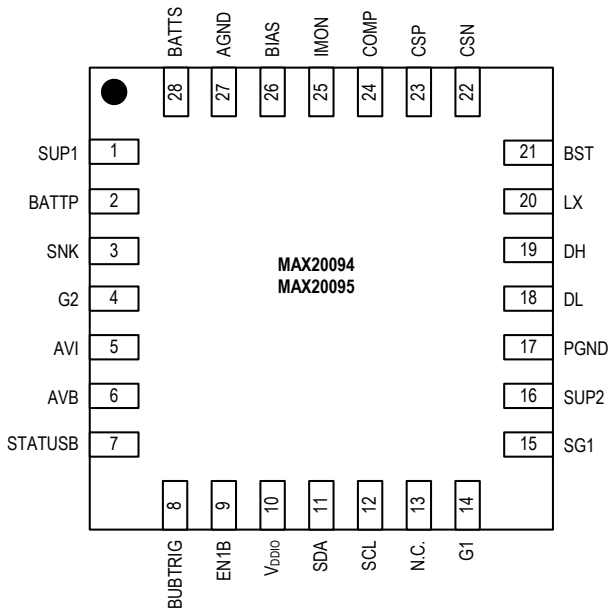
CHARGING PROFILE



AVI VOLTAGE ACCURACY vs. SNK CURRENT



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	SUP1	Input to the CC/CV Charger. Connect a 2.2µF ceramic capacitor from SUP1 to the ground plane.
2	BATTP	Charger Output for the Backup Battery (BUB). BATTP is the current sink for the battery state-of-health (SOH) check. Place a 10µF, 2.2µF, and 0.1µF ceramic capacitor as close as possible to the SUP2 pin. See the *PCB Layout Recommendations* section for details on trace sizing to BATTP.
3	SNK	Connection for the Source of the External MOSFET (M4) for State-of-Health (SOH) Measurements. The SNK pin sinks the preset current from the BUB to the external MOSFET during SOH measurements.
4	G2	Gate Drive to Turn On the MOSFET (M4) and Sink Current Into the IC. This function is controlled by I^2C. G2 is not connected when the discharger is disabled. When the discharger is enabled, G2 is driven to BATTP for 62µs (typ) before the circuit starts up.
5	AVI	Analog Voltage Measurement for SNK Current Set During SOH Measurement. There is a 30kΩ pulldown resistor when AVI is disabled.
6	AVB	Analog Battery Voltage-Measurement Output During SOH Measurements. There is a 60kΩ pulldown resistor connected 10µs before the AVB switch is turned off through I^2C.
7	STATUSB	STATUSB (Battery Boost) Default Open-Drain Output. Driven to AGND during boost operation due to loss of primary power; otherwise, high impedance.
8	BUBTRIG	Backup Battery-Active Timed Output. Driven to BIAS for 200ms following backup boost controller start of operation; otherwise, driven to AGND.
9	EN1B	Charger Disable. EN1B is connected to ground during normal operation. If pulled high, the charger is disabled, regardless of the I^2C register setting.

Pin Description (continued)

PIN	NAME	FUNCTION
10	VDDIO	I²C Logic Interface Supply Voltage, 2.5V to 5.5V. Connect to the I²C bus supply.
11	SDA	I²C Data Signal
12	SCL	I²C Clock Input
13	N.C.	Connect to GND in the Application
14	G1	High-Side p-Channel MOSFET (M3) Driver. There is a 188kΩ resistor between G1 and SG1.
15	SG1	Source of the External p-Channel MOSFET (M3). SG1 and G1 control the gate drive of external MOSFET M3.
16	SUP2	System Supply Voltage Input. High-voltage-tolerant input to the LDO, which generates 5V supply for the IC. Connect a resistor and capacitor filter from the battery-filtered rail and SUP2. See the *Applications Information* section for more details.
17	PGND	Power Ground Pin. Connect directly to the PCB ground plane.
18	DL	Low-Side MOSFET Driver Output. Connect to the gate of the boost converter's low-side MOSFET.
19	DH	High-Side MOSFET Driver Output. Connect to the boost converter's high-side MOSFET.
20	LX	Switching Node of DC-DC Controller
21	BST	Boosted Supply Voltage for the High-Side Sync MOSFET Gate Drive
22	CSN	Current-Sense Resistor, Inductor-Side Sense Point. Connect CSN as close as possible to the current-sense resistor terminal. See the *PCB Layout Recommendations* section for details on proper layout.
23	CSP	Current-Sense Resistor Input Pin. Connect CSP as close as possible to the current-sense resistor for accurate current sensing. See the *PCB Layout Recommendations* section for details on proper layout.
24	COMP	Loop-Compensation Component Connection Pin. COMP is the output of the internal g_m amplifier. Connect a resistor in series with a capacitor to the AGND pin. The component values are selected according to the data sheet recommendations.
25	IMON	Connect IMON to GND with a 500Ω Resistor. $V_{IMON} = (I_{CHG}/440) \times 500\Omega$. Max $R_{IMON} = (V_{BATTP(MIN)} - 0.25)/(0.0025I_{CHG}) - 200$.
26	BIAS	Supply Pin for the Internal IC Circuits. This pin should be decoupled with a 2.2µF capacitor. BIAS is the output of the LDO connected to the $V_{SUP\_}$ pin, and is used to supply the internal circuitry with 5V.
27	AGND	Analog Ground. Low-noise ground for precision circuit blocks.
28	BATTS	Battery Voltage-Sensing Input. Senses the battery voltage for the voltage-feedback loop and routes to the internal analog switch. Connect BATTS as close as possible to the battery's positive terminal for the most accurate voltage sensing of the battery.
—	EP	Exposed Pad

Detailed Description

The MAX20094/MAX20095 ICs combine a configurable constant-current/constant-voltage (CC/CV) battery charger, with a high-efficiency synchronous boost controller to supply critical systems in the event the primary power source is lost. In addition, diagnostic features are available to check battery state-of-health (SOH) and IC functionality. Charging thresholds and the boost output voltage are configurable to support popular battery chemistries and a wide range of cell counts. To support system integration, the ICs have an I²C slave port through which configuration and status bits can be accessed.

BIAS Linear Regulator

An internal 5V linear regulator (BIAS) generates a bias supply for the internal circuitry. Bypass BIAS with a 2.2µF or greater ceramic capacitor to guarantee stability under the full-load condition.

The BIAS input undervoltage-lockout (UVLO) circuitry inhibits boost operation, charging, or SOH if the 5V bias supply (BIAS) is below its 2.5V (typ) UVLO falling threshold. Once the 5V bias supply (BIAS) rises above its UVLO rising threshold and the block control logic conditions are met, the ICs are functional.

Block Control Logic

The logic governing the operation of the boost controller, battery charger, and SOH is summarized in Table 1.

Logic Equations

STATUSB Pin

The STATUSB pin is an open-drain, active-low nMOS output pin that can be used in a shared-interrupt configuration with a µC master, and any number of similarly configured slave devices (using a wired-OR configuration with an external pullup resistor to a suitable supply, typically V_{DDIO}). Under default conditions, the STATUSB pin is active when the boost is actively regulating SUP2. The function of the STATUSB pin can be changed to provide other types of operation using the I²C interface (see the GEN_STATUS and EN_INT registers).

Charger Block

The normal operating mode of the ICs is to maintain charge on the backup battery (BUB). This function is provided by the charger block.

Table 1. Block Control Logic

BLOCK	COMMENTS
SOH	SOH is enabled when: ● I²C register bit is set, and ● Boost is not regulating, and ● Not in thermal-shutdown condition
Boost	Boost is enabled/regulating when: ● I²C register bit is set, and ● SUP2 is below OV_F threshold ● Not in thermal-shutdown condition **Note:**When boost is regulating, SOH and charger functions are disabled.
Charger	Charger is enabled when: ● I²C register bit is set and EN1B pin = 0 ● Boost is not regulating, and ● Not in thermal-shutdown condition **Note:** While enabled, the charger mode progression is controlled by an internal state machine and associated comparators.

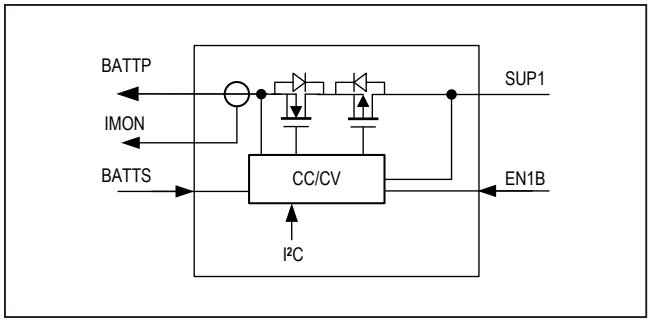


Figure 1. Charger Block Diagram

Charger State Machine Description

Once enabled, the charger operation is governed by a state machine, described below and detailed in Figure 2. The real-time operation of the charger can be read back using the CHGR_STATUS (01\h) register.

The charger is held in an OFF state when CONTROL/CHG_EN=0, or START_BIASRDY=0, or the die temperature is above the thermal-shutdown threshold. Once CONTROL/CHG_EN=1, bias has been established (START_BIASRDY=1) and the die temperature is below the thermal-shutdown threshold (START_THMSD=0), the charger moves to standby mode, and a 15µS timer is started, allowing the charger's internal biases and comparators to settle.

The charger remains in standby mode until internal biases are established (based on the startup timer) and supply conditions are checked and found to be valid. The charger returns to standby mode in the event of an invalid supply condition. Supply conditions can be verified in real time using the CHGR_STATUS (01\h) register. A supply condition alert is also available in GEN_STATUS (02\h).

The charger next moves to a 50mA current-limited charging mode (PREQUAL). The charger remains in this mode until V_{BUB} exceeds V_{PQVTHR}, which is factory set to 2V. Contact the factory for different settings.

The charger now begins the fast-charging procedure, beginning in a constant-current mode (FAST_CHG_CC). Charge current is programmed using the CHGR_CC (05\h) register. The charger remains in fast charging until V_{BUB} exceeds V_{CVTHR} and returns to FAST_CHG_CC if V_{BUB} falls below V_{CVTHR}, which is selected using the CHGR_CV (06\h) register.

When V_{BUB} exceeds V_{CVTHR}, the charger continues charging in a constant-voltage mode **(**FAST_CHG_CV). A constant-voltage-mode alert is available in GEN_STATUS (02\h), notifying the user that charging is nearing completion. Once the charger has moved to FAST_CHG_CV mode, the charger current is monitored. If I_{CHG} falls below 50mA, the fast-charging operation is completed and the charger moves to FAST_CHG_DONE mode. The charger remains in this mode until it is disabled by the user (returning to OFF), a supply fault condition occurs (returning to STANDBY), or V_{BUB} falls below V_{CVTHR} - 200mV (returning to FAST_CHG_CC). After entering the DONE state, a charging-done alert is available in GEN_STATUS (02\h), notifying the user that charging is completed.

If V_{SUP1} and V_{BUB} enter dropout, the charge current is reduced due to the $R_{DS(ON)}$ of the internal MOSFET, and the voltage difference between V_{SUP1} and the battery. If charge current continues to decrease, the ALRT_CV and CHGR_MODE changes to show CV state. Once charge current reduces to 50mA, ALRT_CV remains 1, ALRT_DONE=1, and CHGR_MODE goes to the DONE state. Use the following equation to estimate the amount of headroom required to stay out of dropout at maximum ambient temperature:

$$V_{Drop\_CHG} = 1.15 \times R_{CHG\_MAX} \times I_{FAST\_CHG\_CC}$$

where R_{CHG_MAX} is the maximum value of R_{CHG} from the *Electrical Characteristics* table.

When CONTROL/CHG_EN=0, then CHRG_STATUS/SUP1_UVLO=1. This default condition is due to internal circuitry being turned off to minimize leakage.

EN1B Pin

The EN1B pin is an active-low input port that controls the operation of the charger block. When the EN1B pin is held low, the charger operation is controlled by the I^2C interface registers. When pulled high (usually due to an external system fault), the charger is instantly disabled and its internal state machine reset. The charger resumes normal operation once the pin is returned low.

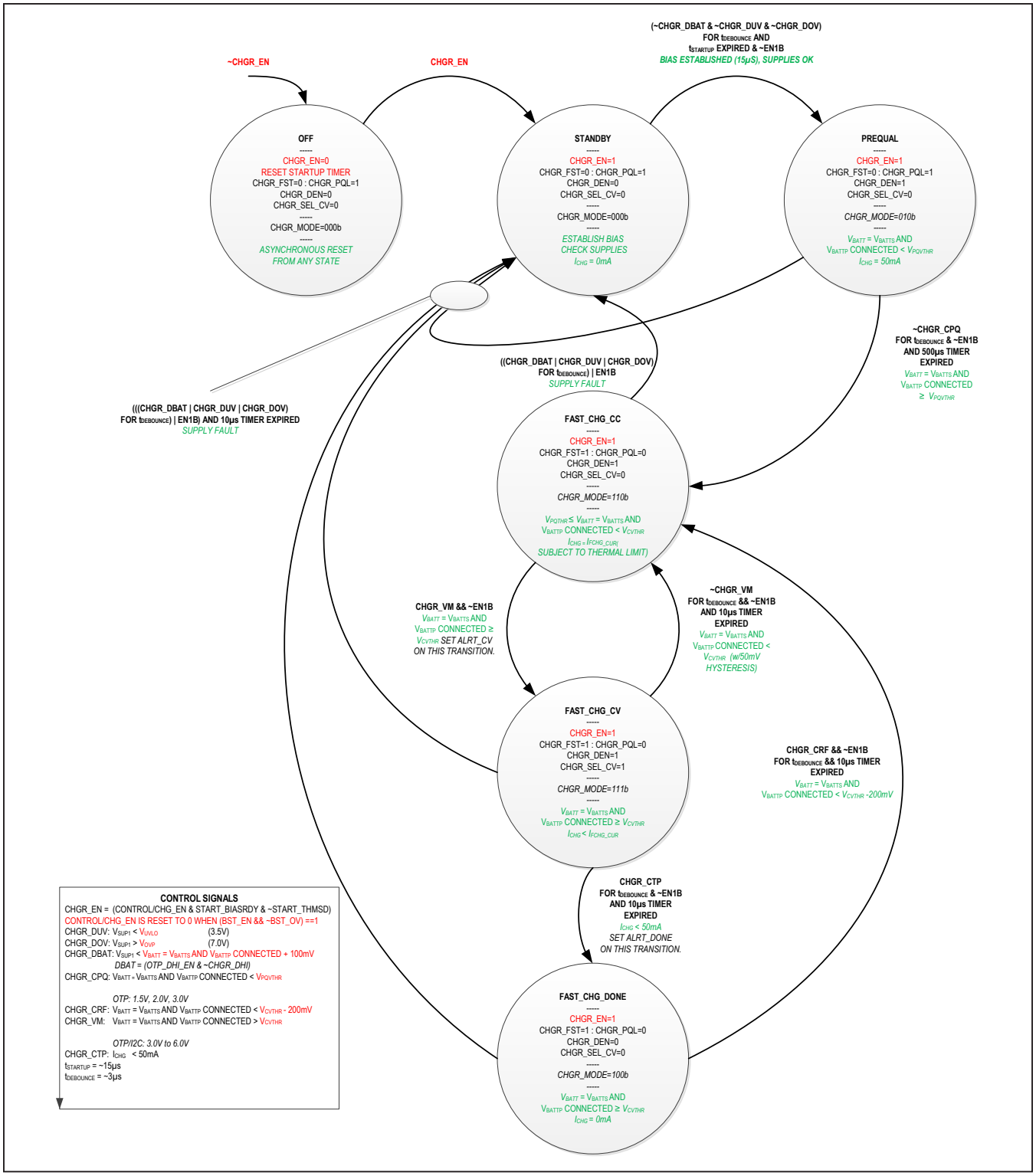


Figure 2. Charger State Machine Diagram

Boost Block

The boost block allows the ICs to maintain a regulated supply voltage on the SUP2 pin using the backup battery (BUB) in the event of a main-battery failure.

The boost is a synchronous current-mode controller with a factory-preset output voltage. The switching frequency is capable of greater than 2MHz. To enable longer battery life, the boost utilizes pulse-frequency modulation (PFM) mode at light load and automatically enters ultra-low I_Q standby mode when output voltage is above the required boost voltage. The boost automatically enters awake mode when the output voltage is at or near the required boost voltage, and sends a discrete signal to the host to indicate it has awakened.

Standby Current

The ICs have low standby supply current, as mentioned in the *Electrical Characteristics* table, but still allow for 250µs (max) quick turn-on time once V_{SUP2} falls below BST_OV_F. I^2C settings are held during the low-standby mode. In this mode, MOSFET M3 (see Figure 3) is OFF until the boost's overvoltage (OV) falling threshold triggers, and then it turns ON.

BUBTRIG Pin

BUBTRIG is an active-low, 200ms one-shot CMOS output used to indicate the start of a period of active regulation by the boost block. When the boost is enabled and begins regulating (due to V_{SUP2} falling below the BOOST_OV_F voltage threshold), BUBTRIG is asserted high for 200ms before going low again (even if the boost block continues regulation duties beyond 200ms). BUBTRIG is not asserted again unless the boost block exits active regulation mode and later resumes regulation activity.

Current Limit

A current-sense resistor ($R_{CS\_}$), connected to the CSP and CSN pins, sets the current limit of the boost converter. The CS_ input has a voltage trip level (V_{LIMIT}) of 50mV (typ). The low 50mV current-limit threshold reduces the power dissipation in the current-sense resistor. Use a current-sense filter to reduce noise in the current-sense path (see the *Shunt Resistor Selection* section).

Skip Operation

Skip mode is enabled with BST_SKIP=1. The transition from pulse-width modulation (PWM) to skip mode occurs as load current is reduced and LX current drops below zero crossing and eventually reaches t_{ON_MIN}. Once

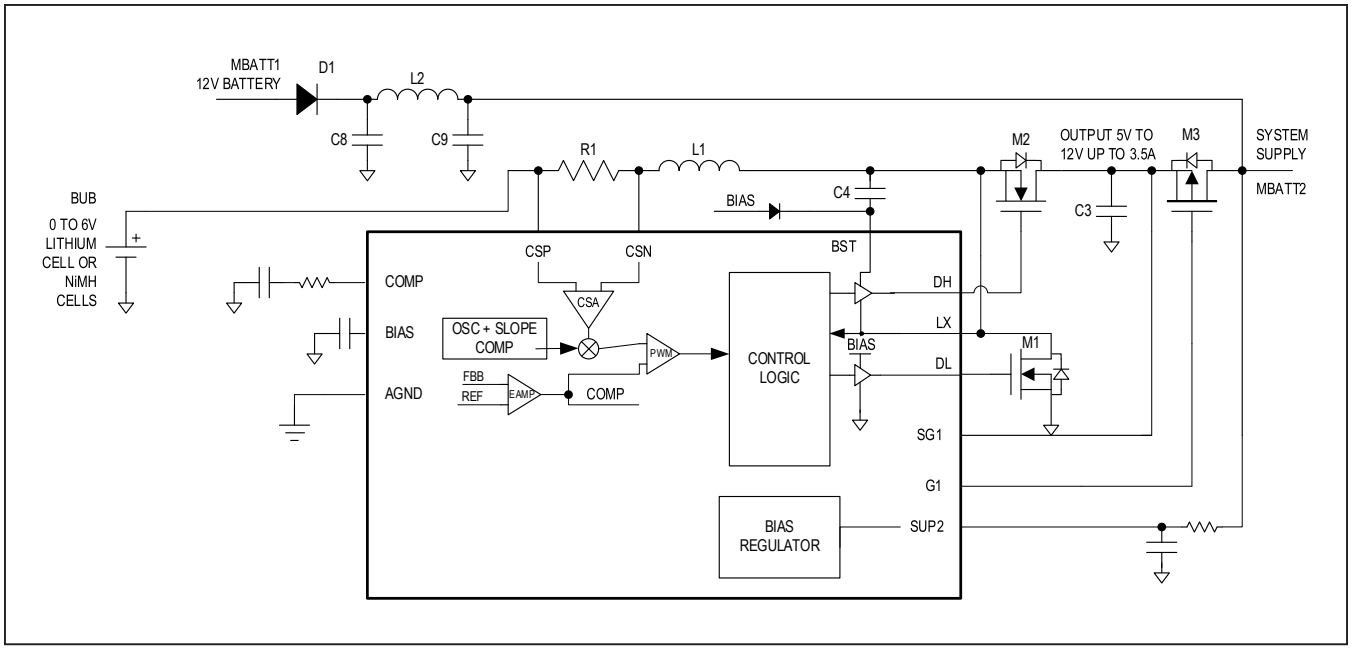


Figure 3. Boost Block Diagram

zero crossing and one cycle of t_{ON_MIN} are reached, the controller enters skip mode. Transition back to PWM mode occurs when there is 480ns of t_{ON_MIN} and the output voltage stays too low, so PWM control resumes to bring output voltage back into regulation.

State-of-Health Block

The state-of-health (SOH) block (see Figure 4) allows the ICs to test the backup battery (BUB) under current-load conditions to aid in determining the condition of the BUB based on output impedance. During the test, the output voltage of the battery, as well as a voltage representation of the current applied, are made available for ADC measurements. When V_{BUB} is less than 2.5V, the SOH discharger is disabled and the SOH_ILIM status bit is set to 1, indicating that a fault has occurred. The SOH sink current setting is the SOH (07/h) register. SOH is enabled by setting CONTROL/SOH_EN. Selection between the hardware-default and register-override values are set by CONTROL/SOH_OVR.

AVB Switch

The AVB switch passes the BATTS sense voltage to the AVB pin. This allows voltage monitoring of the BUB. Resistance of the AVB pass switch is defined in the *Electrical Characteristics* table.

AVI Switch

The AVI switch is an analog output representing the sink current during the SOH measurement. V_{AVI} typically reads 1.5V/A of SOH current.

I²C Interface

Communication with the ICs is achieved using an I²C-compatible serial interface. This interface allows the user to configure and monitor the operation of the device.

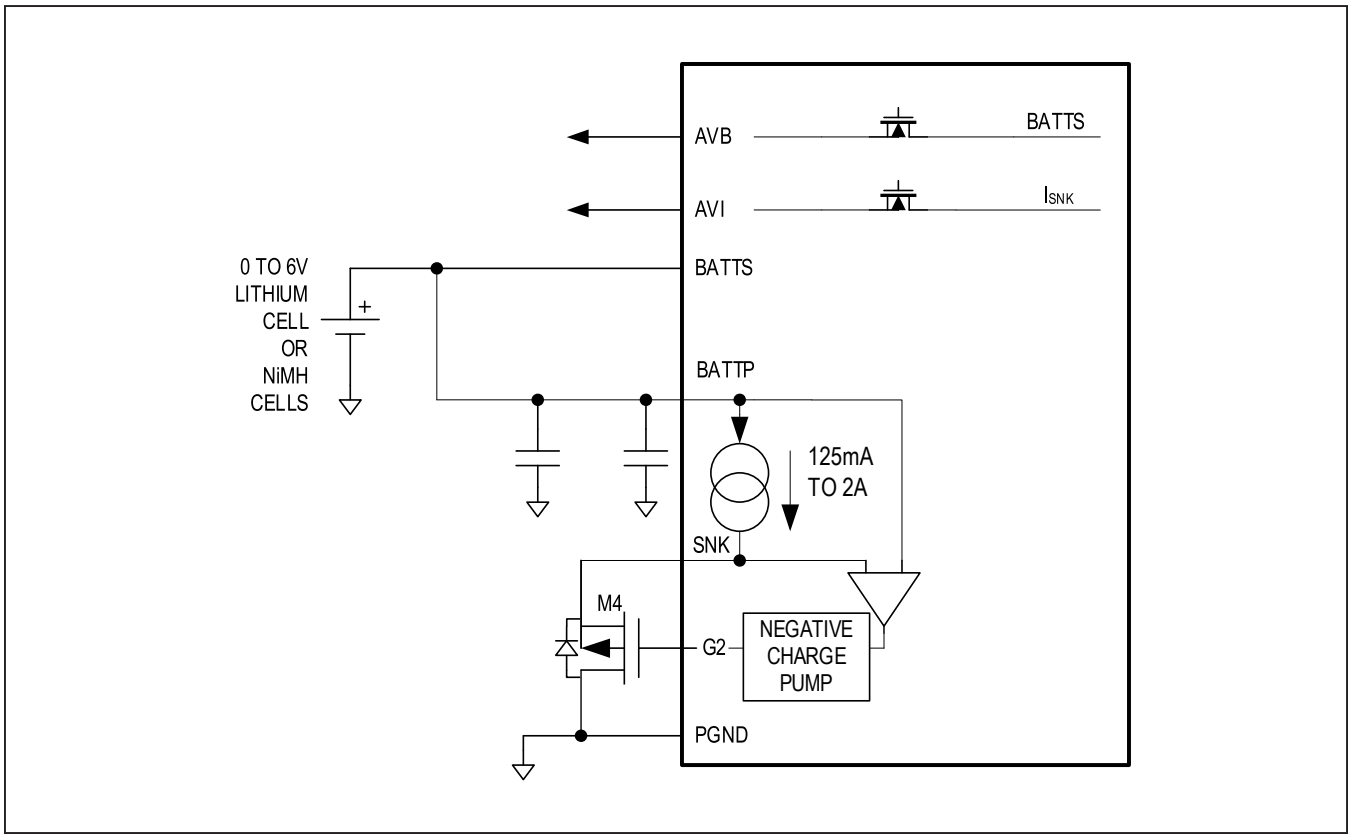


Figure 4. State-of-Health Block Diagram

Serial Addressing

The I2C port operates as slave devices, which send and receive data through an I2C-/SMBus-compatible 2-wire serial interface. The interface uses a serial-data access (SDA) line and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s) devices. A master (typically a microcontroller) initiates all data transfers to the port and generates the SCL clock that synchronizes the data transfer.

The SDA line operates as both an input and an open-drain output. The SDA line requires a pullup resistor (4.7kW, typ). The port's SCL line operates only as an input. The SCL line requires a pullup resistor (4.7kW, typ) if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START (S) condition sent by a master, followed by the core's 7-bit slave address plus the NOP/W bit, one command/register byte, one data byte, and a STOP (P) condition.

I2C Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *I2C START and STOP Conditions* section).

I2C START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the beginning of a transmission to the device. The master terminates transmission, and frees the bus, by issuing a STOP condition.

The bus remains active if a Repeated START condition is generated instead of a STOP condition; this is often used in combined-format read operations. See Figure 5 for examples that show the generation and proper use of START (S), STOP (P), and Repeated START (Sr) conditions.

I2C Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit the device uses for handshake receipt of each byte of data when in write mode. The device pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows the detection of unsuccessful data transfers that occur if a receiving device is busy, or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the device is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge (NACK) is sent when the master reads the final byte of data from the device, followed by a STOP (P) condition.

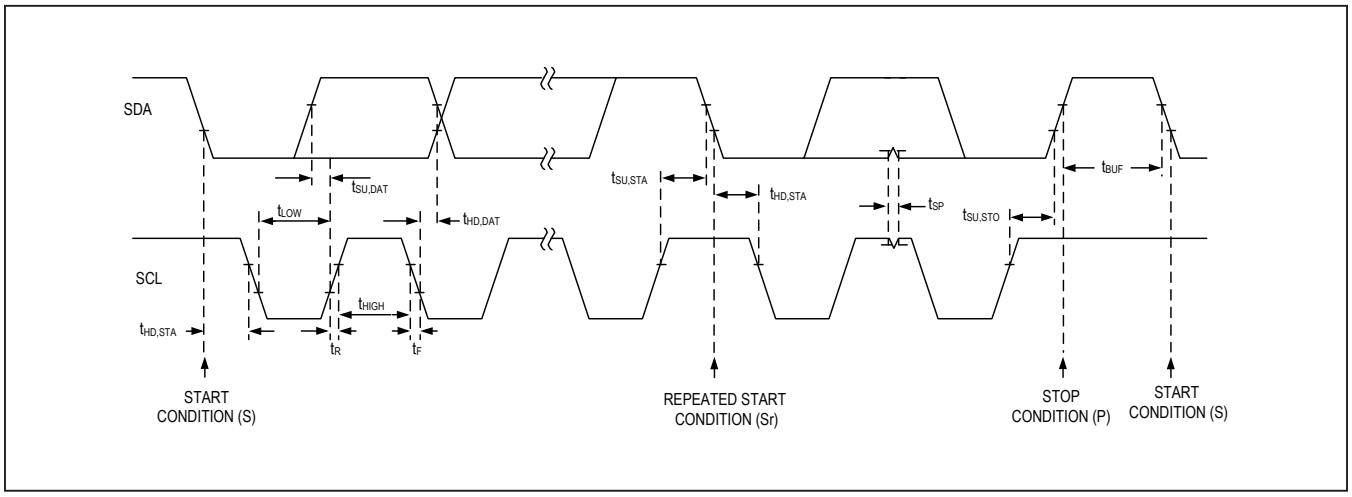


Figure 5. I2C Serial-Interface Timing Diagram

I²C Command and Data Bytes

A command byte follows the slave address. A command byte is typically followed by one or two data bytes unless it is the last byte in the transmission, as would be the case for readback operations (see Figure 5). If data bytes follow the command byte, the command byte indicates the address of the register that should receive the data bytes that follow. The data bytes are stored in a temporary register and then transferred to the appropriate register during the ACK periods between bytes.

I²C Write Operations

A master device communicates with the device by transmitting the proper slave address, followed by a register/command and data word(s). Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each byte is 8 bits long and is always followed by an acknowledge (ACK) clock pulse, as shown in Figure 6. The first byte contains the address of the device, with R/$\overline{W}$ = 0 to indicate a write. The second byte contains the register (or command) to be written, and the third byte contains the data to be written.

I²C Read Operations

The ICs support standard combined-format I²C read-mode operations. Each receive sequence is again framed by a START (S) or Repeated START (Sr) condition and a STOP (P). Each byte is 8 bits long and is always followed by an ACK clock pulse, as shown in Figure 7. The first byte contains the address of the device, with R/$\overline{W}$ = 0 to indicate a write. The second byte contains the register that is to be read back. There is now a Repeated START (Sr) condition, followed by the device address, with R/$\overline{W}$ = 1 to indicate a read and an acknowledge (ACK) clock. The master still has control of the SCL line, but the device takes over the SDA line. The fourth byte in the frame contains the register data readback followed by a STOP (P) condition.

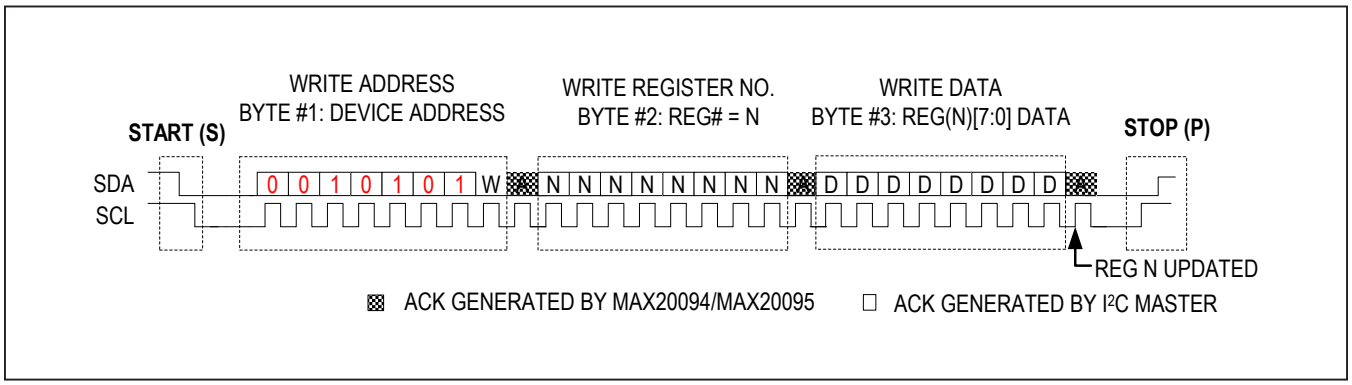


Figure 6. I²C Write Sequence

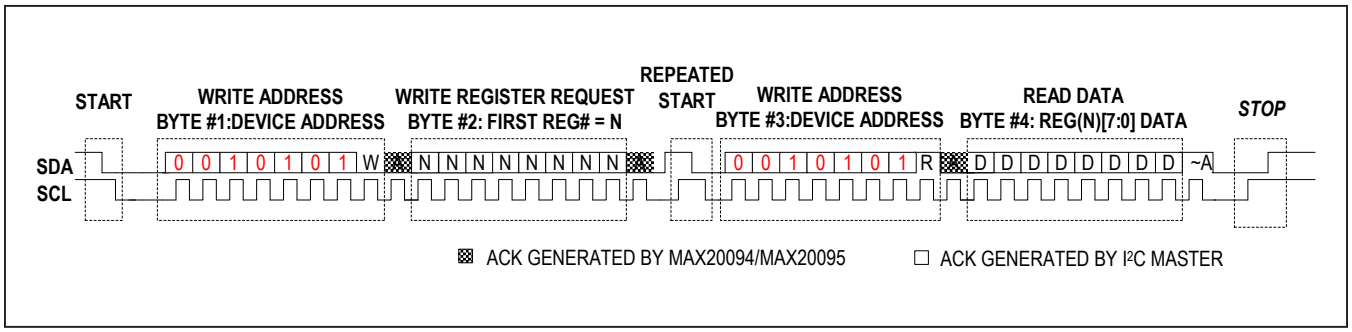


Figure 7. I²C Read Sequence

I²C User Command and Register Map

ADDRESS	NAME	MSB							LSB
USER COMMANDS									
0x00	CHIP_ID[7:0]	DIE_TYPE[7:0]							
0x01	CHGR_STATUS[7:0]	CHGR_EN	CHGR_MODE[2:0]			–	SUP1_UVLO	SUP1_OVP	SUP1_BATT
0x02	GEN_STATUS[7:0]	BOOST	ALRT_BST	ALRT_CV	ALRT_DONE	ALRT_SUP1	THRM_LIM	THRM_SD	SOH_ILIM
0x03	EN_INT[7:0]	EN_BST	EN_ABST	EN_ACV	EN_ADN	EN_ASP	EN_TLIM	EN_TSD	EN_SOHI
0x04	CONTROL[7:0]	SOH_EN	SOH_OVR	AVI_EN	AVB_EN	CHG_EN	CHG_IMON	BST_EN	BST_SKIP
0x05	CHGR_CC[7:0]	–	–	–	FCHG_CUR[4:0]				
0x06	CHGR_CV[7:0]	–	–	–	VCVTHR[4:0]				
0x07	SOH[7:0]	ISINK[3:0]				REG_ISINK[3:0]			
0x08	SW_RST[7:0]	All_Zeros[7:0]							
0xFF	NO_OP[7:0]	Dont_Care[7:0]							

CHIP_ID (0x00)

CHIP_ID is a read-only register that provides information on the chip and silicon revision.

BIT	7	6	5	4	3	2	1	0
Field	DIE_TYPE[7:0]							
Reset	0x02 for MAX20094 and 0x03 for MAX20095							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DIE_TYPE	7:0	DIE_TYPE provides information on the chip and silicon revision.

CHGR_STATUS (0x01)

CHGR_STATUS is a read only register that provides information on the Charger operating mode and related Supply1 voltage status.

BIT	7	6	5	4	3	2	1	0
Field	CHGR_EN	CHGR_MODE[2:0]			–	SUP1_ UVLO	SUP1_OVP	SUP1_ BATT
Reset					–			
Access Type	Read Only	Read Only			–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
CHGR_EN	7	0 = Disabled: CONTROL/CHG_EN=0, or BIAS is below UVLO threshold. 1 = Enabled: CONTROL/CHG_EN=1, and BIAS is above UVLO threshold.
CHGR_MODE	6:4	0b000 = Disabled/standby 0b010 = Prequalify-Charging Mode: $V_{BATT\_} < V_{PQVTHR}$, I_{CHG} = 50mA 0b110 = Fast-Charging Constant Current (CC) Mode: $V_{PQVTHR} \leq V_{BATT\_} < V_{CVTHR}$, $I_{CHG} = I_{FCHG\_CUR}$ 0b111 = Fast-Charging Constant Voltage (CV) Mode: $V_{BATT} \geq V_{CVTHR}$, $I_{CHG} < I_{FCHG\_CUR}$ 0b100 = Fast-Charging Done Mode: $V_{BATT\_} \geq V_{CVTHR}$ and I_{CHG} < 50mA, I_{CHG} = 0mA **Notes:** CHGR_MODE[2] = FAST_CHARGE: Indicates charging is controlled by the fast-charge state progression. CHGR_MODE[1] = BATT_CHARGE: Indicates battery is currently being charged. CHGR_MODE[0] = CV_CHARGE: Indicates the fast-charge progression has reached the CV mode. States 001, 011, 101 are not used.
SUP1_UVLO	2	0 = V_{SUP1} > 3.5V 1 = V_{SUP1} < 3.5V **Note:** 1 when CHG_EN=0.
SUP1_OVP	1	0 = V_{SUP1} < 7.0V 1 = V_{SUP1} > 7.0V
SUP1_BATT	0	0 = V_{SUP1} > ($V_{BATT\_}$ + 100mV) 1 = V_{SUP1} < ($V_{BATT\_}$ + 100mV)

GEN_STATUS (0x02)

GEN_STATUS is a read-only register that provides information on the status and operation of all internal blocks within the ICs. The contents of the GEN_STATUS register can be individually selected for inclusion in the STATUS/INTB interupt term using the EN_INT register.

BIT	7	6	5	4	3	2	1	0
Field	BOOST	ALRT_BST	ALRT_CV	ALRT_ DONE	ALRT_ SUP1	THRM_LIM	THRM_SD	SOH_ILIM
Reset								
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
BOOST	7	0 = Disabled: CONTROL/BST_EN = 0, or $V_{SUP2} > V_{BOOST\_OV\_F}$ 1 = Enabled: CONTROL/BST_EN = 1 and $V_{SUP2} < V_{BOOST\_OV\_F}$ **Note:** Boost threshold is set through OTP.
ALRT_BST	6	0 = Boost has not been activated since the last read. 1 = Boost has been activated since last the read. **Edge-Set, Clear-on-Read:** Once read, this alert is cleared until the boost is deactivated and reactivated. Real-time boost activity can be monitored using D7.
ALRT_CV	5	0 = Charger has not reached fast-charge CV mode since the last read. 1 = Charger has reached fast-charge CV mode since the last read. **Edge-Set, Clear-on-Read:** Onceread, this alert is cleared until the charger exits and reenters the CV state.
ALRT_DONE	4	0 = Charger has not reached fast-charge-done mode since the last read. 1 = Charger has reached fast-charge-done mode since the last read. **Edge-Set, Clear-on-Read:** Onceread, this alert is cleared until the charger exits and reenters the done state.
ALRT_SUP1	3	0 = Supply1 conditions allow normal charger operation. 1 = One or more supply status indicators is active. **Level-Set, Clear-on-Read:** Once read, this alert is cleared if the supply condition has been resolved. Individual supply faults can be read back using CHGR_STATUS.
THRM_LIM	2	0 = Charger is not operating, or is operating normally. 1 = Charger is operating in a thermally limited (reduced-current) mode (> 135°C). **Level-Set, Clear-on-Read:** Once read, this alert is cleared if the thermal-limit condition has been resolved.
THRM_SD	1	0 = Device is operating normally. 1 = Device thermal protection is engaged (> 170°C). **Level-Set, Clear-on-Read:** Onceread, this alert is cleared if the thermal-shut-down condition has been resolved.
SOH_ILIM	0	0 = SOH is not operating, or is operating normally (I_{SNK} < 3A, or V_{BATTP} > undervoltage threshold). 1 = SOH is operating in overcurrent condition ($I_{SNK} \geq$ 3A, or V_{BATTP} < under-voltage threshold when SOH is enabled). **Level-Set, Clear-on-Read:** Once read, this alert is cleared if the overcurrent condition, or BATTP undervoltage condition has been resolved.

EN_INT (0x03)

EN_INT is a read/write register that governs the operation of the STATUSB output pin. The content of this register determines which interrupt input terms are included in the interrupt output OR term (e.g., a '1' in an EN_INT register indicates that the corresponding input term is included in the STATUS interrupt output OR term). See the GEN_STATUS register for detailed descriptions of the interrupt terms.

BIT	7	6	5	4	3	2	1	0
Field	EN_BST	EN_ABST	EN_ACV	EN_ADN	EN_ASP	EN_TLIM	EN_TSD	EN_SOHI
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
EN_BST	7	0 = BOOST status is not included in the STATUS OR term. 1 = BOOST status is included in the STATUS OR term.
EN_ABST	6	0 = ALRT_BST status is not included in the STATUS OR term. 1 = ALRT_BST status is included in the STATUS OR term.
EN_ACV	5	0 = ALRT_CV status is not included in the STATUS OR term. 1 = ALRT_CV status is included in the STATUS OR term.
EN_ADN	4	0 = ALRT_DONE status is not included in the STATUS OR term. 1 = ALRT_DONE status is included in the STATUS OR term.
EN_ASP	3	0 = ALRT_SUP1 status is not included in the STATUS OR term. 1 = ALRT_SUP1 status is included in the STATUS OR term.
EN_TLIM	2	0 = THRM_LIM status is not included in the STATUS OR term. 1 = THRM_LIM status is included in the STATUS OR term.
EN_TSD	1	0 = THRM_SD status is not included in the STATUS OR term. 1 = THRM_SD status is included in the STATUS OR term.
EN_SOHI	0	0 = SOH_ILIM status is not included in the STATUS OR term. 1 = SOH_ILIM status is included in the STATUS OR term.

CONTROL (0x04)

CONTROL is a read/write register that enables/disables device features.

BIT	7	6	5	4	3	2	1	0
Field	SOH_EN	SOH_OVR	AVI_EN	AVB_EN	CHG_EN	CHG_IMON	BST_EN	BST_SKIP
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SOH_EN	7	0 = SOH disabled, G2 driven to BATTP. 1 = SOH enabled, G2 driven to achieve I_{SNK} (V_{BATTP} to AGND - 3V). **Notes:** This bit is reset to 0 when the boost controller is actively regulating (BST_EN=1 and SUP2 < BST_OV_F threshold). This bit is reset to 0 when SOH current limit is true, or V_{BATTP} is undervoltage.
SOH_OVR	6	0 = Use Hardware default value, ISINK[3:0] = OTP_ISINK[3:0]. 1 = Use override value, ISINK[3:0] = REG_ISINK[3:0]. **Note:** This bit allows toggling between the OTP and REG settings of ISINK.
AVI_EN	5	0 = Switch off. 1 = Switch on.
AVB_EN	4	0 = Switch off. 1 = Switch on.
CHG_EN	3	0 = Charger disabled. 1 = Charger enabled (if EN1B is also low). **Notes:** The register value is programmed and read back in this location; the AND term showing the charger-enable status is available as CHGR_STATUS/CHGR_EN. This bit is reset to 0 when the boost controller is actively regulating (BST_EN=1 and SUP2 < BST_OV_F threshold).
CHG_IMON	2	0 = Internally shunting current. 1 = Current is sent to the IMON pin (monitoring current .externally).
BST_EN	1	0 = Boost controller disabled. 1 = Boost controller enabled. **Notes:** This bit is reset to 0 if all the following conditions are true: - boost controller is actively regulating (BST_EN=1 and SUP2 < BST_OV_F threshold). - SUP2 < 4.5V (BST_UV threshold).
BST_SKIP	0	0 = Disable boost skip-mode operation. 1 = Enable boost skip-mode operation.

CHGR_CC (0x05)

CHGR_CC is a read/write register that sets the fast-charge current during constant-current operation.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FCHG_CUR[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
FCHG_CUR	4:0	FCHG_CUR sets the fast-charge current between 50mA and 1000mA in 50mA steps 0b00000 = 50mA 0b00001 = 100mA 0b00010 = 150mA ... 0b10001 = 900mA 0b10010 = 950mA 0b10011 = 1000mA ... 0b11111 = 1000mA **Notes:** Prior to initial write, FCHG_CUR reads back the factory-default setting. The reset value is determined by OTP (0b00000 = 50mA).

CHGR_CV (0x06)

CHGR_CV is a read/write register that sets the charger regulation voltage required to shift to constant-voltage operation.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	VCVTHR[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
VCVTHR	4:0	VCVTHR sets the charger regulation between 3.0V and 6.0V in 100mV steps: 0b00000 = 3.0V 0b00001 = 3.1V 0b00010 = 3.2V ... 0b11100 = 5.8V 0b11101 = 5.9V 0b11110 = 6.0V 0b11111 = 7.0V **Note:** The reset value is determined by OTP (0b00110=3.6V).

SOH (0x07)

SOH is a read/write register that sets the user-programmable sink current during state-of-health (SOH) measurements. Enabling of SOH is accomplished by setting CONTROL/SOH_EN. Current selection between hardware-default and register-override values is set by CONTROL/SOH_OVR (Reg03\h, D6 and D5, respectively). Writes to this register are only required to modify the register-override value, REG_ISINK[3:0]. To support dual-current measurements, this register should be written before the override value is used. Readback of the SOH register returns the ISINK[3:0] value currently in use (read only, depending on the value of CONTROL/SOH_OVR), and the user-programmed value of REG_ISINK[3:0] (for verification).

BIT	7	6	5	4	3	2	1	0
Field	ISINK[3:0]				REG_ISINK[3:0]			
Reset					0b0000			
Access Type	Read Only				Write, Read			

BITFIELD	BITS	DESCRIPTION
ISINK	7:4	If CONTROL/SOH_OVR = 0, OTP_ISINK[3:0] is returned. If CONTROL/SOH_OVR = 1, REG_ISINK[3:0] is returned. 0b0000 = 125mA.
REG_ISINK	3:0	REG_ISINK sets the discharger's current regulation between 125mA and 2A in 125mA steps: 0b0000 = 125mA 0b0001 = 250mA 0b0010 = 375mA ... 0b1101 = 1.750A 0b1110 = 1.875A 0b1111 = 2A

SW_RST (0x08)

SW_RST (software reset) is a write-only register/command that resets the entire part to its original default conditions at the end of the I2C SW_RST transaction (i.e., the data-byte ACK). Execution only occurs if DIN[7:0]=0x00. The effect of a SW_RST is identical to power-cycling the part.

BIT	7	6	5	4	3	2	1	0
Field	All_Zeros[7:0]							
Reset	0b00000000							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
All_Zeros	7:0	

NO_OP (0xFF)

NO_OP (no-operation register) is a read-write register that has no internal effect on the part. If this register is read back, SDA remains zero for I2C readback data. Any attempt to write to this register is ignored, without impact to internal operation.

BIT	7	6	5	4	3	2	1	0
Field	Dont_Care[7:0]							
Reset	0x00							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
Dont_Care	7:0	

Applications Information

Boost Converter

Boost switching current is sensed by R1 in the *Simplified Block Diagram*. During large loads, the limits of the CSN, CSP, and the headroom available on the amplifier need to be observed. The V_{LIMIT} is shown in the *Electrical Characteristics* table. For a 0.003Ω (typ) sense resistor and 40mV (min) V_{LIMIT}, the peak inductor current is 13.3A. As the BUB is depleted of charge, the CSP pin voltage decreases. When the undervoltage lockout on CSP is disabled, the CSP low voltage for minimum headroom is 1.5V (typ), assuming 100mΩ battery ESR and $3.2V_{BUB}$.

Inductor Selection

Duty cycle and frequency are important to calculate the inductor size, as the inductor current ramps up during the on-time of the switch and ramps down during its off-time. A higher switching frequency generally improves transient response and reduces component size; however, if the boost components are used as the input filter components during nonboost operation, low frequency becomes advantageous.

The duty-cycle range of the boost converter depends on the effective input-to-output voltage ratio. In the following calculations, the duty cycle refers to the on-time of the boost MOSFET:

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{BUB(MIN)}}{V_{OUT(MAX)}}$$

or including the voltage drops across the inductor, MOSFET ($V_{ON,FET}$):

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{BUB(MIN)} + I_{OUT} \times R}{V_{OUT(MAX)}}$$

where:

$$R = R_{DC} + R_{DSON\_M2} + R_{DSON\_M3}$$

The ratio of the inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good initial value is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and elected LIR determine the inductor value as follows:

$$L[\mu H] = \frac{V_{IN} \times D}{f_{SW}[MHz] \times LIR}$$

where:

$$D = (V_{OUT} - V_{IN})/V_{OUT}$$

V_{IN} = Typical input voltage

V_{OUT} = Typical output voltage

$$LIR = 0.3 \times I_{OUT}/1 - D$$

Select the inductor with a saturation current rating higher than the peak-switch current limit of the converter:

$$I_{L,\,PEAK} > I_{L,\,MAX} + \frac{\Delta I_{L,\,RIP,\,MAX}}{2}$$

Running a boost converter in continuous-conduction mode introduces a right-half-plane zero into the transfer function. To avoid the effect of this right-half-plane zero, the crossover frequency for the control loop should be ≤ 1/3 x f_{RHP_ZERO}. If faster bandwidth is required, a smaller inductor and higher switching frequency is recommended.

MOSFET Selection

The key selection parameters for choosing the n-channel MOSFET used in the boost converter follow.

Threshold Voltage

The boost's n-channel MOSFET must be a logic-level type with guaranteed on-resistance specifications at V_{GS} = 4.5V.

Current Capability

The n-channel MOSFET must deliver the input current ($I_{IN(MAX)}$):

$$I_{IN(MAX)} = I_{LOAD(MAX)} \times \frac{D_{MAX}}{1 - D_{MAX}}$$

Choose MOSFETs with the appropriate average current at V_{GS} = 4.5V.

Input Capacitor Selection

The BUB provides the voltage on the input and some stability to transients, but can include a wiring harness or series resistance. Add a 10µF, 2.2µF, and 0.1µF X7R ceramic capacitor at the BATTP input of the MAX20094. Review the MAX20094 Evaluation Kit schematic and PCB layout with the factory to optimize the input capacitors.

The input current for the boost converter is continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and the maximum ESR using the following equations:

$$C_{BUB} = \frac{\Delta I_L \times D}{4 \times f_{SW} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where:

$$\Delta I_L = \frac{\left(V_{BUB} - V_{DS}\right) \times D}{L \times f_{SW}}$$

V_{DS} is the total voltage drop across the external MOSFET, plus the voltage drop across the inductor ESR. ΔI_L is the peak-to-peak inductor ripple current as calculated above. ΔV_Q is the portion of input ripple due to the capacitor discharge and ΔV_{ESR} is the contribution due to ESR of the capacitor. Assume the input capacitor-ripple contribution due to ESR (ΔV_{ESR}) and capacitor discharge (ΔV_Q) are equal when using a combination of ceramic and aluminum capacitors. During the converter turn-on, a large current is drawn from the input source, especially at a high output-to-input differential.

Output Capacitor Selection

In a boost converter, the output capacitor supplies the load current when the boost MOSFET is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak-to-peak:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT}}$$

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

I_{OUT} is the load current in A, f_{SW} is in MHz, C_{OUT} is in µF, ΔV_Q is the portion of the ripple due to the capacitor discharge, and ΔV_{ESR} is the contribution due to the ESR of the capacitor. D_{MAX} is the maximum duty cycle at the minimum input voltage. Use a combination of low-ESR ceramic, and high-value low-cost aluminum capacitors for lower output ripple and noise.

Shunt Resistor Selection

The current-sense resistor ($R_{CS\_}$), connected between the battery and the inductor, sets the current limit. The CS_ input has a voltage trip level ($V_{CS\_}$) of 50mV (typ). Set the current-limit threshold high enough to accommodate the component variations. Use the following equation to calculate the value of $R_{CS\_}$:

$$R_{CS\_} = \frac{V_{CS\_}}{I_{IN(MAX)}}$$

where $I_{IN(MAX)}$ is the peak current that flows through the MOSFET at full load and minimum V_{IN}.

$$I_{IN(MAX)} = I_{LOAD(MAX)} / \left(1 - D_{MAX}\right)$$

When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (DL) quickly terminates the on-cycle.

Input Filter for SUP2

An input filter consisting of a 10µF capacitor and 100mΩ resistor is suggested. SUP2 current is approximately 50mA for boost applications in FPWM mode, 300µA in skip mode, and 26µA in standby mode. For charger and SOH applications, SUP2 current is approximately 1mA.

PCB Layout Recommendations

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (see Figure 5). When possible, mount all power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more.

- Minimize current-sensing errors by connecting CSP and CSN. Use kelvin sensing directly across the current-sense resistor ($R_{CS\_}$).
- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (SUP2, CSP, and CSN).

PCB Layout Procedure

- Place the power components first, with ground terminals adjacent (low-side FET, C_{IN}, C_{OUT}, and Schottky). If possible, make all these connections on the top layer with wide, copper-filled areas.
- Mount the controller IC adjacent to the low-side MOSFET (preferably on the back side opposite NL_ and NH_) to keep LX, GND, DH_, and the DL_ gate-drive lines short and wide. To keep the driver impedance low, and for proper adaptive dead-time sensing, the DL_ and DH_ gate traces must be short and wide (50 mils to 100 mils), if the MOSFET is 1in from the controller IC.
- Group the gate-drive components (BST_ diode and capacitor and LDO bypass capacitor, BIAS) together as close as possible to the controller IC. Be aware that gate currents of up to 1A flow from the bootstrap capacitor to BST_, from DH_ to the gate of the external HS switch, and from the LX pin to the inductor. Dimension those traces accordingly.
- Make the DC-DC controller ground connections, as shown in the MAX20094 EV kit component placement guide (see Figure 8). This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go, and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly under the IC.
- Connect the output power planes directly to the output filter capacitor's positive and negative terminals with multiple vias, and place the entire DC-DC converter circuit as close as possible to the load.

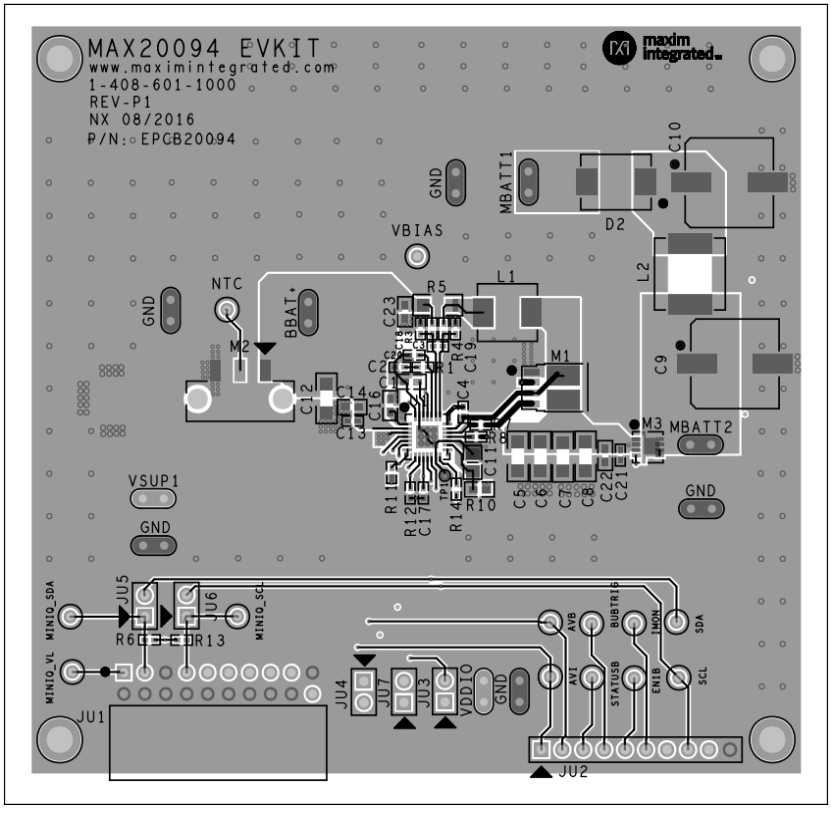


Figure 8. MAX20094 EV Kit Component Placement Guide/PCB Layout

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	f_{SW}	V_{OUT}	BUB_UVLO
MAX20094ATIA/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	6.2V	On
MAX20094ATIB/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	6.5V	On
MAX20094ATIC/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	6.8V	On
MAX20094ATID/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	7.1V	On
MAX20094ATIE/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	400kHz	6.2V	On
MAX20095ATIA/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	5.5V	On
MAX20095ATIB/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	8V	On
MAX20095ATIC/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	9V	On
MAX20095ATID/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	10V	On
MAX20095ATIE/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	12V	On

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
(SW) = Side-wettable package.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/17	Initial release	—
1	7/17	Updated min and max numbers for Boost Mode Fixed-Output Voltage (V_{SUP2}), deleted Boost Mode Fixed-Output Voltage Accuracy row in *Electrical Characteristics*; updated Reset address in *CHIP_ID (0x00)* register table; removed future product status from MAX20095ATIA/VY+ in *Ordering Information*	4, 20, 30
2	5/18	Changed package outline number (from 21-100041 to 21-100130) and land pattern number (from 90-0025 to 90-0027), as well as thermal resistances in the *Package Information* table; removed future product status from MAX20095ATIB/VY+, MAX20095ATIC/VY+, MAX20095ATID/VY+, and MAX20095ATIE/VY+ in the *Ordering Information* table	3, 30
3	7/19	Updated *Simplified Block Diagram*, *Pin Description*, *Detailed Description*, *I2C User Command and Register Map*, and *Ordering Information*	2, 11, 16, 17, 20, 24, 26, 27, 30
4	1/20	Updated *Simplified Block Diagram*, *Electrical Characteristics*, *Detailed Description*, *Register Map*, *Applications Information*, and *Ordering Information*	2, 5, 16, 17, 22, 27, 30

