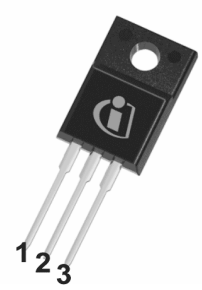
MOSFET

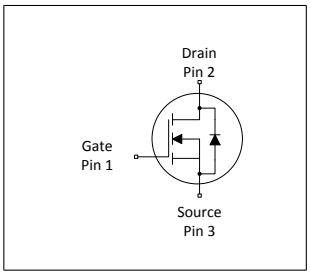
OptiMOS™ 5 Power-Transistor, 60 V

PG-TO 220 FP



Features

- Ideal for high frequency switching and sync. rec.
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	4	mΩ
I_D	72	A
Q_{oss}	44	nC
Q_G(0V..10V)	38	nC

Type / Ordering Code	Package	Marking	Related Links
IPA040N06NM5S	PG-TO 220 FullPAK	040N065S	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	72 51	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C
Pulsed drain current[1]	$I_{D,pulse}$	-	-	288	A	T_C=25 °C
Avalanche energy, single pulse[2]	E_{AS}	-	-	77	mJ	I_D=72 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	36	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.2	°C/W	-

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	V_{DS}=V_{GS}, I_D=50 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	3.6 4.7	4.0 -	mΩ	V_{GS}=10 V, I_D=72 A V_{GS}=6 V, I_D=18 A
Gate resistance[3]	R_G	-	1.3	-	Ω	-
Transconductance	g_{fs}	-	110	-	S	|V_{DS}|≥2|I_D|$R_{DS(on)max}$, I_D=72 A

[1] See Diagram 3 for more detailed information
[2] See Diagram 13 for more detailed information
[3] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	2700	3500	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance	C_{oss}	-	670	-	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	28	-	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=72 A, $R_{G,ext}$=3 Ω
Rise time	t_r	-	16	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=72 A, $R_{G,ext}$=3 Ω
Turn-off delay time	$t_{d(off)}$	-	33	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=72 A, $R_{G,ext}$=3 Ω
Fall time	t_f	-	8	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=72 A, $R_{G,ext}$=3 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	13	-	nC	V_{DD}=30 V, I_D=72 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	8	-	nC	V_{DD}=30 V, I_D=72 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	7	-	nC	V_{DD}=30 V, I_D=72 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	13	-	nC	V_{DD}=30 V, I_D=72 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	38	50	nC	V_{DD}=30 V, I_D=72 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.9	-	V	V_{DD}=30 V, I_D=72 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	33	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	44	-	nC	V_{DD}=30 V, V_{GS}=0 V

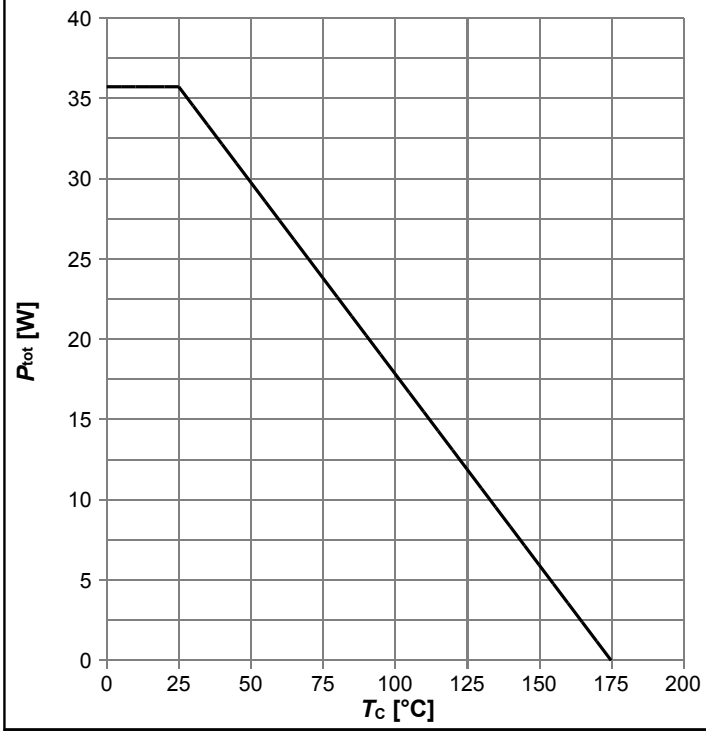
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	30	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	288	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.88	1.2	V	V_{GS}=0 V, I_F=30 A, T_j=25 °C
Reverse recovery time[1]	t_{rr}	-	33	-	ns	V_R=30 V, I_F=30 A, di_F/dt=100 A/µs
Reverse recovery charge[1]	Q_{rr}	-	28	-	nC	V_R=30 V, I_F=30 A, di_F/dt=100 A/µs

[1] Defined by design. Not subject to production test.
[2] See ″Gate charge waveforms″ for parameter definition

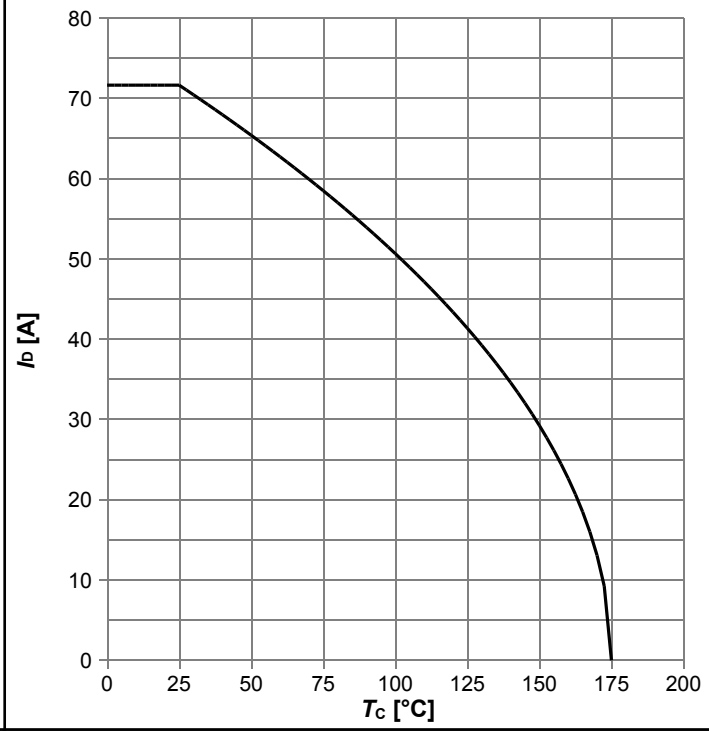
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



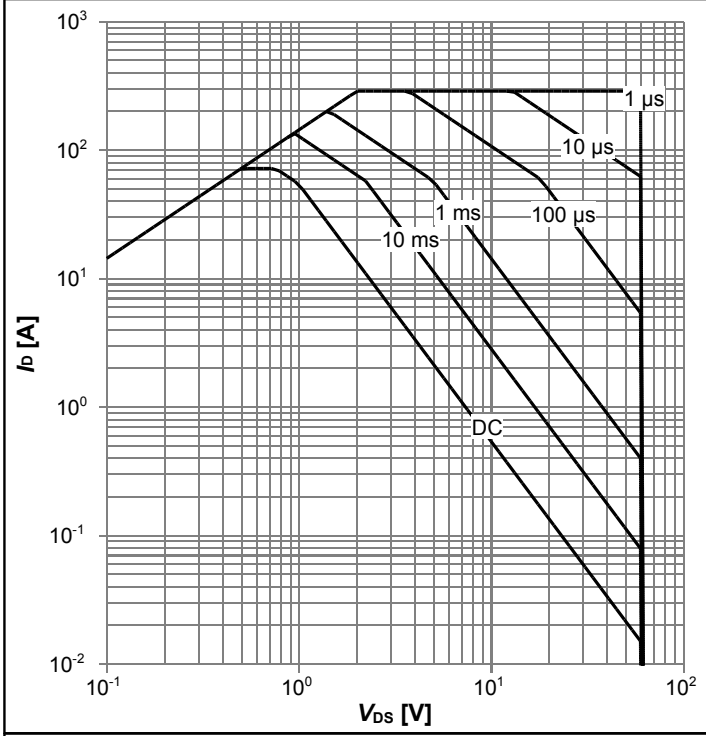
$P_{tot}=f(T_C)$

Diagram 2: Drain current



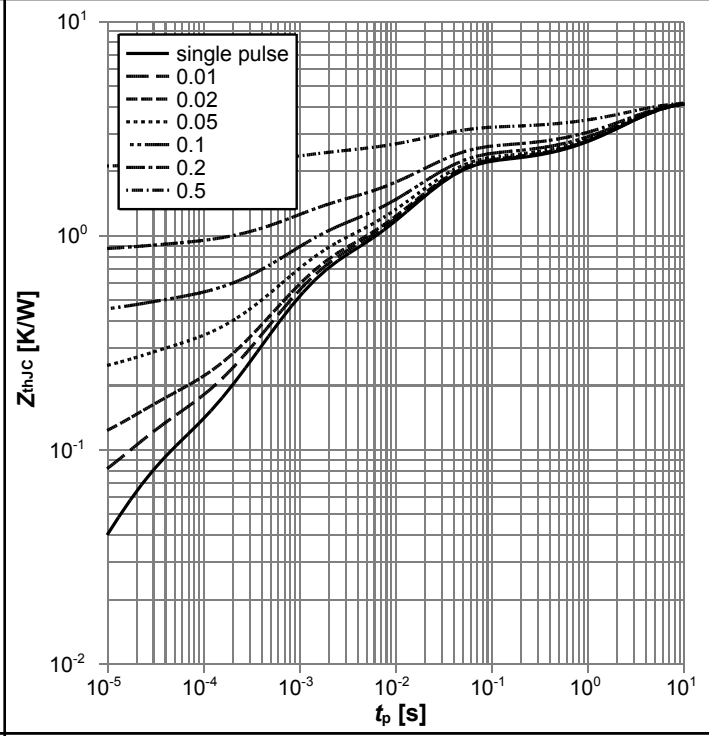
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



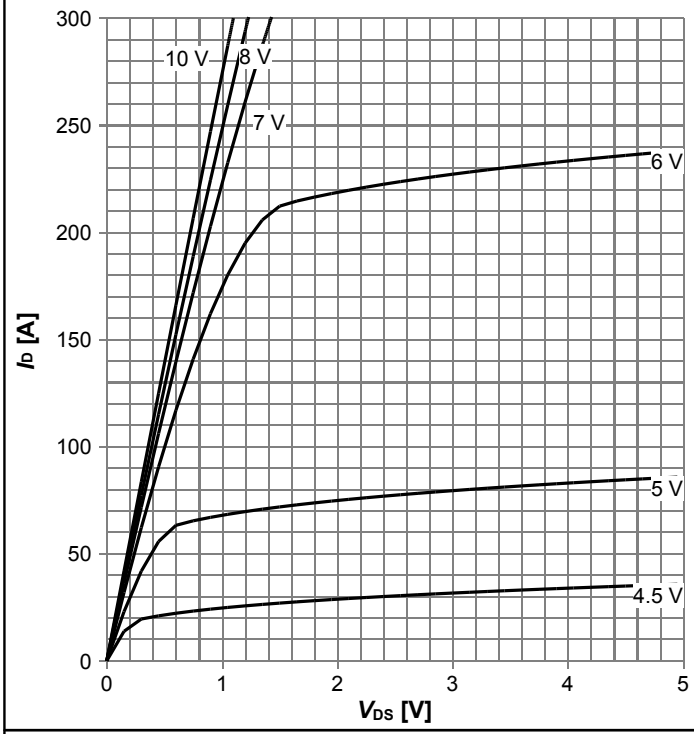
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



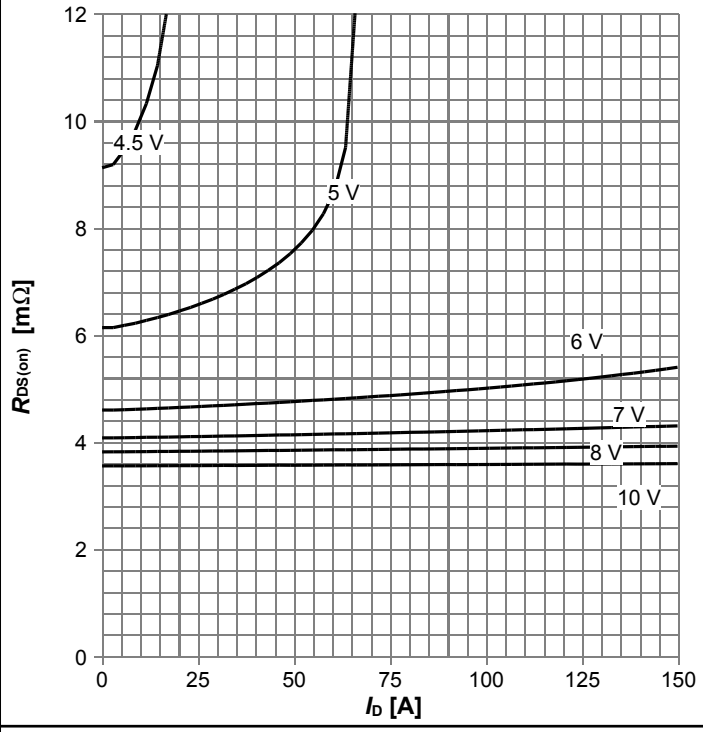
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



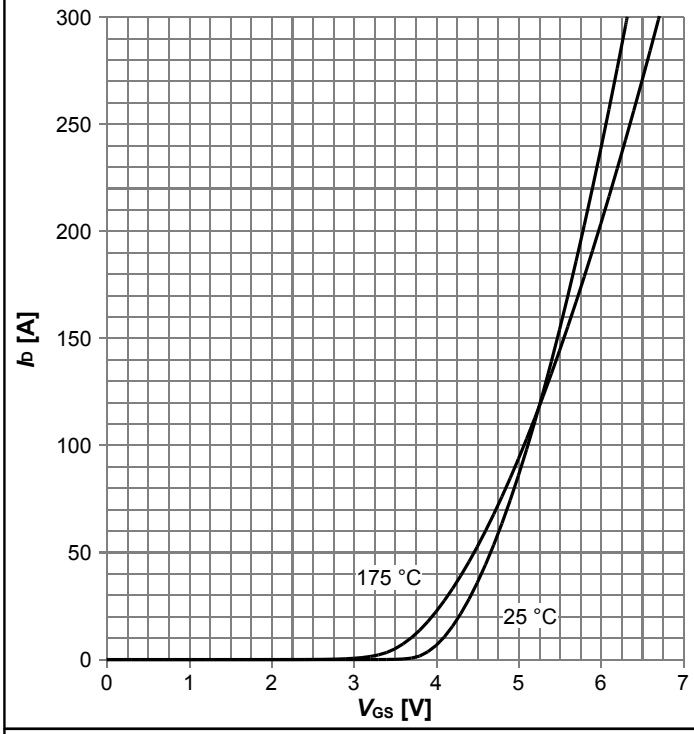
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



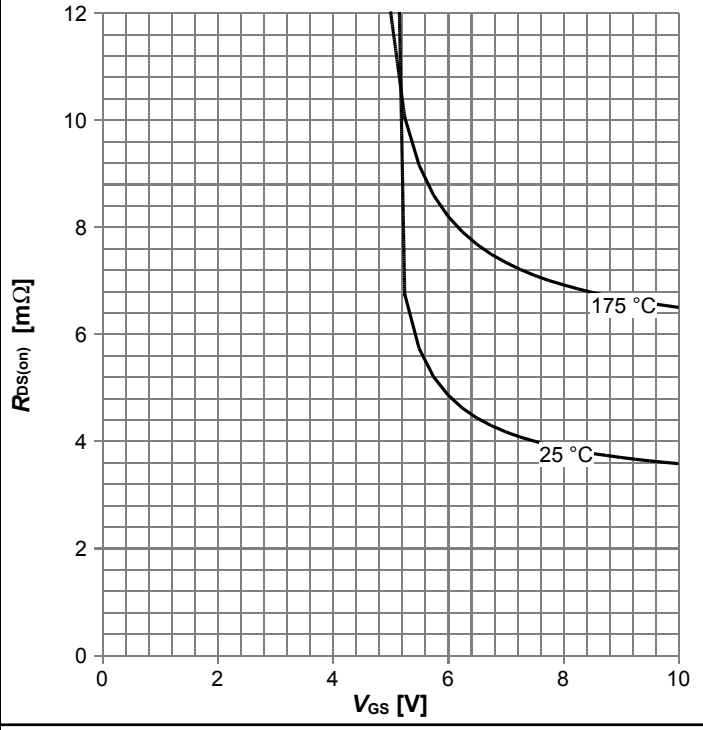
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



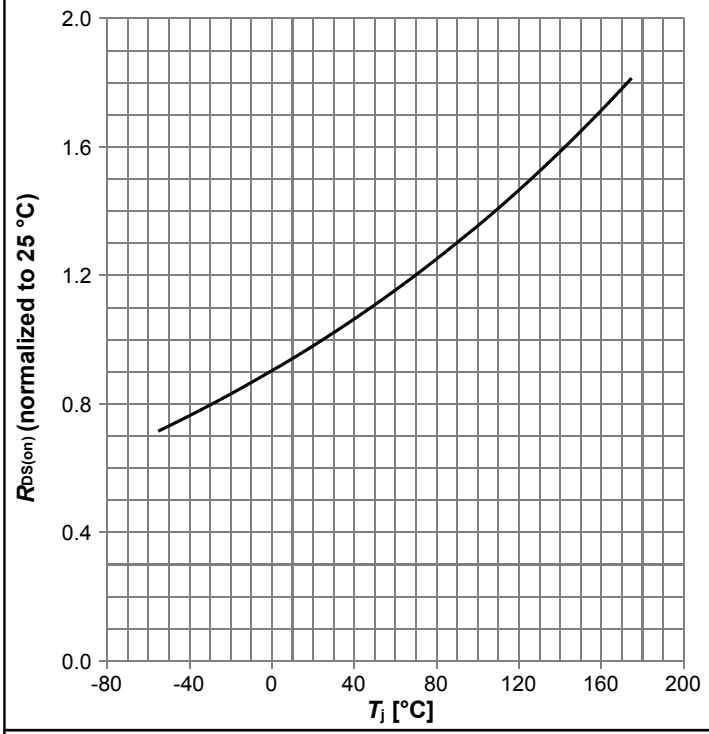
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



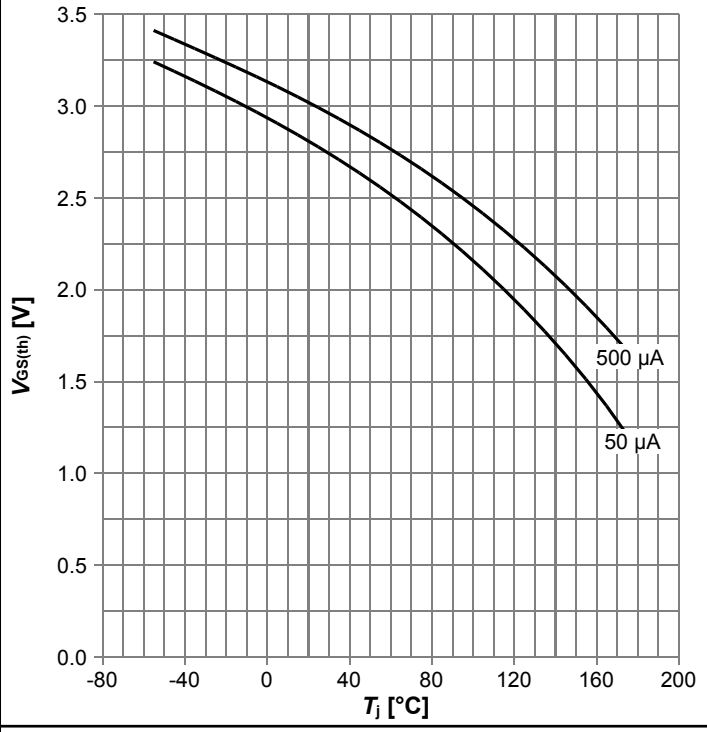
$R_{DS(on)}=f(V_{GS})$, $I_D=72$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



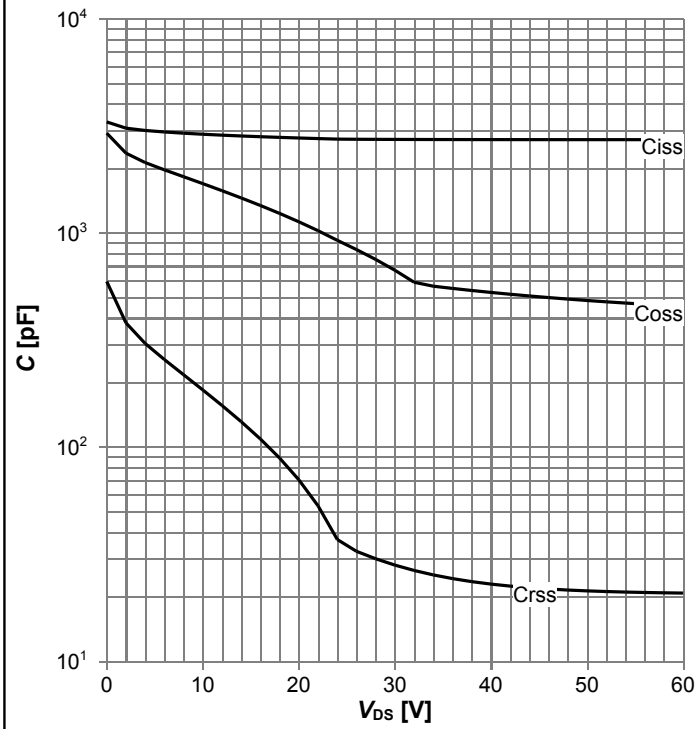
$R_{DS(on)}$=f(T_j), I_D=72 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



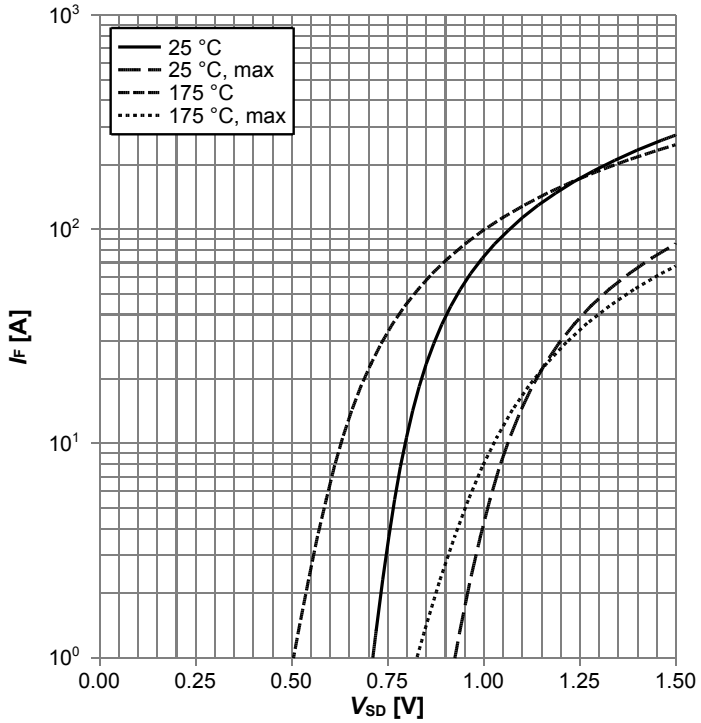
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



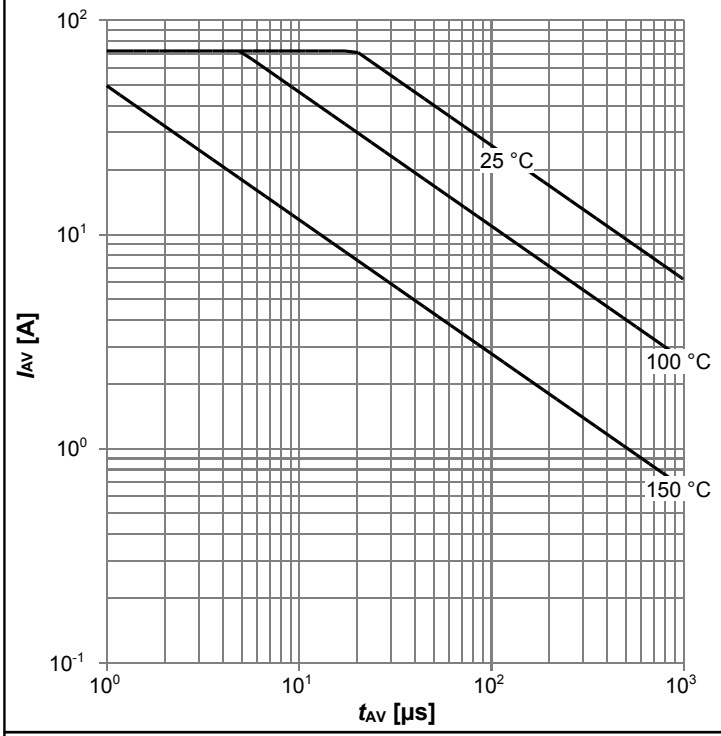
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



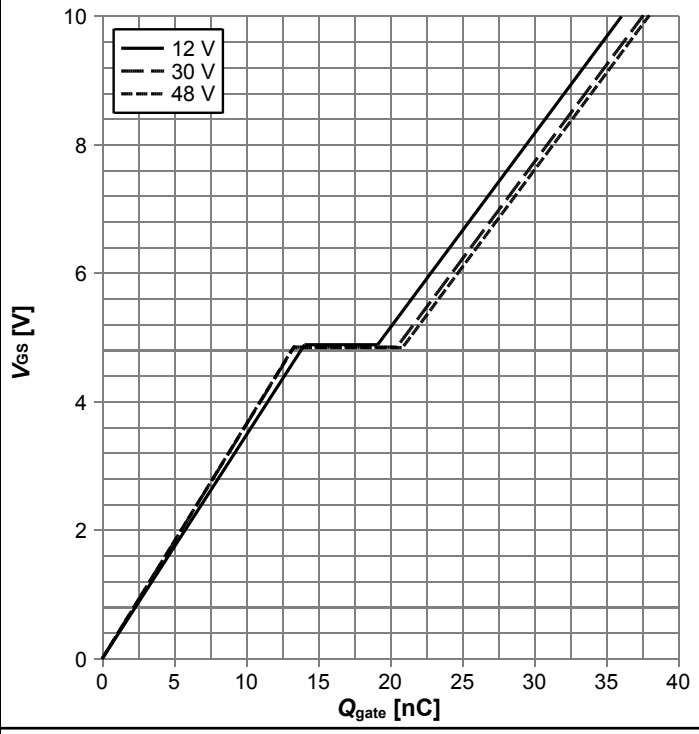
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



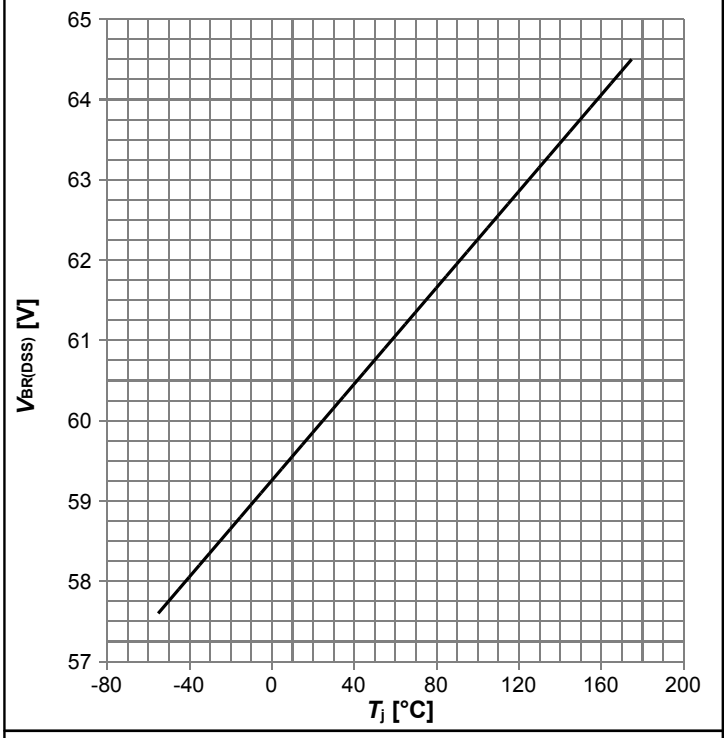
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



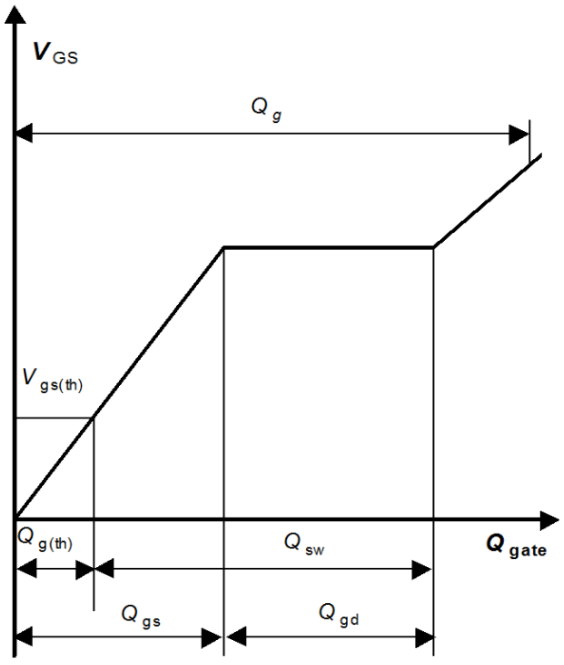
$V_{GS}=f(Q_{gate})$, $I_D=72$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

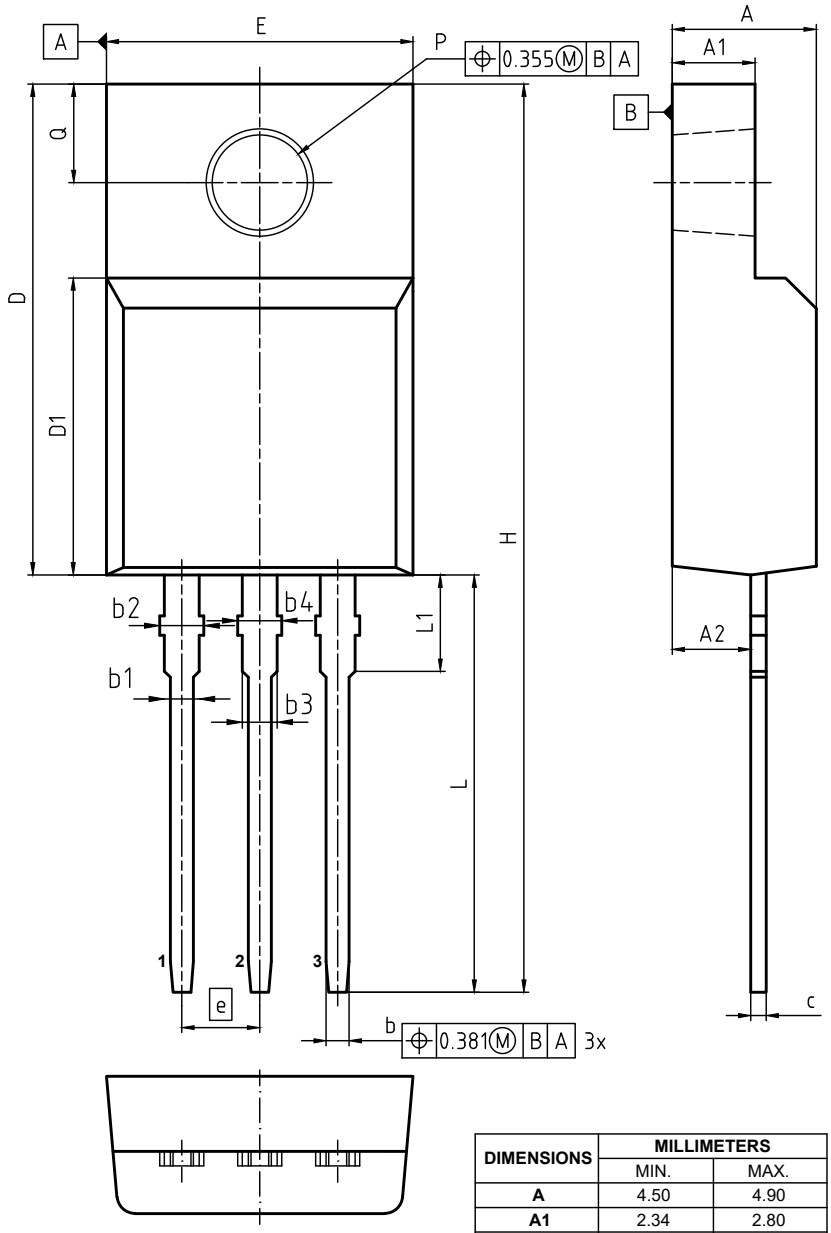


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines



NOTES:
STANDARD QUALITY GRADE
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.80
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	1.20	1.50
b3	0.65	1.38
b4	1.20	1.50
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.38
Q	3.15	3.50

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REVISION
03

ISSUE DATE
23.07.2018

SCALE 5:1
0 1 2 3 4 5mm

EUROPEAN PROJECTION

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

Revision History

IPA040N06NM5S

Revision: 2019-09-02, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2019-07-16	Release of final version
2.1	2019-09-02	Update package outline

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