ESD144-B1-W0201

Protection device

TVS (Transient Voltage Suppressor)
Bi-directional, 18 V, 0.2 pF, 0201, RoHS and Halogen Free compliant

Features

- ESD / transient protection according to:
  - IEC61000-4-2 (ESD): ±18 kV (air / contact discharge)
  - IEC61000-4-4 (EFT): ±2.5 kV / ±50 A (5/50 ns)
  - IEC61000-4-5 (Surge): ±3.5 A (8/20 µs)
- Bi-directional working voltage up to: V_{RWM} = ±18 V
- Line capacitance: C_L = 0.2 pF (typical) at f = 1 MHz
- Clamping voltage: V_{CL} = 12.5 V (typical) at I_{TLP} = 16 A with R_{DYN} = 0.58 Ω (typical)
- Very low reverse current: I_R < 1 nA (typical)
- Small form factor SMD size 0201 and low profile (0.58 x 0.28 x 0.15 mm³)
- Bi-directional and symmetric I/V characteristics for optimized design / assembly

RoHS

Potential applications

- ESD protection of RF signal lines in Near Field Communication (NFC) applications, RF antenna
- For further information please refer to application notes *[4]*, *[5]*

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

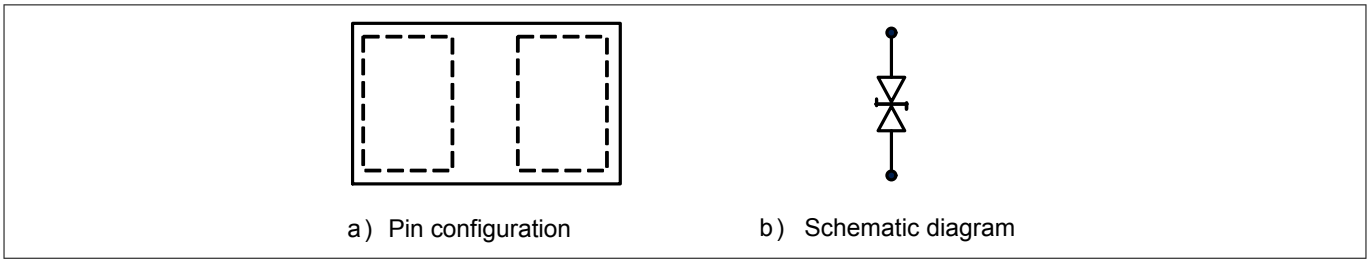

Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
ESD144-B1-W0201	WLL-2-3	1 line, bi-directional	AA [1)]

1 The device does not have any marking on the device top. The marking code is on pad side.

Table of contents

1 Maximum ratings

Note: *T_A = 25 °C, unless otherwise specified*

Table 2 Maximum ratings

Parameter	Symbol	Values	Unit
Reverse working voltage[1)]	V_{RWM}	±18	V
ESD discharge [2)]	V_{ESD} (contact)	±18	kV
	V_{ESD} (air)	±18	
Peak pulse power [3)]	P_{PK}	21	W
Peak pulse current [3)]	I_{PP}	±3.5	A
Operating temperature range	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

Attention: ***Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.***

1 Device snaps back to a low holding voltage. Please refer to AN525 for latch-up prevention *[5]*
2 V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF discharge network)
3 Stress pulse: 8/20 µs current waveform according to IEC61000-4-5

2 Electrical characteristics

Note: *T_A = 25 °C, unless otherwise specified*
Device is electrically symmetrical

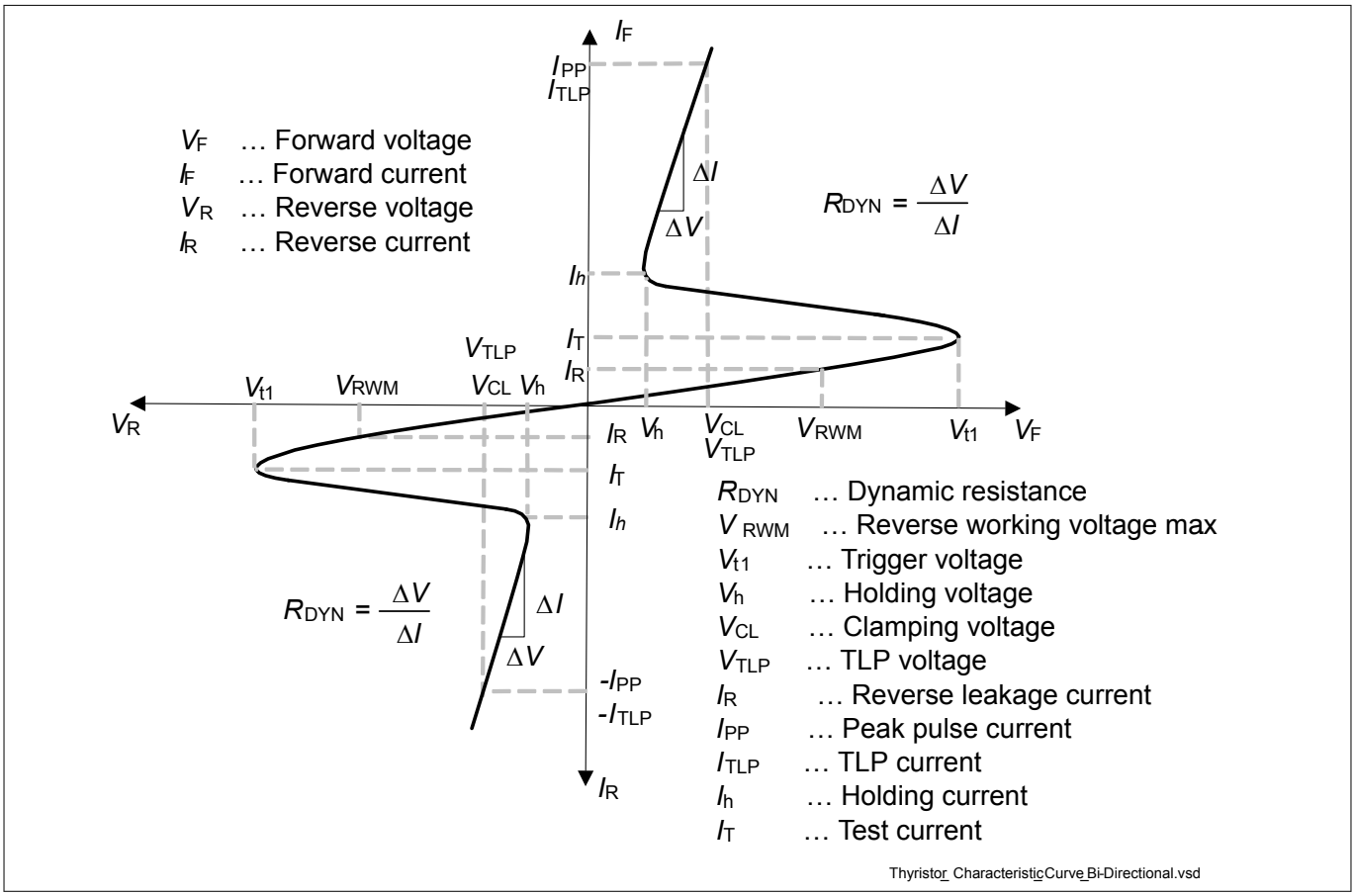

Figure 2 Definitions of electrical characteristics

Electrical characteristics

Table 3 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Breakdown voltage	V_{br}	18.5	22	28.5	V	I_R = 1 mA
Holding voltage	V_h	–	1.9	–	V	$I_R = I_h$
Holding reverse current	I_h	–	25	–	mA	$V_R = V_h$
Reverse current	I_R	–	–	50	nA	V_R = 18 V

Table 4 AC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.2	0.35	pF	V_R = 0 V, f = 1 MHz
		–	0.19	–		V_R = 0 V, f = 2.5 GHz

Table 5 ESD and Surge characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Clamping voltage [1)]	V_{CL}	–	8	–	V	I_{TLP} = 8 A, t_p = 100 ns
		–	12.5	–		I_{TLP} = 16 A, t_p = 100 ns
Clamping voltage [2)]		–	3	–		I_{PP} = 1 A, t_p = 8/20 µs
		–	5	–		I_{PP} = 3 A, t_p = 8/20 µs
Dynamic resistance [1)]	R_{DYN}	–	0.58	–	Ω	t_p = 100 ns

1 Please refer to Application Note AN210 *[1]*. TLP parameters: Z_0 = 50 Ω , t_p = 100ns, t_r = 0.6 ns.
2 Stress pulse: 8/20µs current waveform according to IEC61000-4-5

3 Typical characteristic diagrams

Note: *T_A = 25 °C, unless otherwise specified*

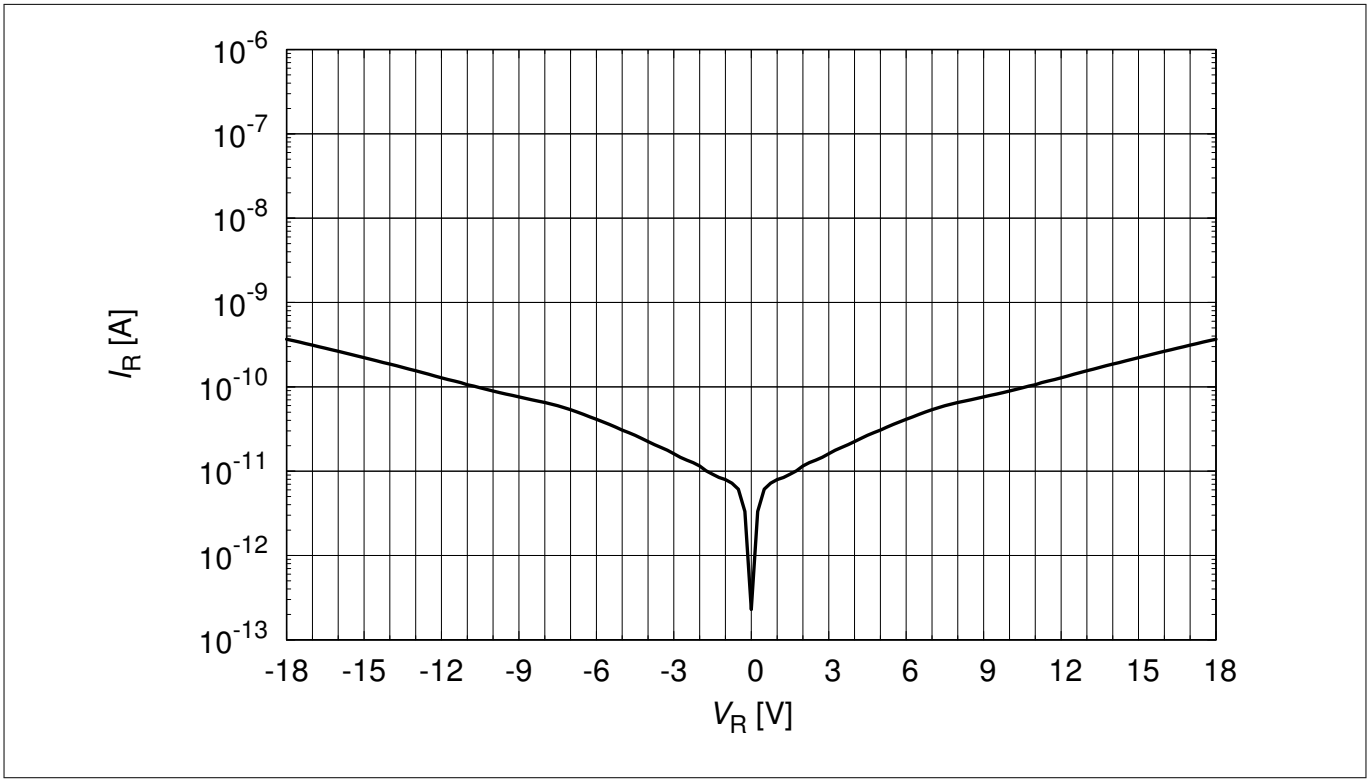

Figure 3 Reverse leakage current: $I_R = f(V_R)$

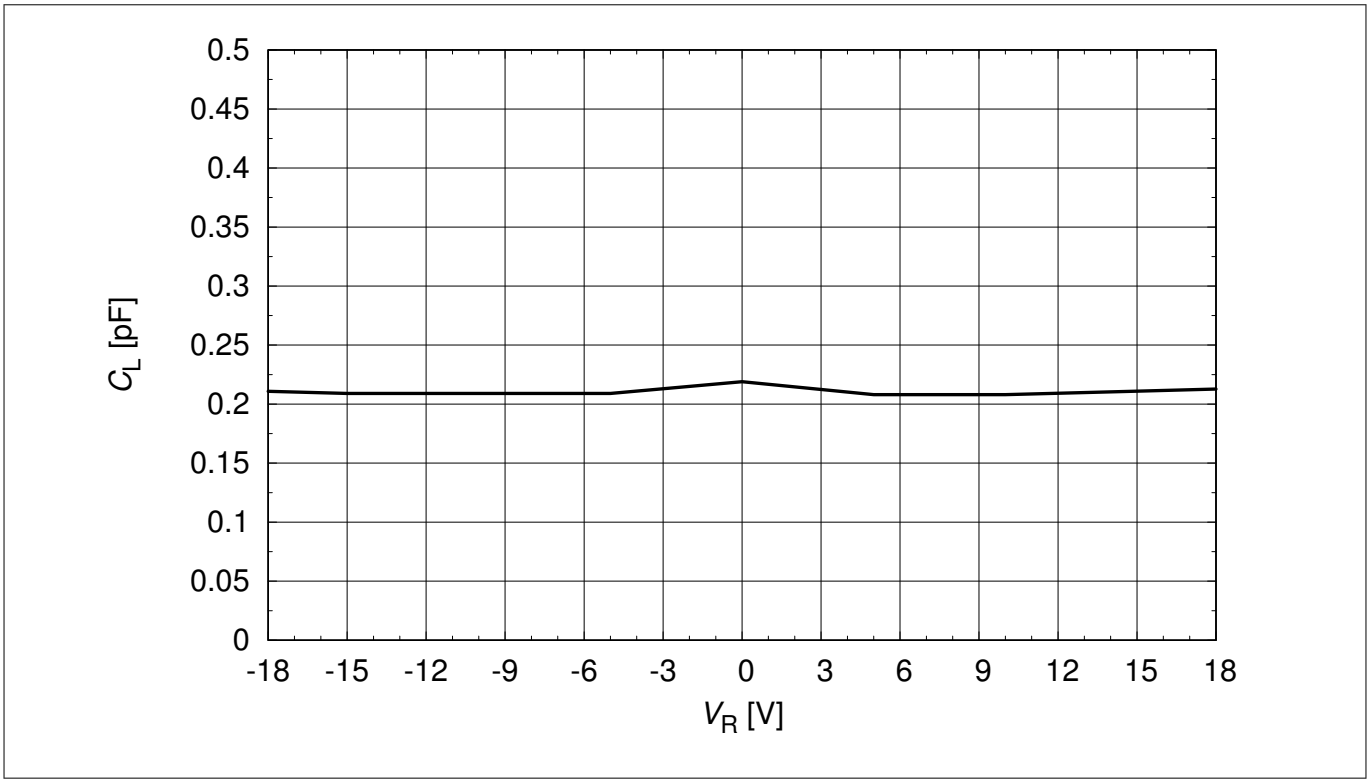

Figure 4 Line capacitance: $C_L = f(V_R)$, f = 1 MHz

Typical characteristic diagrams

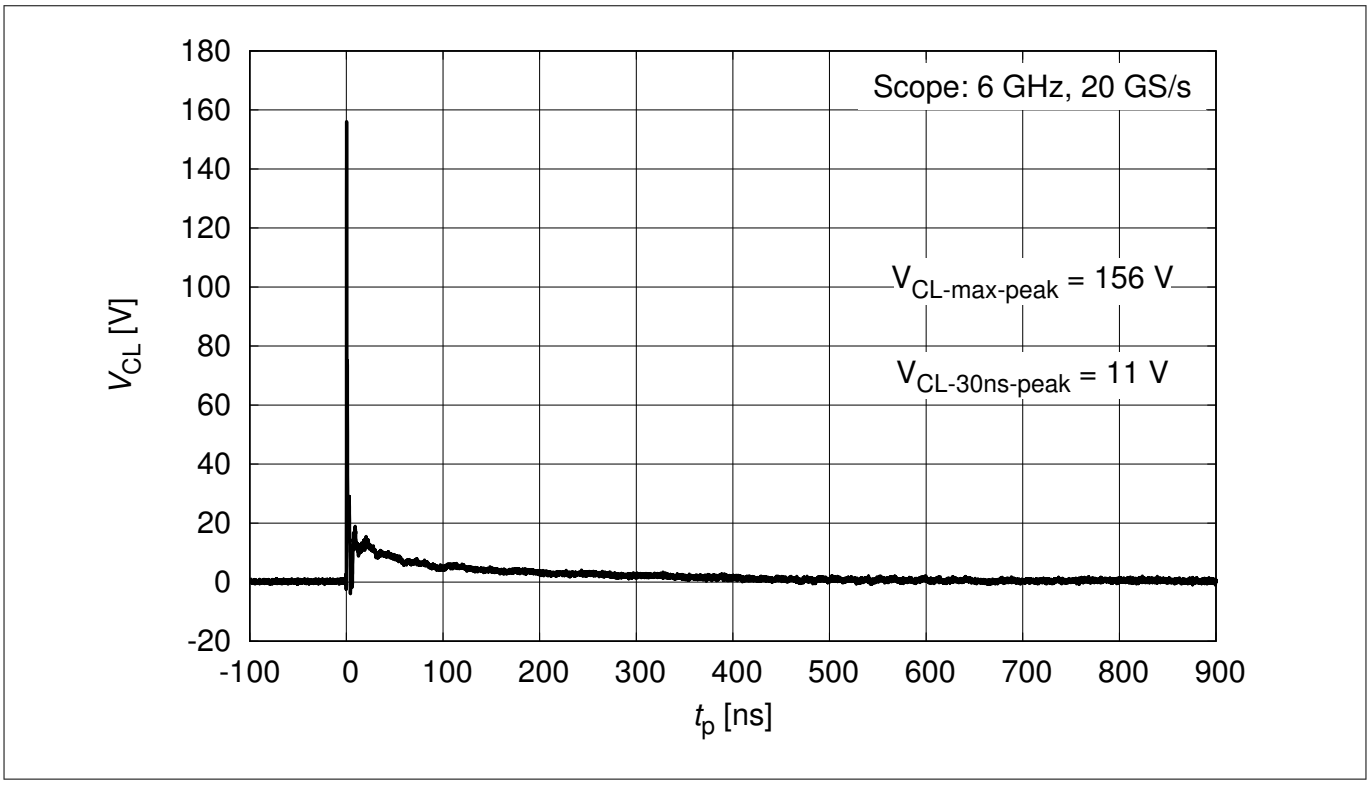

Figure 5 Clamping voltage (ESD): V_{CL} = f(t), 8 kV positive pulse according to IEC61000-4-2

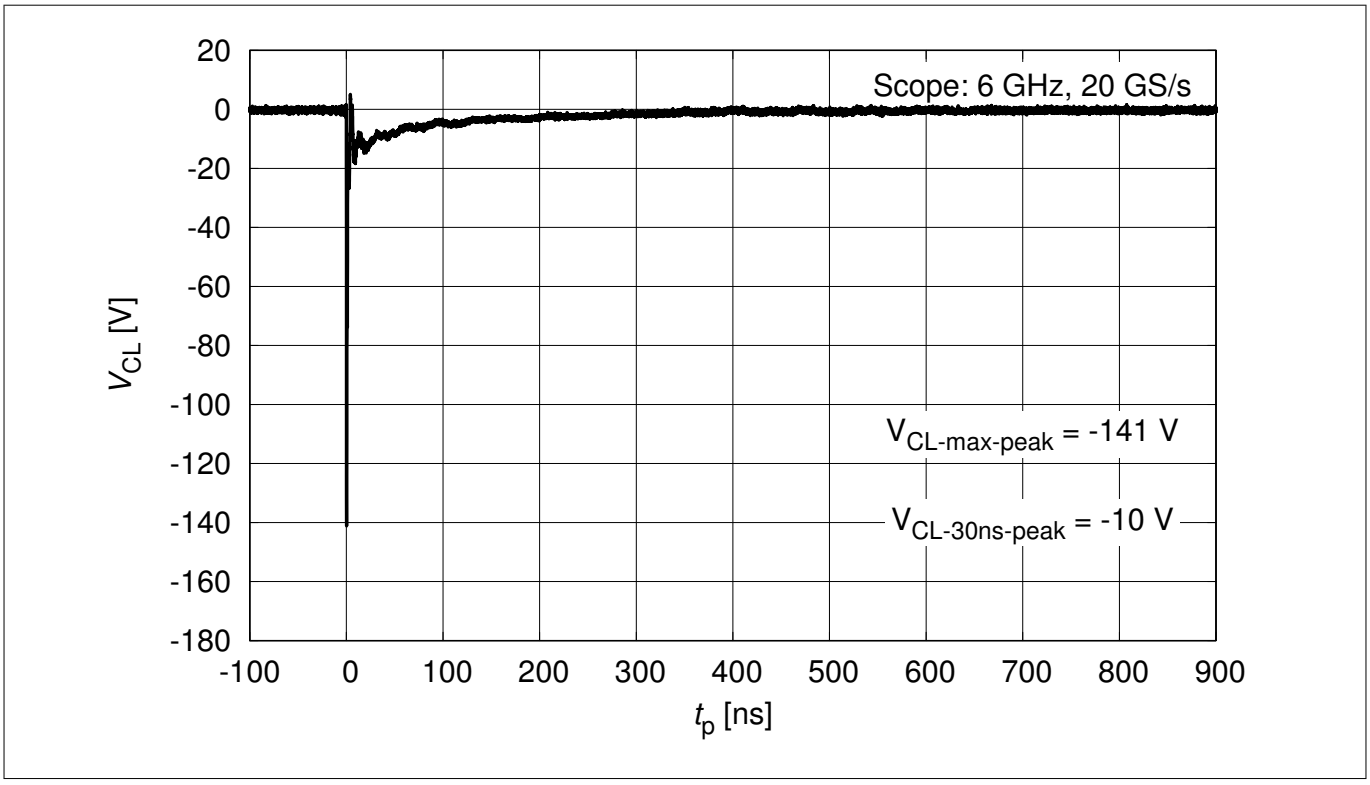

Figure 6 Clamping voltage (ESD): V_{CL} = f(t), 8 kV negative pulse according to IEC61000-4-2

Typical characteristic diagrams

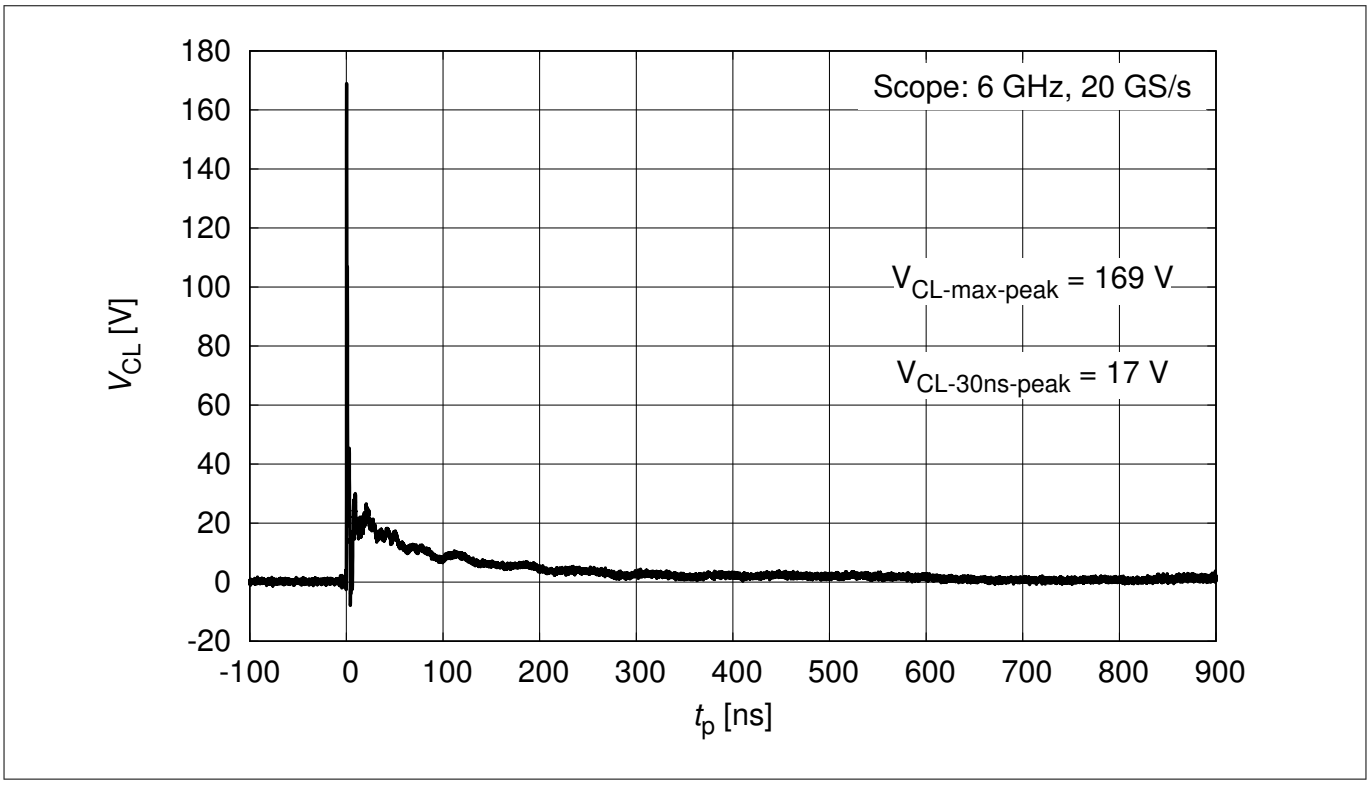

Figure 7 Clamping voltage (ESD): V_{CL} = f(t), 15 kV positive pulse according to IEC61000-4-2

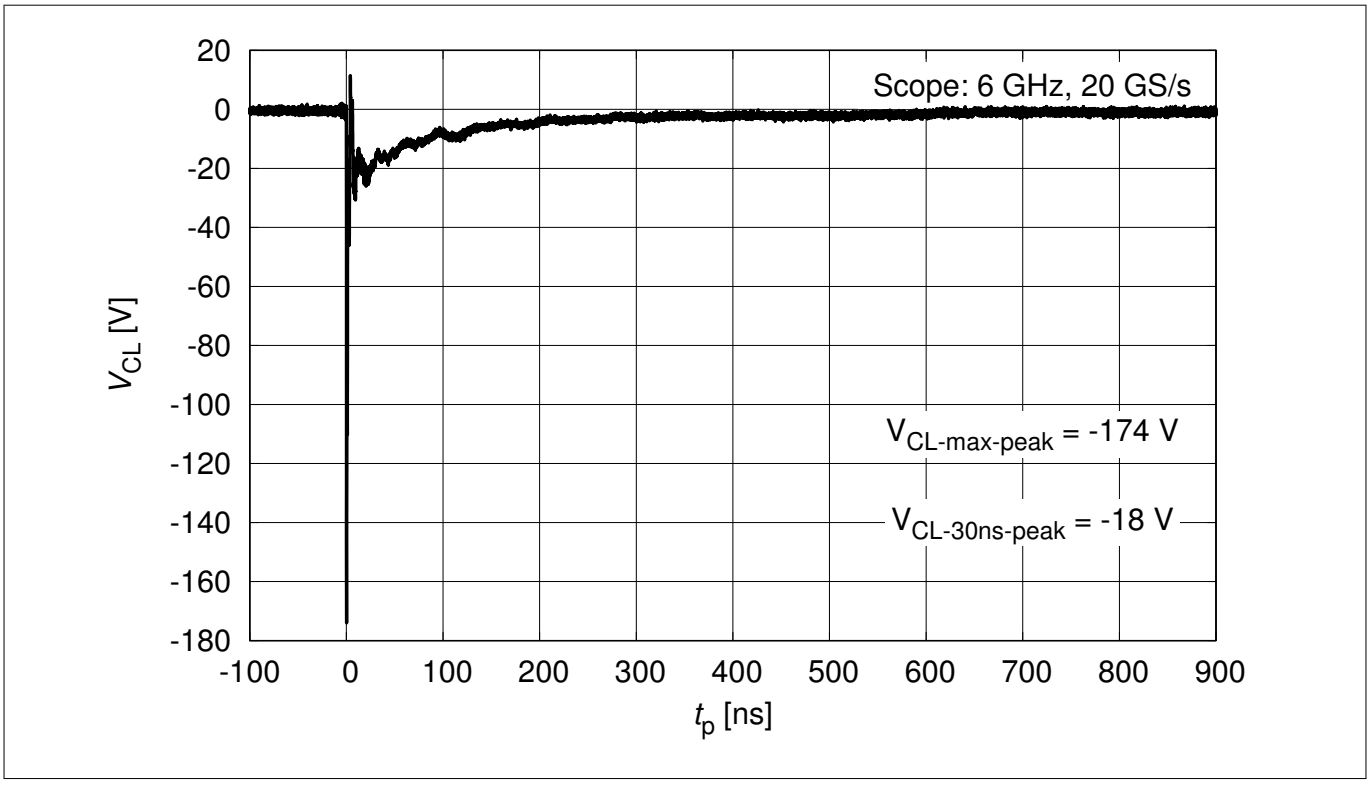

Figure 8 Clamping voltage (ESD): V_{CL} = f(t), 15 kV negative pulse according to IEC61000-4-2

Typical characteristic diagrams

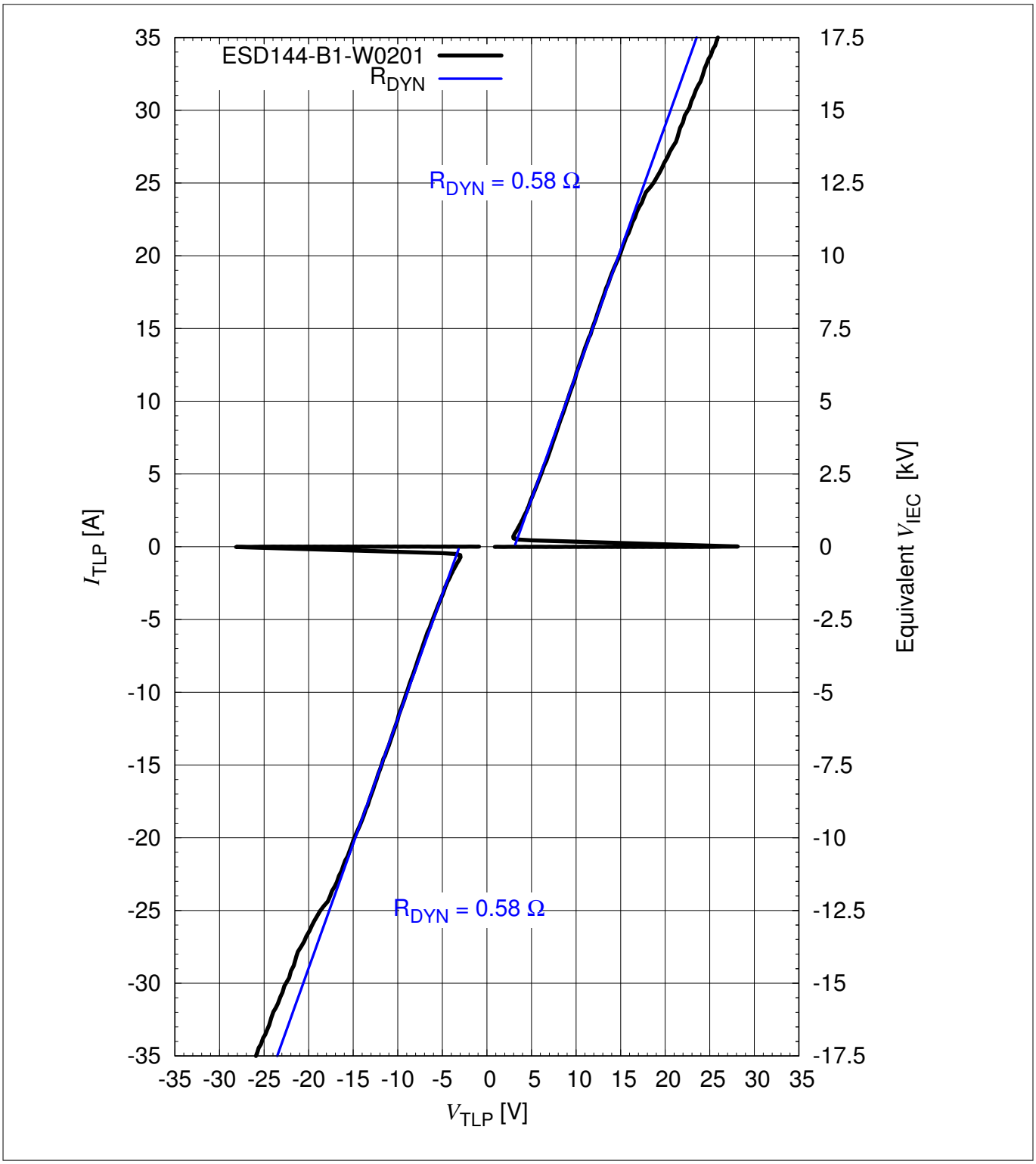

Figure 9 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ *[1]*

Typical characteristic diagrams

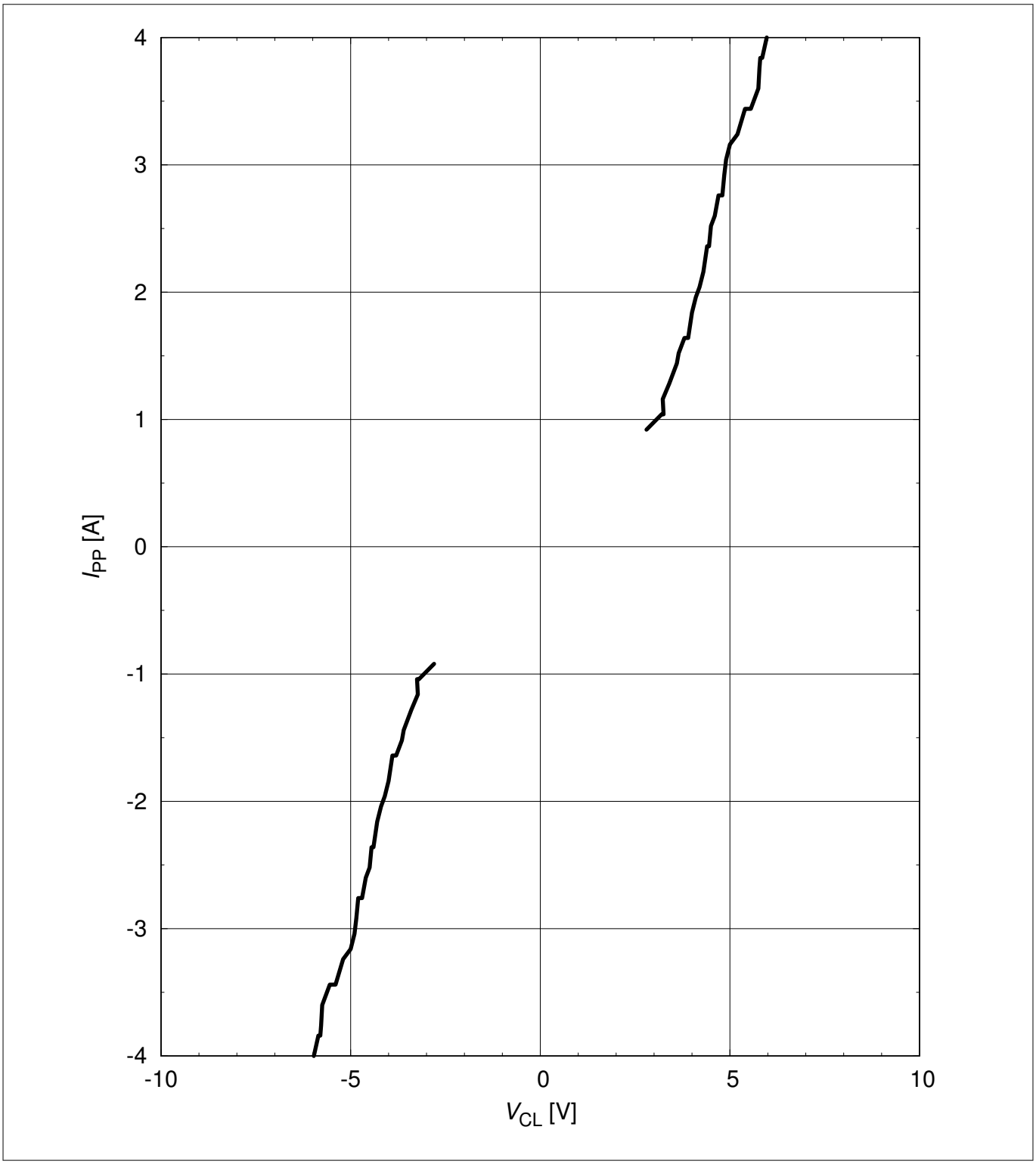

Figure 10 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ according to IEC61000-4-5 *[1]*

Typical characteristic diagrams

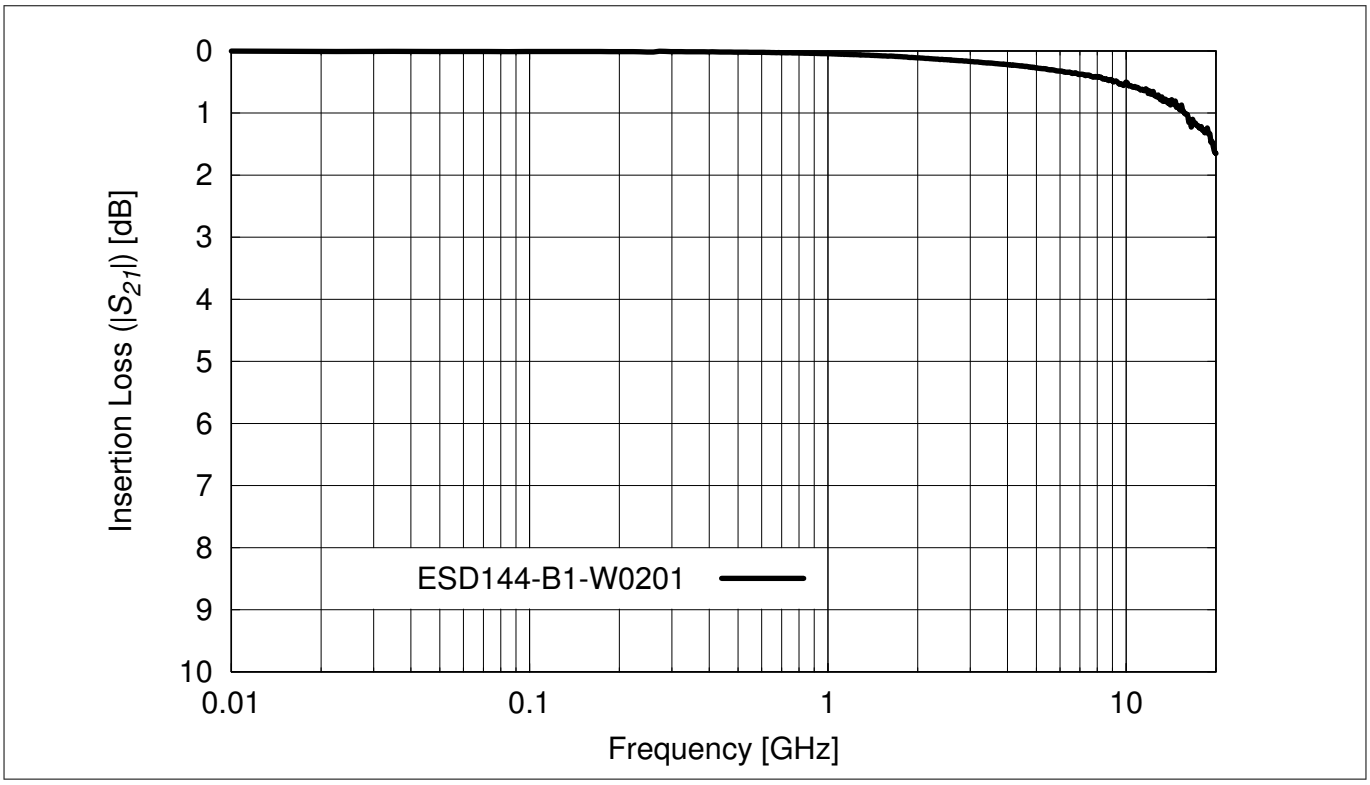

Figure 11 Insertion loss vs. frequency in a 50 Ω system

4 Package information

4.1 WLL-2-3 package

Note: *Dimensions in mm*

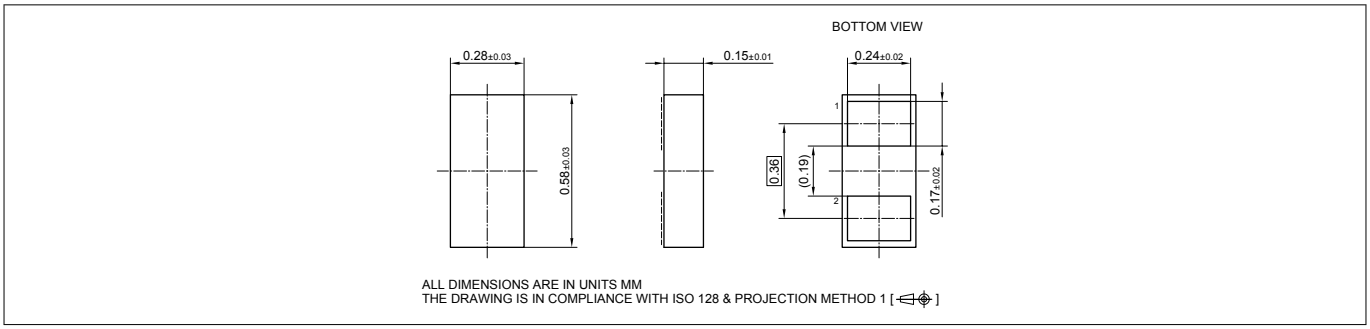

Figure 12 WLL-2-3 package outline

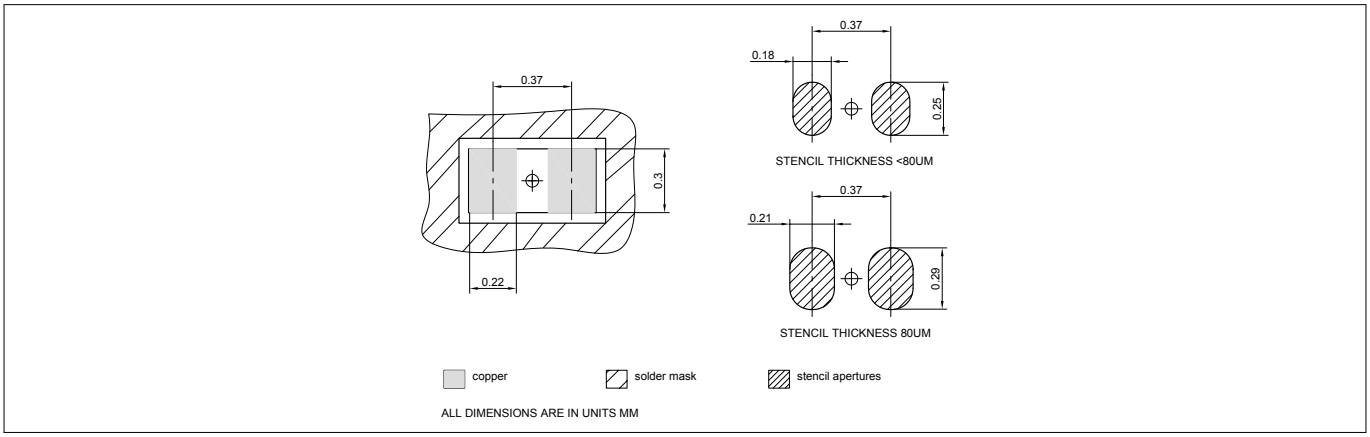

Figure 13 WLL-2-3 footprint - Recommendations for Printed Circuit Board Assembly see *[2]*

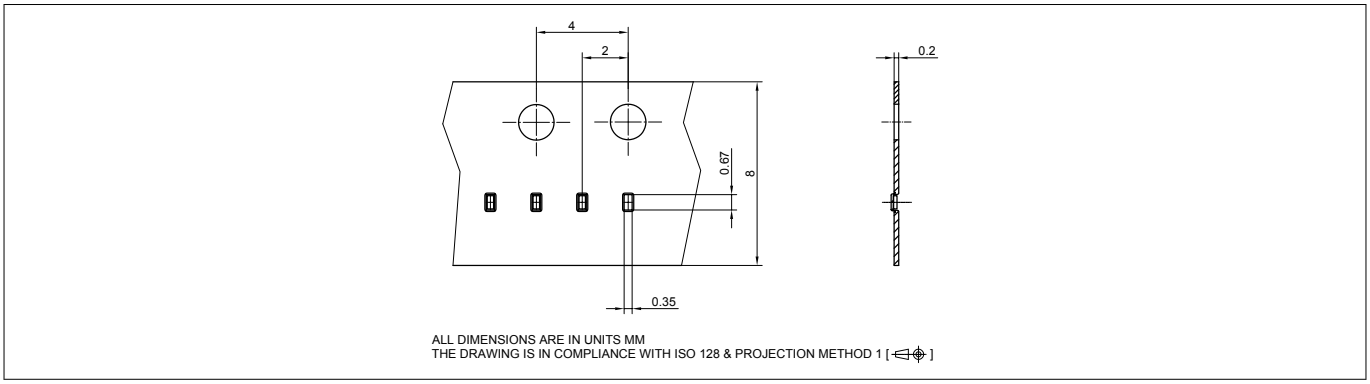

Figure 14 WLL-2-3 packing

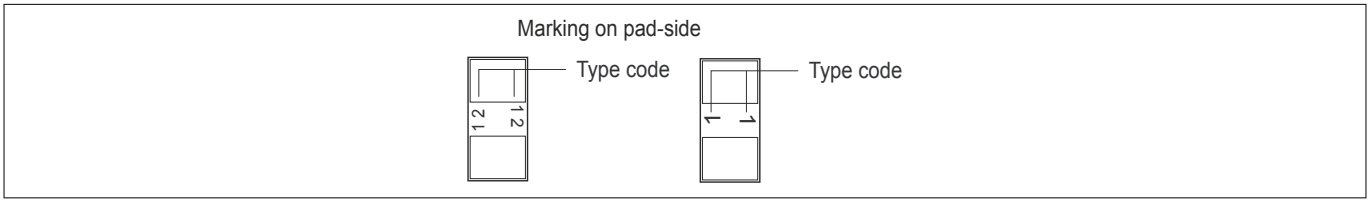

Figure 15 WLL-2-3 marking example (see *Table 1*)

5 References

[1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

[2] Infineon AG - **Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages**
http://www.infineon.com/Packageinformation_WLL

[3] Infineon AG - **Application Note AN392**: TVS Diodes in ChipScalePackage reduce size and save cost

[4] Infineon AG - **Application Note AN244**: ESD Protection in Chip Size Package (CSP) tailored for the NFC Frontend

[5] Infineon AG - **Application Note AN525**: Latch-up prediction for SCR TVS device

Revision history

Revision history: Rev.0.9, 2016-04-21	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2017-08-14	
All	Final datasheet

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Edition 2017-08-14

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-mao1482157662556

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