Gate Driver Providing Galvanic Isolation Series

1ch Gate Driver Providing Galvanic Isolation 2500 Vrms Isolation Voltage

BM6109FV-C

General Description

BM6109FV-C is a gate driver with an isolation voltage of 2500 Vrms. It has an I/O delay time of 700 ns, minimum input pulse width of 600 ns, and incorporates the fault signal output function, under voltage lockout (UVLO) function, Short circuit protection (SCP) function, overcurrent protection (OCP) function, overheat protection function, active miller clamping function and temperature monitoring function.

Key Specifications

■ Isolation Voltage:	2500 Vrms
■ Maximum Gate Drive Voltage:	18 V
■ I/O Delay Time:	700 ns(Max)
■ Minimum Input Pulse Width:	600 ns

Package

Package	W(Typ) x D(Typ) x H(Max)
SSOP-B28W	9.2 mm x 10.4 mm x 2.4 mm

Features

- AEC-Q100 Qualified(Note 1)
- Fault Signal Output Function
- Under Voltage Lockout Protection Function
- Short Circuit Protection Function
- Overcurrent Protection Function
- Overheat Protection Function
- Soft Turn Off Function
  (Adjustable Turn OFF Time)
- Active Miller Clamping
- Temperature Monitor

(Note 1) Grade1

Applications

- Automotive Inverter
- Automotive DC-DC Converter
- Industrial Inverter System
- UPS System

Typical Application Circuit

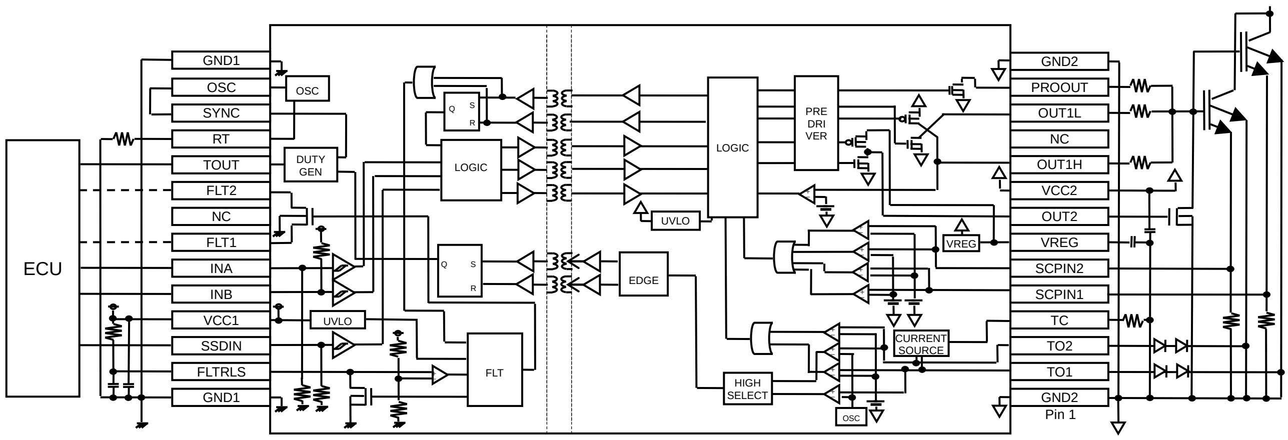


Figure 1. Basic Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configurations

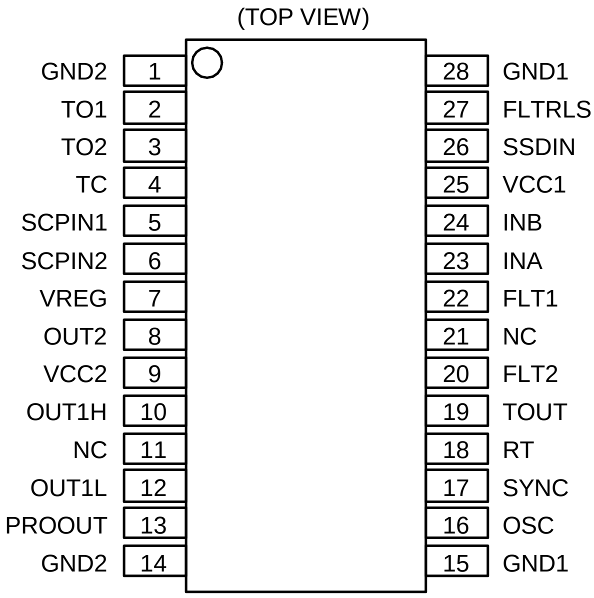


Figure2. Pin Configurations

Pin Description

Pin No.	Pin Name	Function
1	GND2	Secondary side ground pin
2	TO1	Constant current output / Sensor voltage input pin 1
3	TO2	Constant current output / Sensor voltage input pin 2
4	TC	Constant current setting resistor connection pin
5	SCPIN1	Short circuit and overcurrent detection pin 1
6	SCPIN2	Short circuit and overcurrent detection pin 2
7	VREG	Secondary side internal power supply pin
8	OUT2	Miller Clamp Control pin
9	VCC2	Secondary side power supply
10	OUT1H	Source side output / Gate voltage input pin
11	NC	No connection
12	OUT1L	Sink side output pin
13	PROOUT	Soft shutdown output pin
14	GND2	Secondary side ground pin
15	GND1	Primary side ground pin
16	OSC	Output pin for oscillation frequency
17	SYNC	External clock input pin
18	RT	Oscillation frequency setup resistor connection pin
19	TOUT	Temperature information output pin
20	FLT2	Fault signal output pin
21	NC	No connection
22	FLT1	Fault signal output pin
23	INA	Control input pin
24	INB	Control input pin
25	VCC1	Primary side power supply pin
26	SSDIN	Soft shutdown control input pin
27	FLTRLS	Fault output holding time setup pin
28	GND1	Primary side ground pin

Description of Recommended Range Of External Constants

Pin Name	Symbol	Recommended Value Min	Typ	Max	Unit
TC (As Temperature monitor)	R_{TC}	0.5	-	25	kΩ
TC (No Temperature monitor)	R_{TC}	0.1	1	10	MΩ
RT	R_{RT}	40.2	100	402	kΩ
FLTRLS	C_{FLTRLS}	-	0.01	1.50	µF
FLTRLS	R_{FLTRLS}	50	200	1000	kΩ
VCC1	C_{VCC1}	0.2	-	-	µF
VCC2	C_{VCC2}	0.4	-	-	µF
VREG	C_{VREG}	0.1	1	10	µF

C_{VCC1} : Power supply for driving the internal transformer
C_{VCC2} : Power supply for driving MOS FET/IGBT gate

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Primary Side Supply Voltage	V_{CC1}	-0.3 to +7.0 (Note 2)	V
Secondary Side Supply Voltage	V_{CC2}	-0.3 to +20.0 (Note 3)	V
Input Voltage for INA, INB, SSDIN and SYNC Pins	V_{IN}	-0.3 to V_{CC1}+0.3 or 7.0 (Note 2)	V
Input Voltage for SCPIN1 and SCPIN2 Pins	V_{SCPIN}	-0.3 to +6.0 (Note 3)	V
Input Voltage for TO1 and TO2 Pins	V_{TO}	-0.3 to V_{CC2}+0.3 (Note 3)	V
Input Voltage for FLT Pin	V_{FLT}	-0.3 to +7.0 (Note 2)	V
Output Current for FLT Pin	I_{FLT}	10	mA
Output Current for TOUT Pin	I_{TOUT}	10	mA
Output Current for OSC Pin	I_{OSC}	10	mA
Output Current for OUT1H Pin (Peak10 µs)	$I_{OUT1HPEAK}$	5 (Note 4)	A
Output Current for OUT1L Pin (Peak10 µs)	$I_{OUT1LPEAK}$	5 (Note 4)	A
Output Current for PROOUT Pin (Peak10 µs)	$I_{PROOUTPEAK}$	5 (Note 4)	A
Output Current for OUT2 Pin (Peak10 µs)	$I_{SOUTPEAK}$	5 (Note 4)	A
Output Current for VREG Pin	I_{VREG}	10	mA
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

(Note 2) Relative to GND1
(Note 3) Relative to GND2
(Note 4) On the supposition that requirements for Tj=150°C are satisfied

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance(Note 5)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 7)	2s2p(Note 8)	
SSOP-B28W				
Junction to Ambient	θ_{JA}	112.9	64.4	°C/W
Junction to Top Characterization Parameter(Note 6)	Ψ_{JT}	34	23	°C/W

(Note 5) Based on JESD51-2A(Still-Air).
(Note 6) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 7) Using a PCB board based on JESD51-3.
(Note 8) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
VCC1 Supply Voltage (Note 9)	V_{CC1}	4.5	5.0	5.5	V
VCC2 Supply Voltage (Note 10)	V_{CC2}	14	16	18	V
TO1 and TO2 Input Voltage (Note 10)	V_{TO}	1.4	-	3.5	V
SYNC Input Frequency	f_{SYNC}	5	20	50	kHz
Operating Temperature	Topr	-40	-	+125	°C

(Note 9) Relative to GND1
(Note 10) Relative to GND2

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Unit
Insulation Resistance (V_{IO}=500 V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1 min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1 s	V_{ISO}	3000	Vrms

Electrical Characteristics

(Unless otherwise specified Ta=-40 °C to 125 °C, V_{CC1}=4.5 V to 5.5 V, V_{CC2}=14 V to 18 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Primary Side Circuit Current 1	I_{CC11}	2.1	4.8	10.1	mA	OUT=L
Primary Side Circuit Current 2	I_{CC12}	2.1	4.8	10.1	mA	OUT=H
Primary Side Circuit Current 3	I_{CC13}	2.2	4.9	10.3	mA	INA=10 kHz, Duty=50 %
Primary Side Circuit Current 4	I_{CC14}	2.3	5.0	10.4	mA	INA=20 kHz, Duty=50 %
Secondary Side Circuit Current	I_{CC2}	1.6	3.2	4.8	mA	R_{TC}=4.7 kΩ
VREG Output Voltage	V_{REG}	4.8	5.0	5.2	V	
Logic Input						
Logic High Level Input Voltage	V_{INH}	0.7 x V_{CC1}	-	V_{CC1}	V	INA, INB, SSDIN, SYNC
Logic Low Level Input Voltage	V_{INL}	0	-	0.3 x V_{CC1}	V	INA, INB, SSDIN, SYNC
Logic Pull Down Resistance	R_{IND}	250	500	1000	kΩ	INA, SSDIN, SYNC
Logic Pull Up Resistance	R_{INU}	250	500	1000	kΩ	INB
Logic Input Filter Time	t_{INFIL}	5	35	65	ns	INA, INB, SSDIN
Minimum Input Pulse Width(High pulse)	t_{INMINH}	70	130	190	ns	INA, INB
Minimum Input Pulse Width(Low pulse)	t_{INMINL}	70	130	190	ns	INA, INB
Minimum Input Pulse Width (SSDIN)	$t_{SSDINMIN}$	50	80	110	ns	SSDIN
Output						
Turn ON Time	t_{PON}	110	220	440	ns	
Turn OFF Time	t_{POFF}	110	220	440	ns	
Propagation Distortion	t_{PDIST}	-110	0	+110	ns	
OUT1H-OUT1L Deadtime H	t_{HLOFFH}	50	120	190	ns	For output L to H
OUT1H-OUT1L Deadtime L	t_{HLOFFL}	50	120	190	ns	For output H to L
OUT1H ON Resistance	R_{ON1H}	-	0.45	1.00	Ω	I_{OUT1H}=-100 mA
OUT1L ON Resistance	R_{ON1L}	-	0.45	1.00	Ω	I_{OUT1L}=100 mA
OUT1H Maximum Current	$I_{OUTHMAX1}$	4.5	-	-	A	Design guarantee, V_{CC2}=16 V
OUT1L Maximum Current	$I_{OUTLMAX1}$	4.5	-	-	A	Design guarantee, V_{CC2}=16 V
Soft Shutdown Output Delay Time	t_{SSD}	100	150	200	ns	
PROOUT ON Resistance	R_{ONPRO}	-	0.9	2.0	Ω	I_{PROOUT}=100 mA
OUT2 ON Threshold	V_{OUT2ON}	2.7	3.0	3.3	V	
OUT2 Delay Time	t_{OUT2}	-	-	100	ns	
OUT2 ON Resistance (Source side)	R_{ON2H}	-	2.0	4.5	Ω	I_{OUT2}=-100 mA
OUT2 ON Resistance (Sink side)	R_{ON2L}	-	2.6	5.5	Ω	I_{OUT2}=100 mA
OUT2 H Voltage	V_{OUT2H}	V_{REG}-0.45	V_{REG}-0.2	V_{REG}	V	I_{OUT2}=-100 mA
Common Mode Transient Immunity	CM	100	-	-	kV/μs	Design guarantee

Electrical Characteristics-continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Temperature Monitor						
TC Output Voltage	V_{TC}	0.916	0.940	0.964	V	
TOx Constant Current	I_{TO}	194	200	206	µA	TOx=TO1, TO2, R_{TC}=4.7 kΩ
TOUT Duty Accuracy 1	D_{TOUT1}	-2.35	0.00	+2.35	%	TO1=TO2=1.40 V (Duty=10.00 %), SYNC=20 kHz
TOUT Duty Accuracy 2	D_{TOUT2}	-2.85	0.00	+2.85	%	TO1=TO2=1.95 V (Duty=30.95 %), SYNC=20 kHz
TOUT Duty Accuracy 3	D_{TOUT3}	-3.58	0.00	+3.58	%	TO1=TO2=2.75 V (Duty=61.43 %), SYNC=20 kHz
TOUT Duty Accuracy 4	D_{TOUT4}	-4.27	0.00	+4.27	%	TO1=TO2=3.50 V (Duty=90.00 %), SYNC=20 kHz
High Selector Accuracy	V_{HS}	-7	0	+7	mV	Design guarantee
Internal Triangular Wave Frequency	f_{TRI}	8	10	14	kHz	Design guarantee
TOUT Delay Time	t_{TOUT}	-	-	15	ms	Design guarantee f_{SYNC}=20 kHz
TOUT ON Resistance (Source side)	R_{ONTH}	-	60	160	Ω	I_{TOUT}=-1 mA
TOUT ON Resistance (Sink side)	R_{ONTL}	-	60	160	Ω	I_{TOUT}=1 mA
TOx Disconnected Detection Voltage	V_{TOH}	7	8	9	V	TOx=TO1, TO2
OSC Oscillation Frequency	f_{OSC}	17.5	20.0	22.5	kHz	R_{RT}=100 kΩ
OSC ON Resistance (Source side)	R_{ONOSCH}	-	60	160	Ω	I_{OSC}=-1 mA
OSC ON Resistance (Sink side)	R_{ONOSCL}	-	60	160	Ω	I_{OSC}=1 mA
External Synchronization Frequency	f_{SYNC}	-	20	-	kHz	SYNC=20 kHz
External Synchronization Delay Time	t_{SYNC}	60	-	350	ns	

Electrical Characteristics-continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Protective Function						
Primary Side UVLO OFF Voltage	V_{UV1H}	4.05	4.25	4.45	V	
Primary Side UVLO ON Voltage	V_{UV1L}	3.95	4.15	4.35	V	
Primary Side UVLO Hysteresis	V_{HYSUV1}	0.05	0.1	0.15	V	
Primary Side UVLO Delay Time (OUT1H, OUT1L)	t_{UV1OUT}	2	10	30	μs	
Primary Side UVLO Delay Time (FLT1, FLT2)	t_{UV1FLT}	2	10	30	μs	
Secondary Side UVLO OFF Voltage	V_{UV2H}	11.9	12.5	13.1	V	
Secondary Side UVLO ON Voltage	V_{UV2L}	11.4	12.0	12.6	V	
Secondary Side UVLO Hysteresis	V_{HYSUV2}	0.25	0.50	0.75	V	
Secondary Side UVLO Delay Time (OUT1H, OUT1L)	t_{UV2OUT}	2	10	30	μs	
Secondary Side UVLO Delay Time (FLT1, FLT2)	t_{UV2FLT}	3	-	65	μs	
Short Circuit Detection Voltage	V_{SCDET}	0.540	0.600	0.660	V	
Short Circuit Detection Delay Time (OUT1H, OUT1L)	t_{SCOUT}	160	330	500	ns	
Short Circuit Detection Delay Time (FLT1, FLT2)	t_{SCFLT}	1	-	35	μs	
Overcurrent Detection Voltage	V_{OCDET}	0.282	0.300	0.318	V	
Overcurrent Detection Delay Time (OUT1H, OUT1L)	t_{OCOUT}	7	10	13	μs	
Overcurrent Detection Delay Time (FLT1, FLT2)	t_{OCFLT}	8	-	48	μs	
Overheat Detection Voltage	V_{TO}	1.25	1.32	1.39	V	
Overheat Detection Delay Time (OUT1H, OUT1L)	t_{TOOUT}	160	330	500	ns	
Overheat Detection Delay Time (FLT1, FLT2)	t_{TOFLT}	1	-	35	μs	
FLT ON Resistance	R_{ONFLT}	-	3.7	10	Ω	I_{FLT} =10 mA
Fault Release Delay Time	t_{RLS}	100	-	330	μs	
FLTRLS Threshold	V_{FLTRLS}	0.64 x V_{CC1} -0.1	0.64 x V_{CC1}	0.64 x V_{CC1} +0.1	V	
FLTRLS Discharge Switch ON Resistance	$R_{ONFLTRLS}$	-	3.7	10	Ω	I_{FLTRLS} =10 mA
FLTRLS Leak Current	$I_{LFLTRLS}$	-1	0	+1	μA	

Typical Performance Curves

(Reference data)

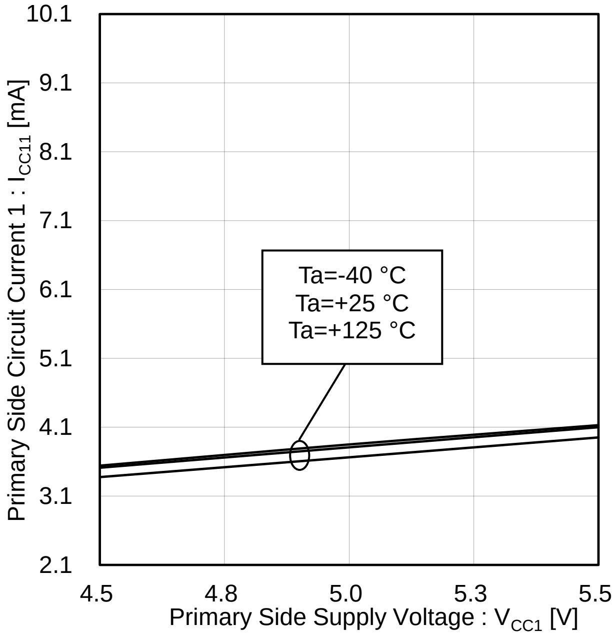


Figure 3. Primary Side Circuit current 1 vs Primary Side Supply Voltage (OUT=L)

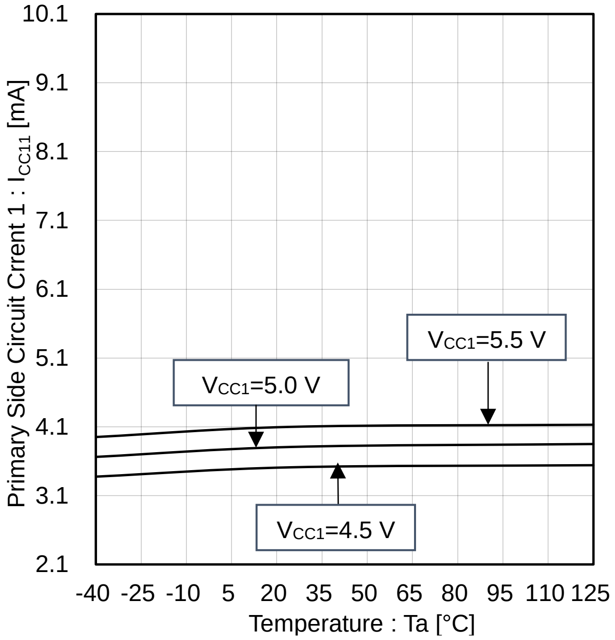


Figure 4. Primary Side Circuit Current 1 vs Temperature (OUT=L)

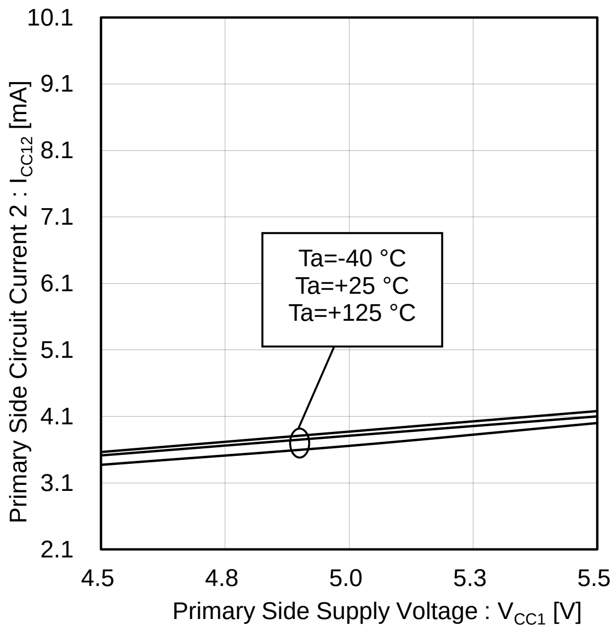


Figure 5. Primary Side Circuit Current 2 vs Primary Side Supply Voltage (OUT=H)

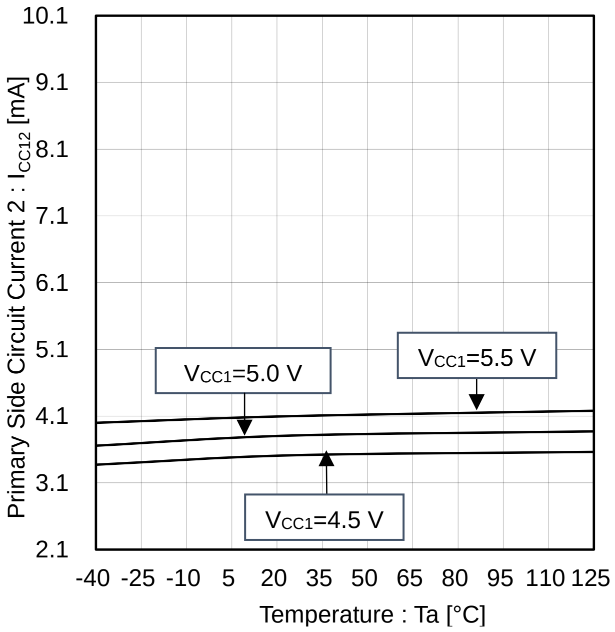


Figure 6. Primary Side Circuit Current 2 vs Temperature (OUT=H)

Typical Performance Curves - continued
(Reference data)

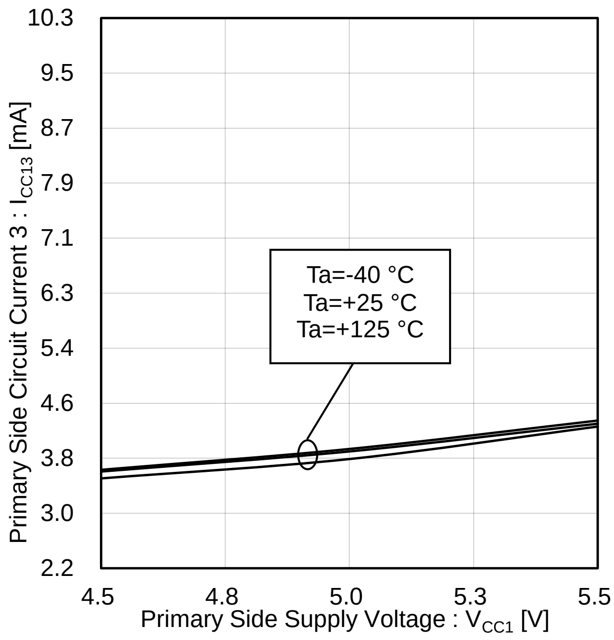


Figure 7. Primary Side Circuit Current 3 vs Primary Side Supply Voltage
(INA=10 kHz, Duty=50 %)

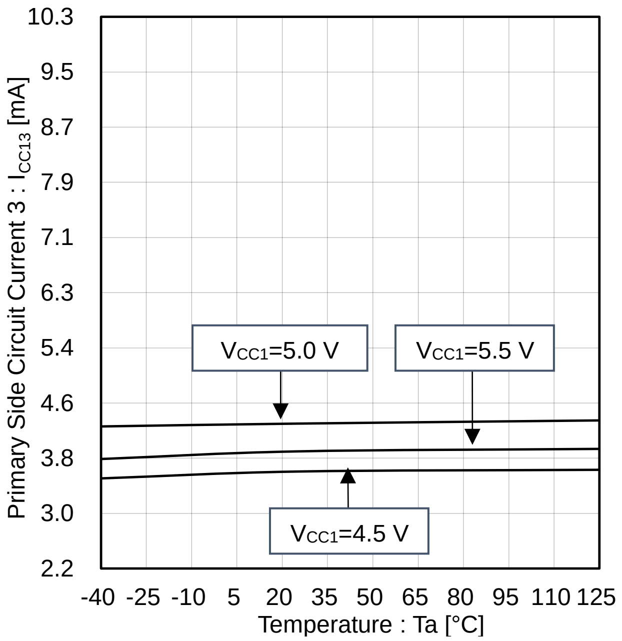


Figure 8. Primary Side Circuit Current 3 vs Temperature
(INA=10 kHz, Duty=50 %)

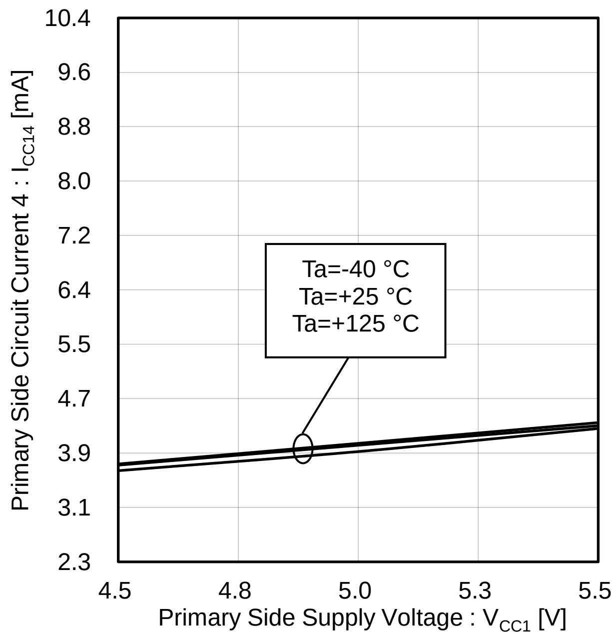


Figure 9. Primary Side Circuit Current 4 vs Primary Side Supply Voltage
(INA=20 kHz, Duty=50 %)

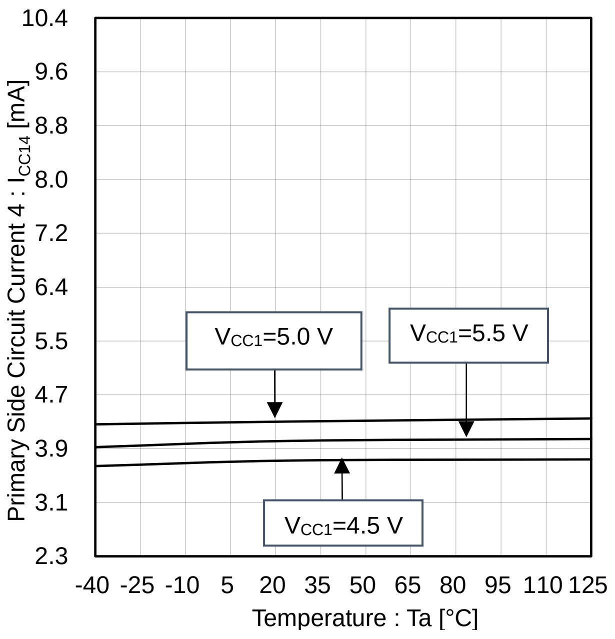


Figure 10. Primary Side Circuit Current 4 vs Temperature
(INA=20 kHz, Duty=50 %)

Typical Performance Curves - continued
(Reference data)

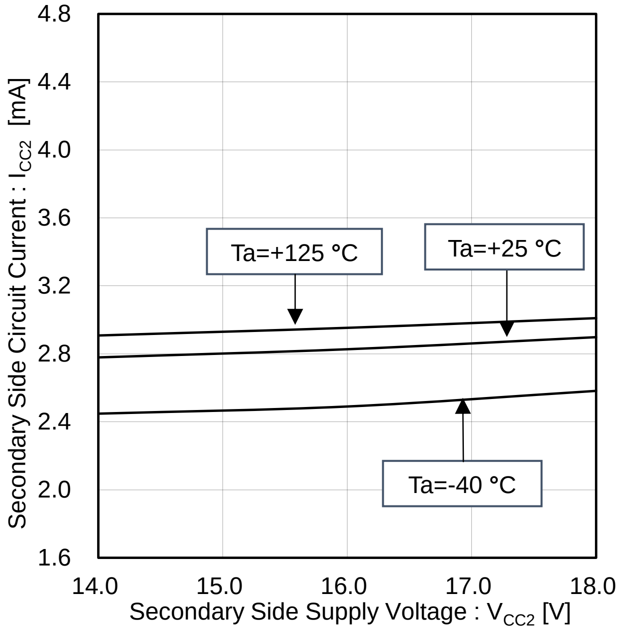


Figure 11. Secondary Side Circuit Current vs Secondary Side Supply Voltage

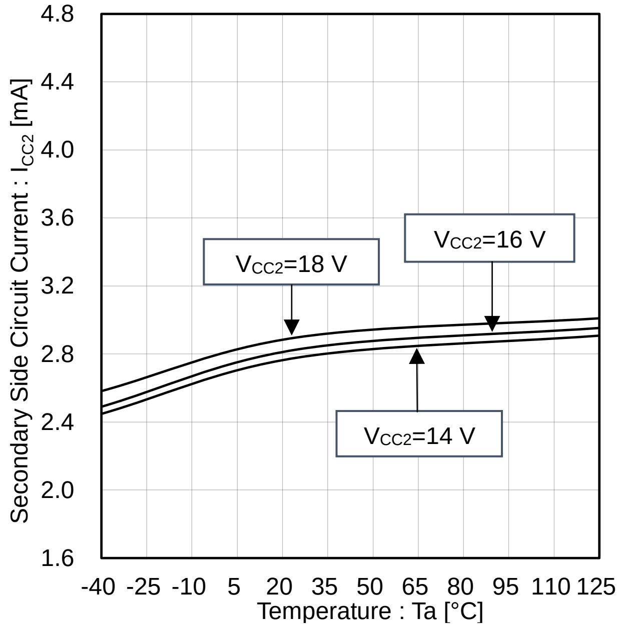


Figure 12. Secondary Side Circuit Current vs Temperature

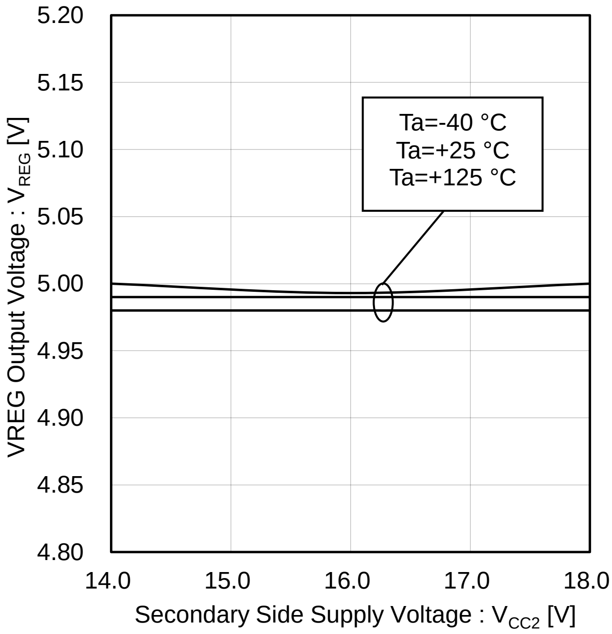


Figure 13. VREG Output Voltage vs Secondary Side Supply Voltage

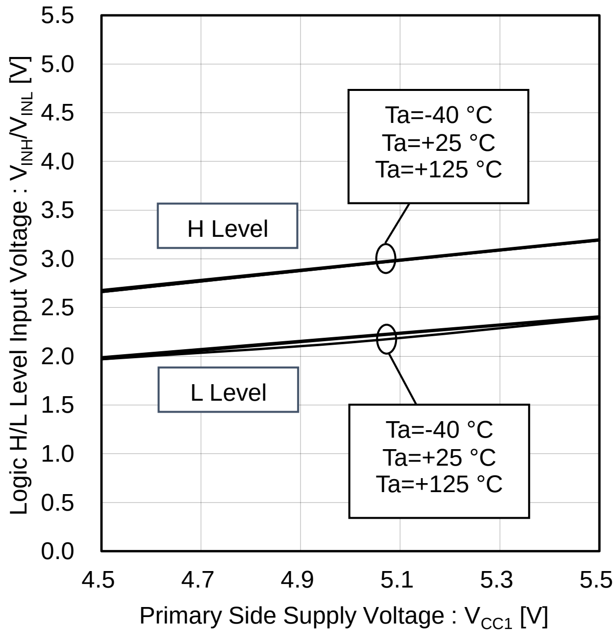


Figure 14. Logic H/L Level Input Voltage vs Primary Side Supply Voltage
(INA, INB, SSDIN, SYNC)

Typical Performance Curves - continued

(Reference data)

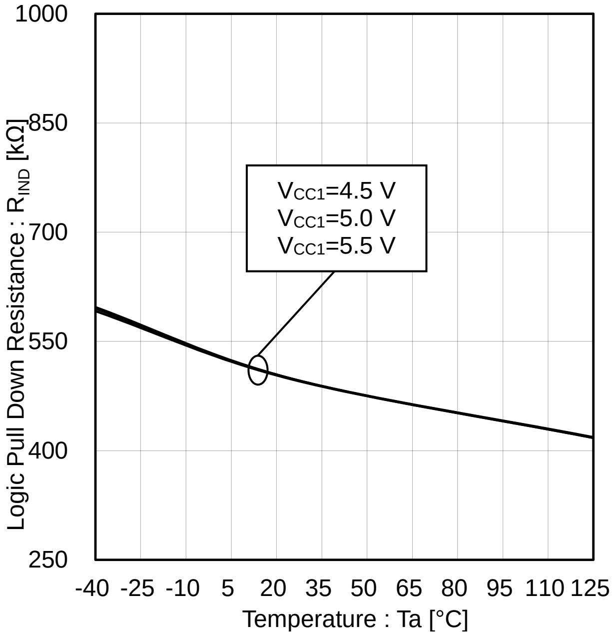


Figure 15. Logic Pull Down Resistance vs Temperature (INA, SSDIN, SYNC)

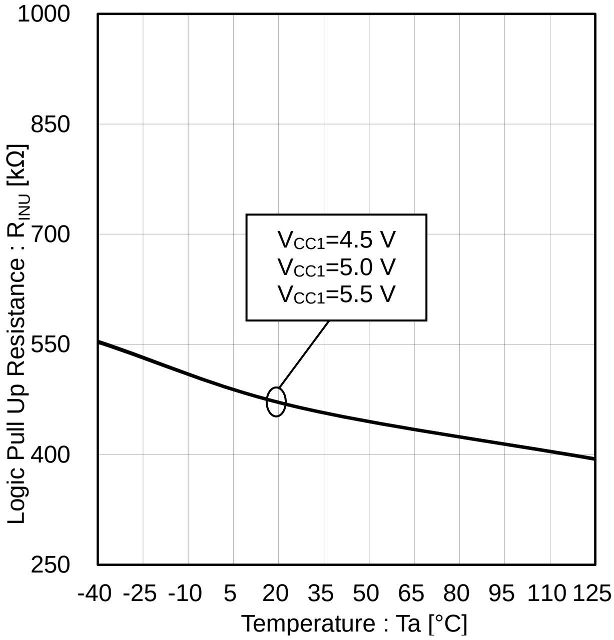


Figure 16. Logic Pull Up Resistance vs Temperature (INB)

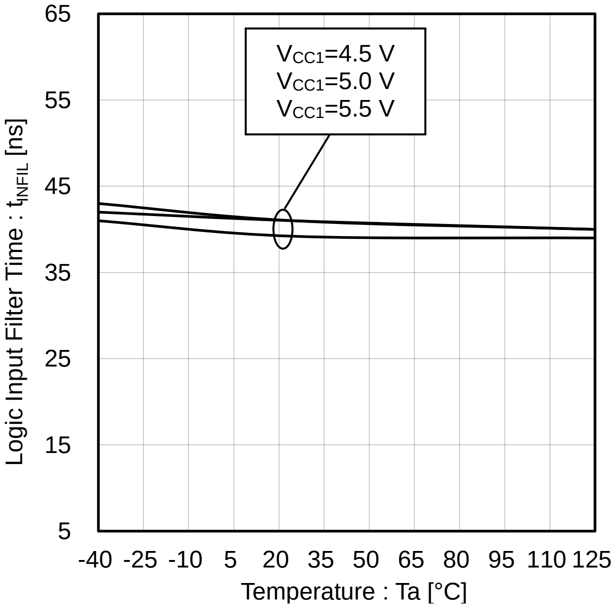


Figure 17. Logic Input Filter Time vs Temperature (INA, INB, SSDIN)

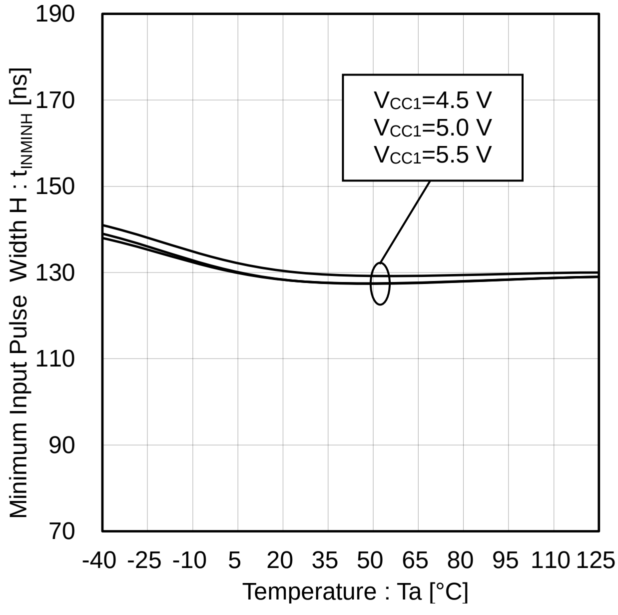


Figure 18. Minimum Input Pulse Width H vs Temperature (INA, INB)

Typical Performance Curves - continued
(Reference data)

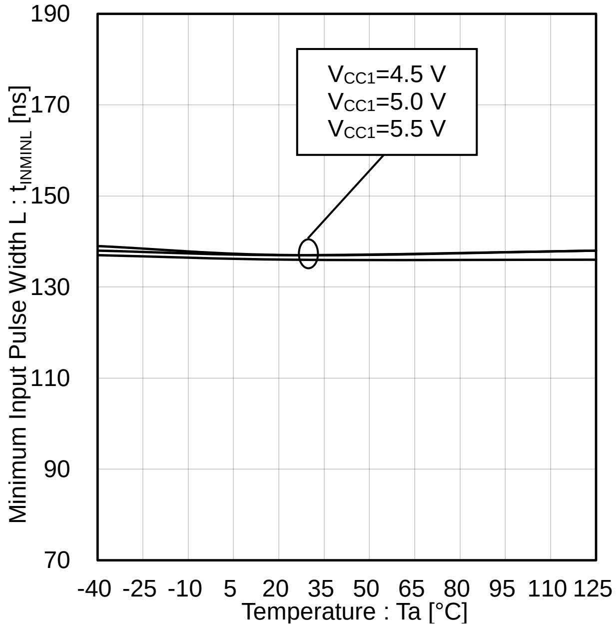


Figure 19. Minimum Input Pulse Width L vs Temperature (INA, INB)

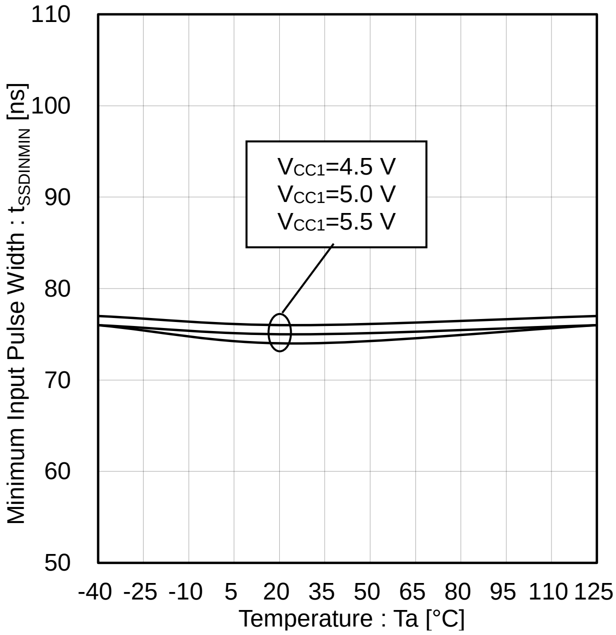


Figure 20. Minimum Input Pulse Width vs Temperature (SSDIN)

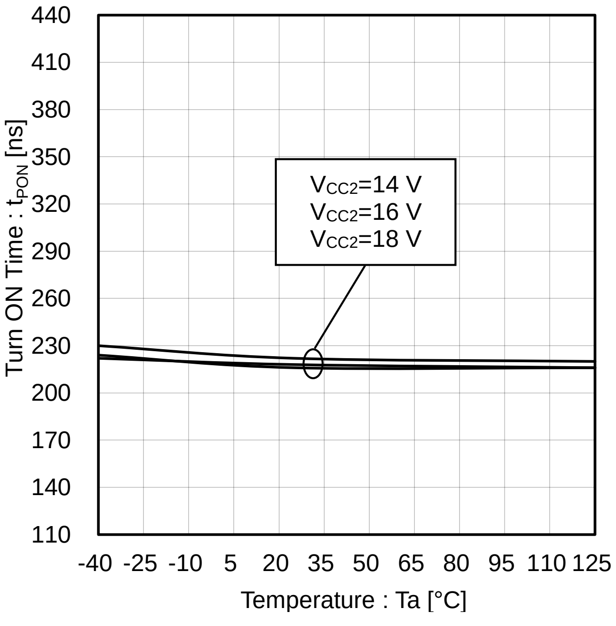


Figure 21. Turn ON Time vs Temperature

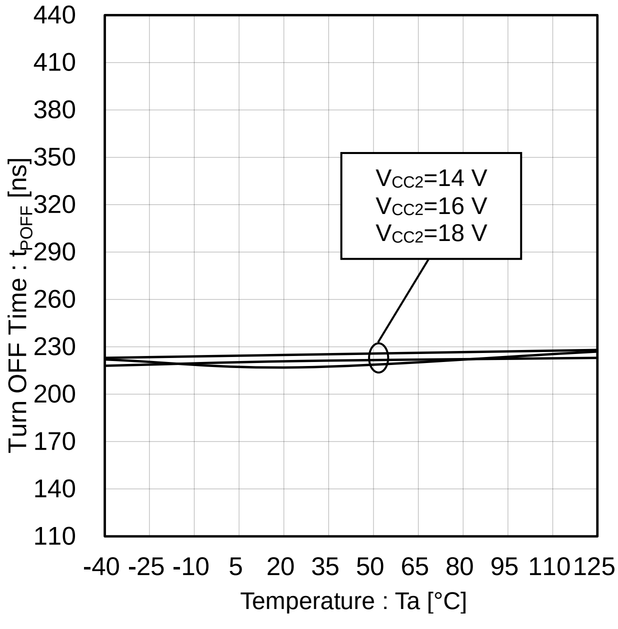


Figure 22. Turn OFF Time vs Temperature

Typical Performance Curves - continued

(Reference data)

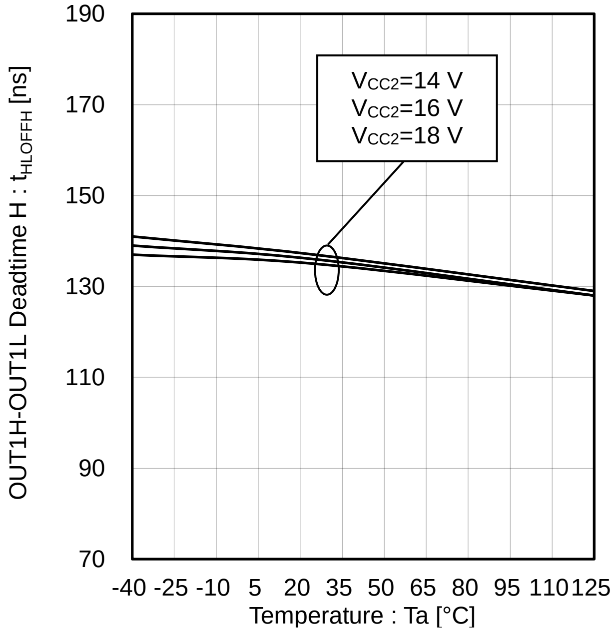


Figure 23. OUT1H-OUT1L Deadtime H vs Temperature (Output L to H)

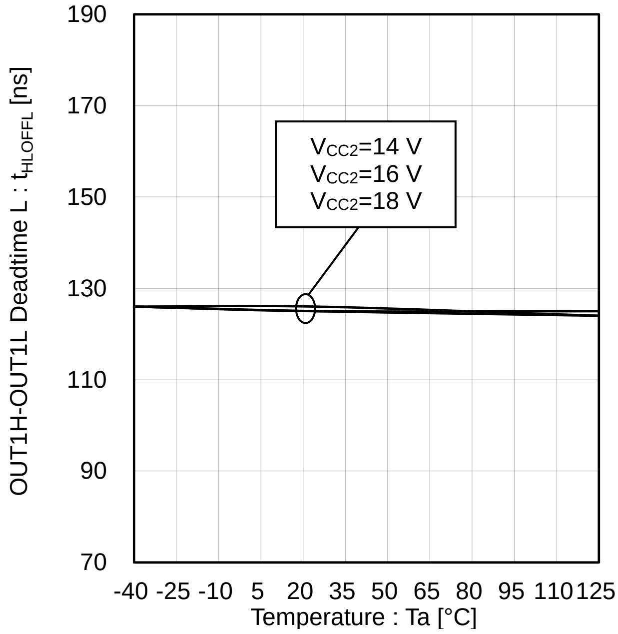


Figure 24. OUT1H-OUT1L Deadtime L vs Temperature (Output H to L)

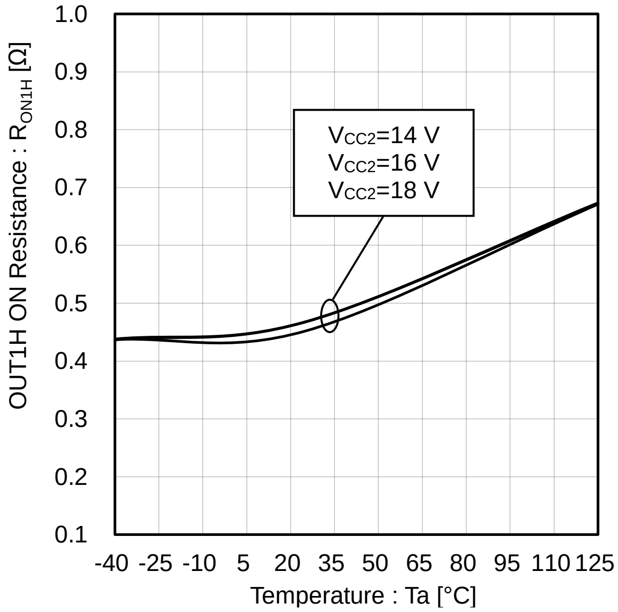


Figure 25. OUT1H ON Resistance vs Temperature

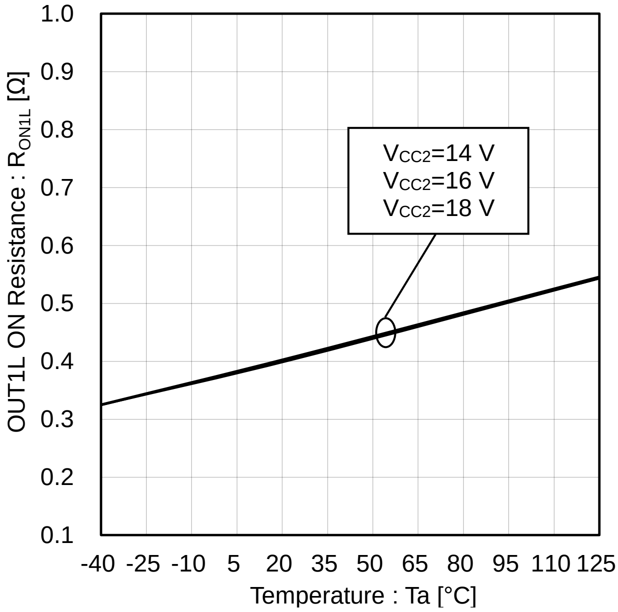


Figure 26. OUT1L ON Resistance vs Temperature

Typical Performance Curves - continued

(Reference data)

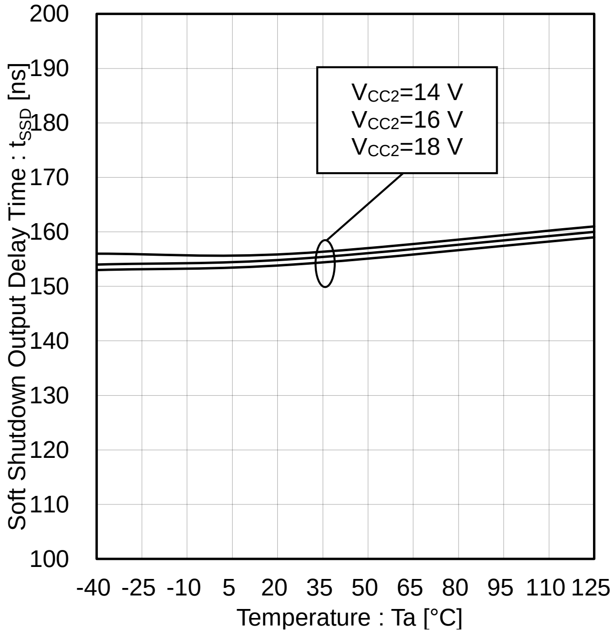


Figure 27. Soft Shutdown Output Delay Time vs Temperature

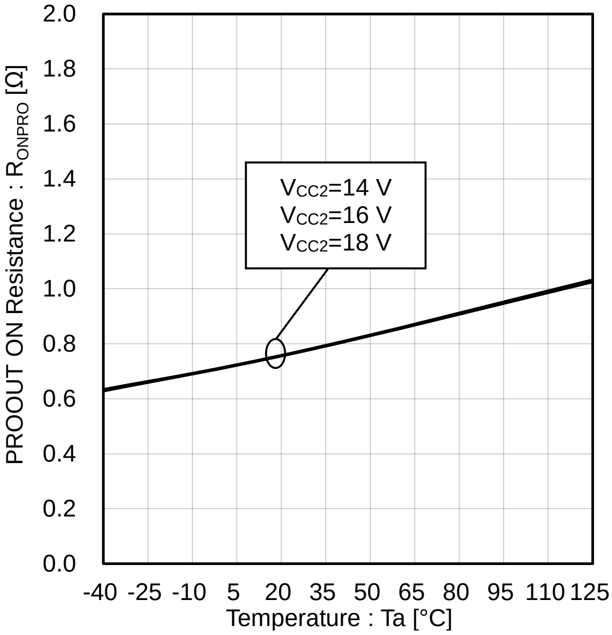


Figure 28. PROOUT ON Resistance vs Temperature

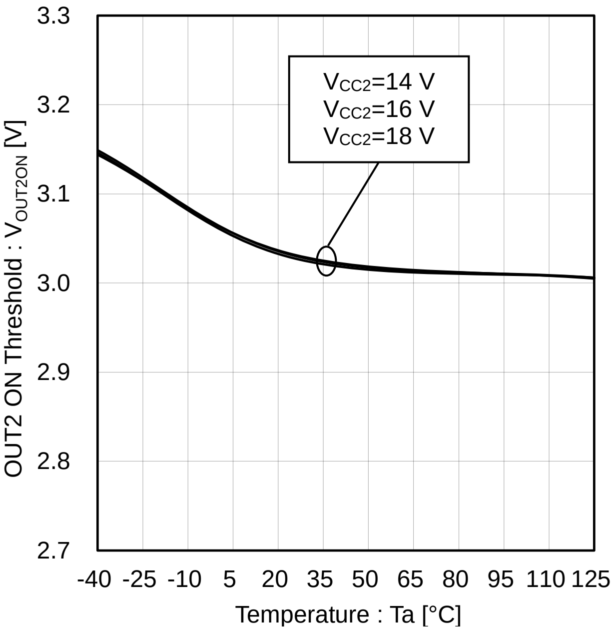


Figure 29. OUT2 ON Threshold vs Temperature

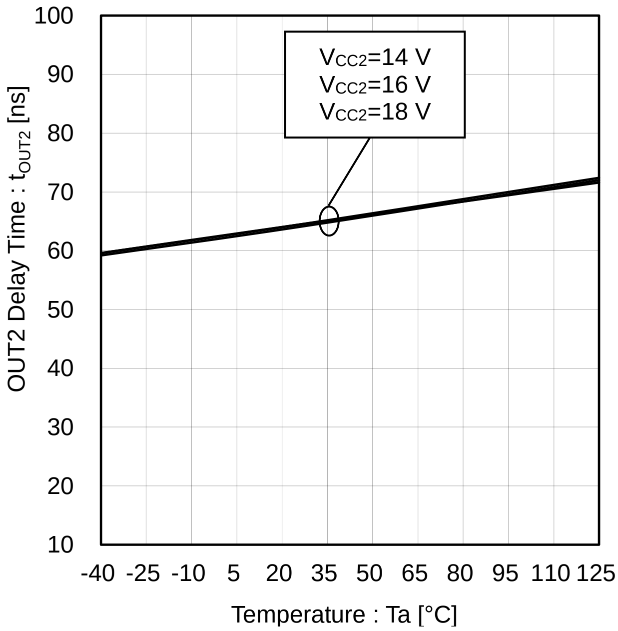


Figure 30. OUT2 Delay Time vs Temperature

Typical Performance Curves - continued

(Reference data)

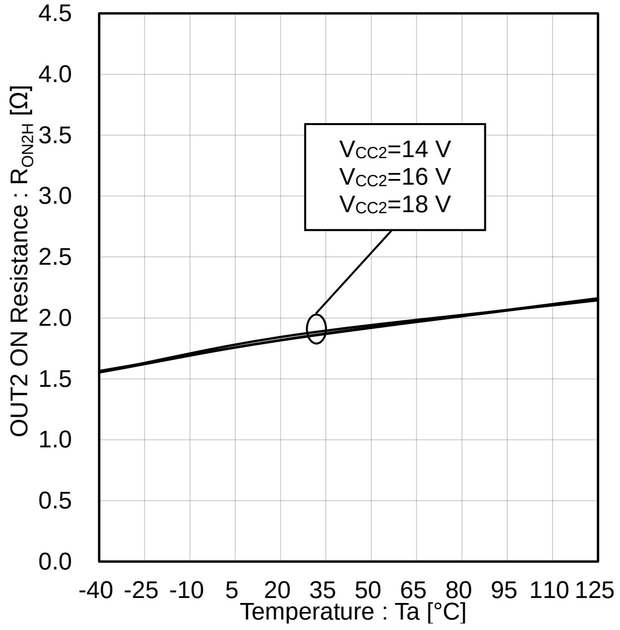


Figure 31. OUT2 ON Resistance vs Temperature (Source)

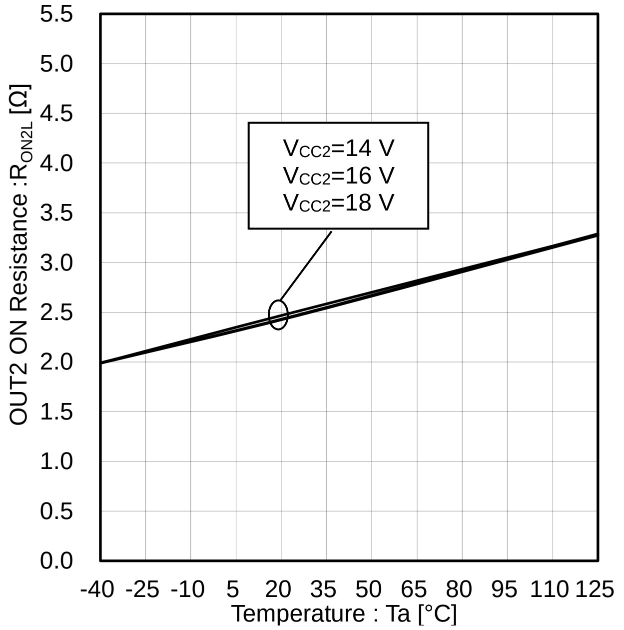


Figure 32. OUT2 ON Resistance vs Temperature (Sink)

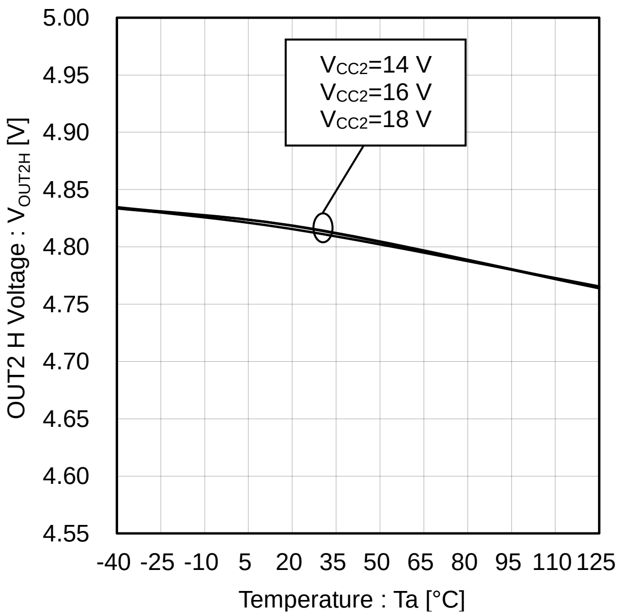


Figure 33. OUT2 H Voltage vs Temperature

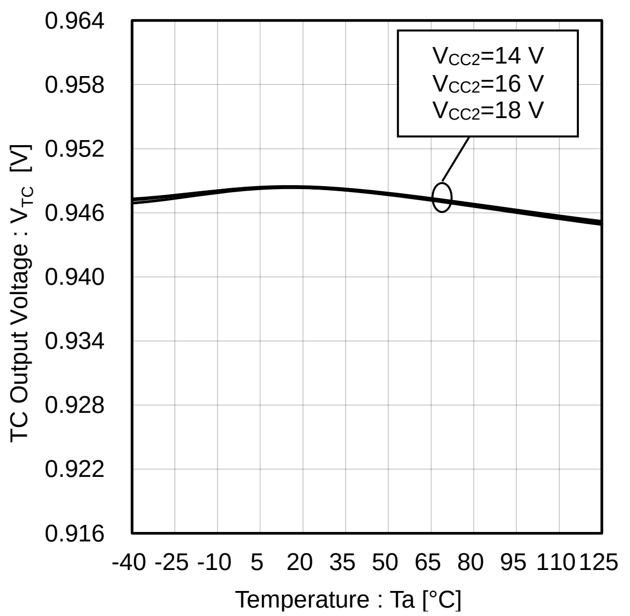


Figure 34. TC Output Voltage vs Temperature

Typical Performance Curves - continued

(Reference data)

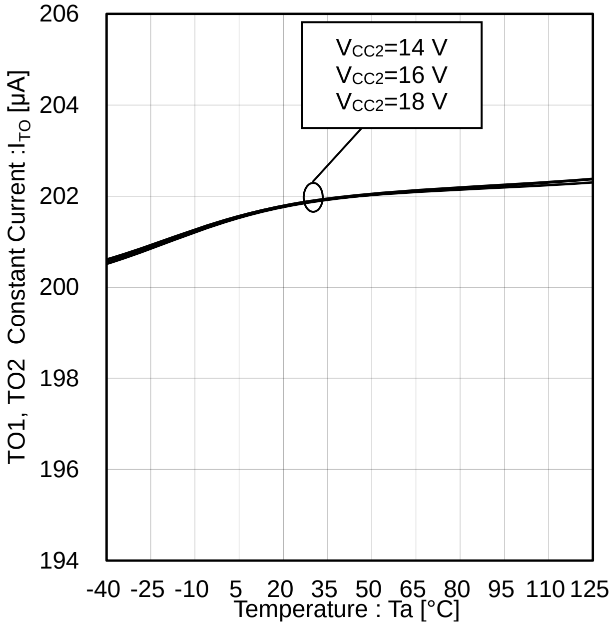


Figure 35. TO1, TO2 Constant Current vs Temperature

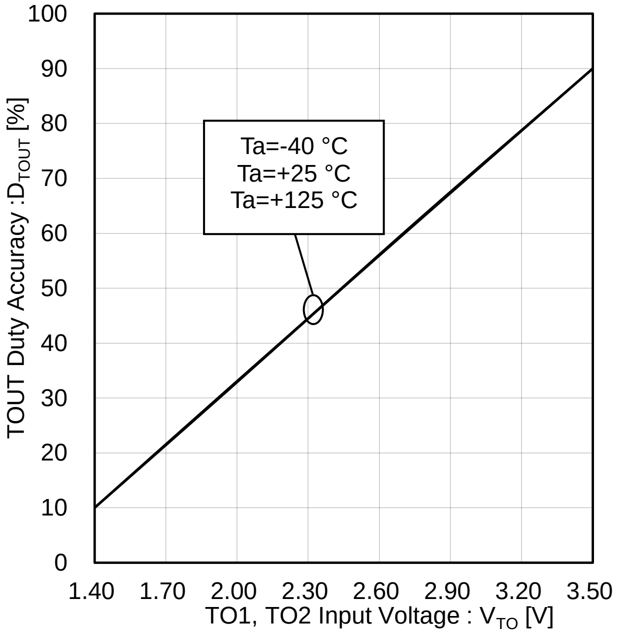


Figure 36. TOUT Duty Accuracy vs TO1, TO2 Input Voltage

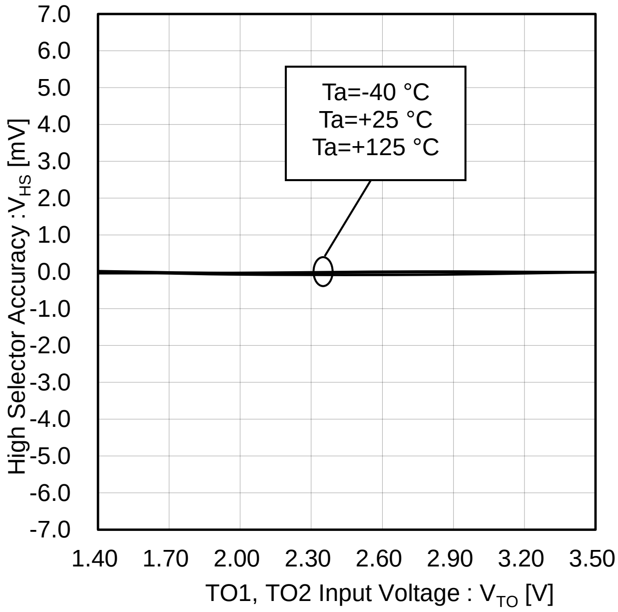


Figure 37. High Selector Accuracy vs TO1, TO2 Input Voltage

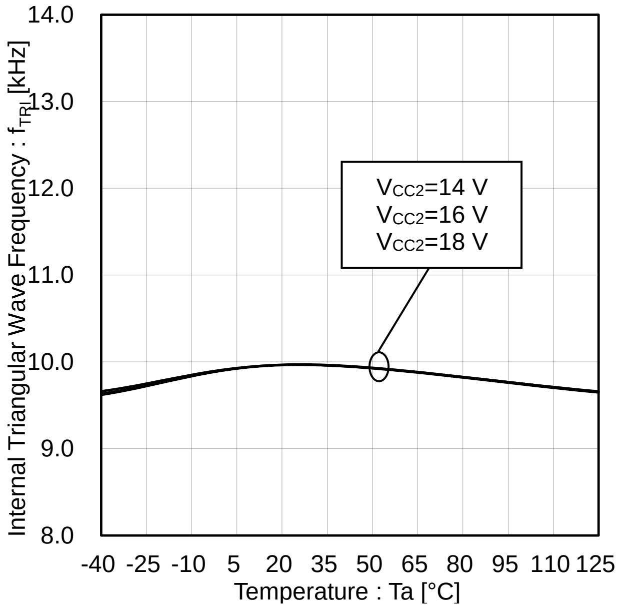


Figure 38. Internal Triangular Wave Frequency vs Temperature

Typical Performance Curves - continued
(Reference data)

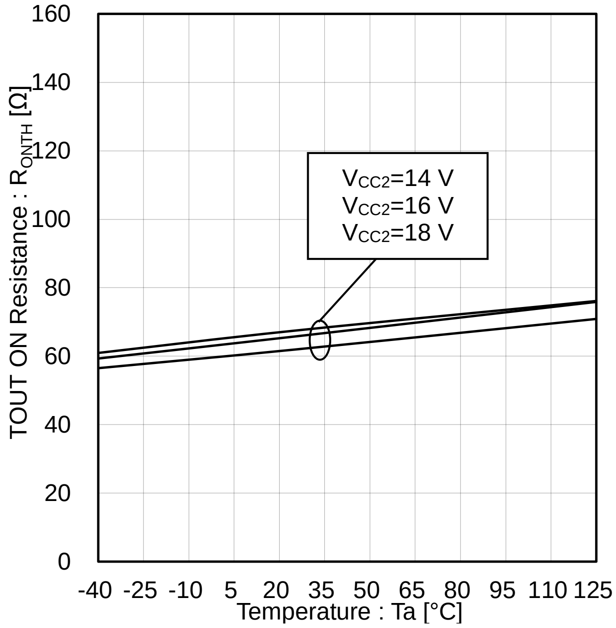


Figure 39. TOUT ON Resistance vs Temperature (Source)

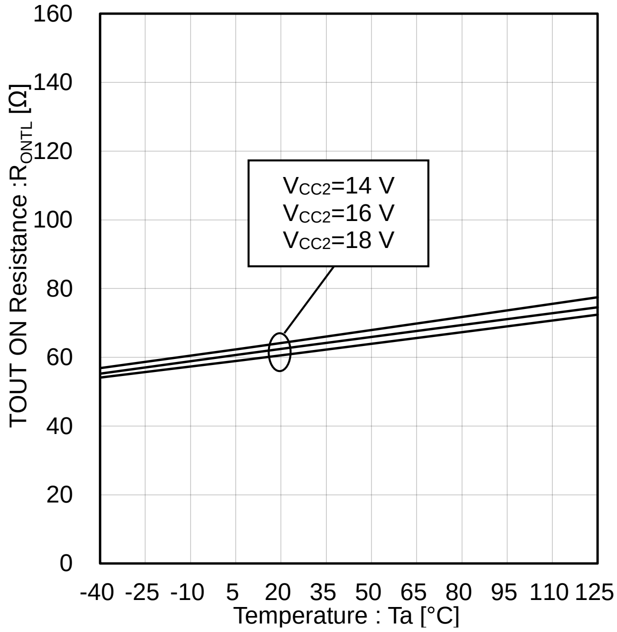


Figure 40. TOUT ON Resistance vs Temperature (Sink)

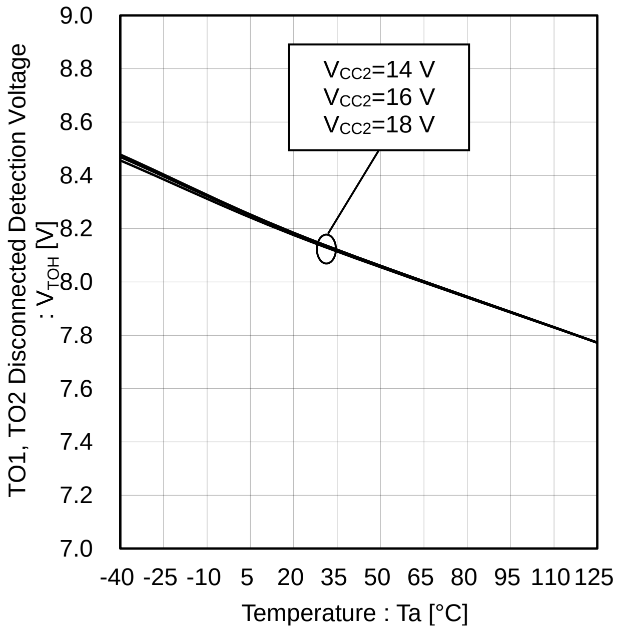


Figure 41. TO1, TO2 Disconnected Detection Voltage vs Temperature

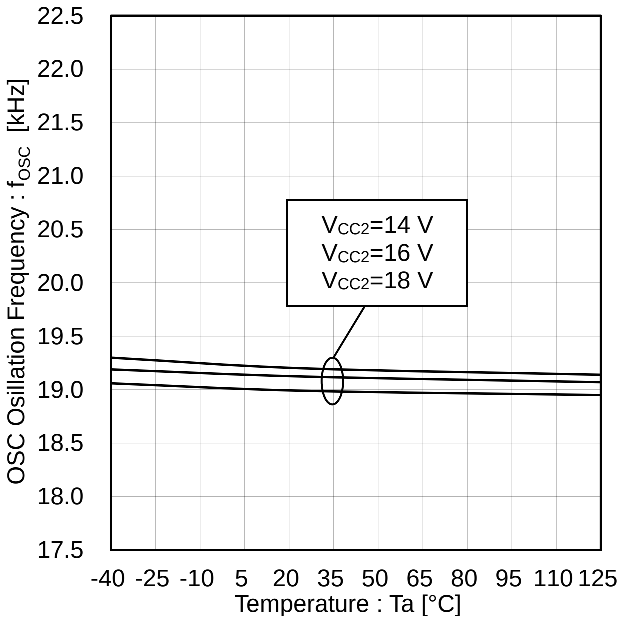


Figure 42. OSC Oscillation Frequency vs Temperature

Typical Performance Curves - continued

(Reference data)

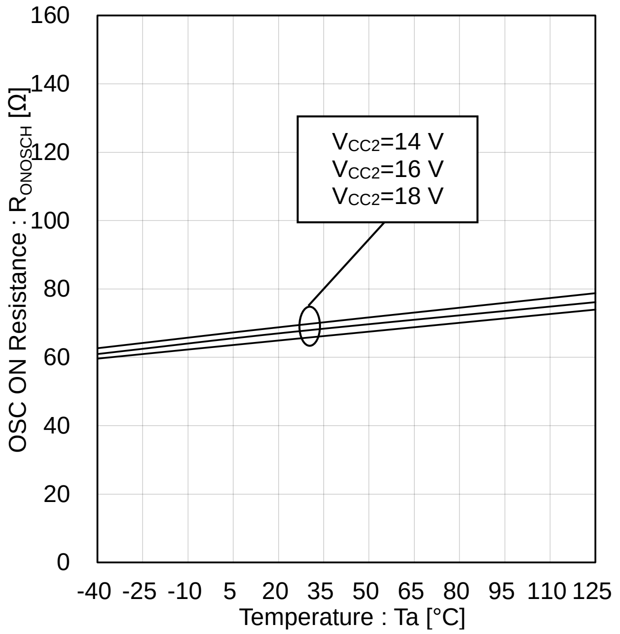


Figure 43. OSC ON Resistance vs Temperature (Source)

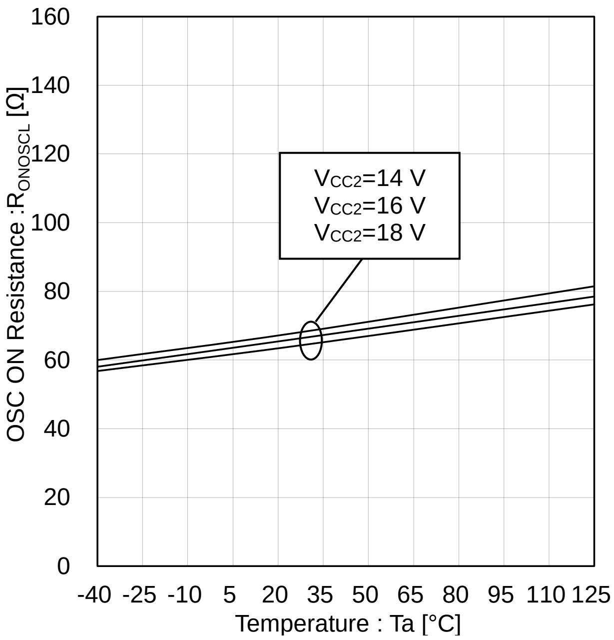


Figure 44. OSC ON Resistance vs Temperature (Sink)

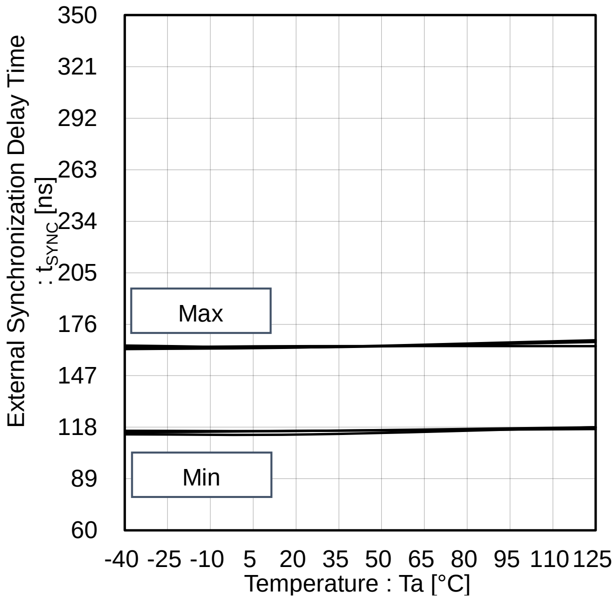


Figure 45. External Synchronization Delay Time vs Temperature

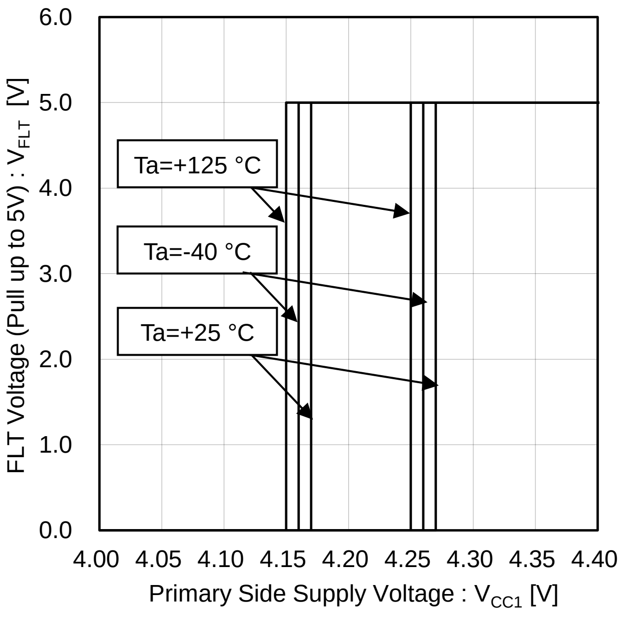


Figure 46. FLT Voltage vs Primary Side Supply Voltage (Primary Side UVLO ON/OFF Voltage)

Typical Performance Curves - continued

(Reference data)

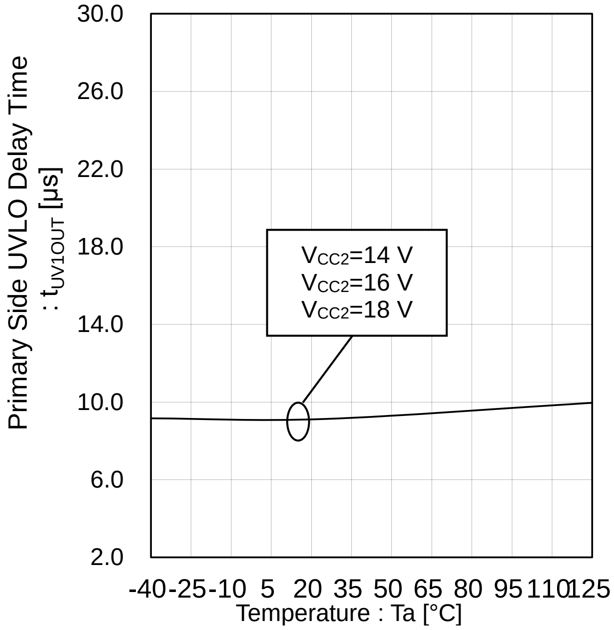


Figure 47. Primary Side UVLO Delay Time vs Temperature (OUT1H, OUT1L)

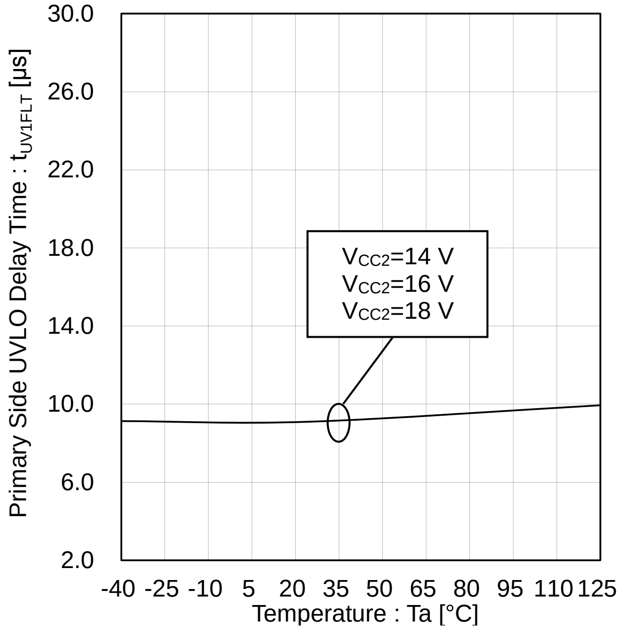


Figure 48. Primary Side UVLO Delay Time vs Temperature (FLT1, FLT2)

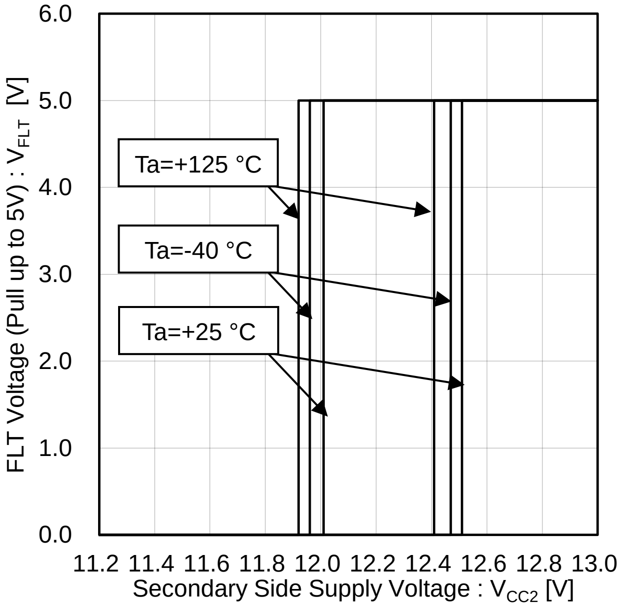


Figure 49. FLT Voltage vs Secondary Side Supply Voltage (Secondary Side UVLO ON/OFF Voltage)

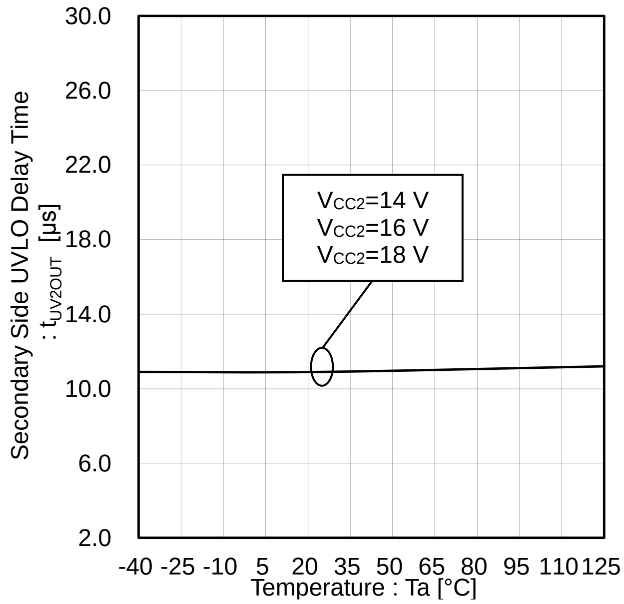


Figure 50. Secondary Side UVLO Delay Time vs Temperature (OUT1H, OUT1L)

Typical Performance Curves - continued

(Reference data)

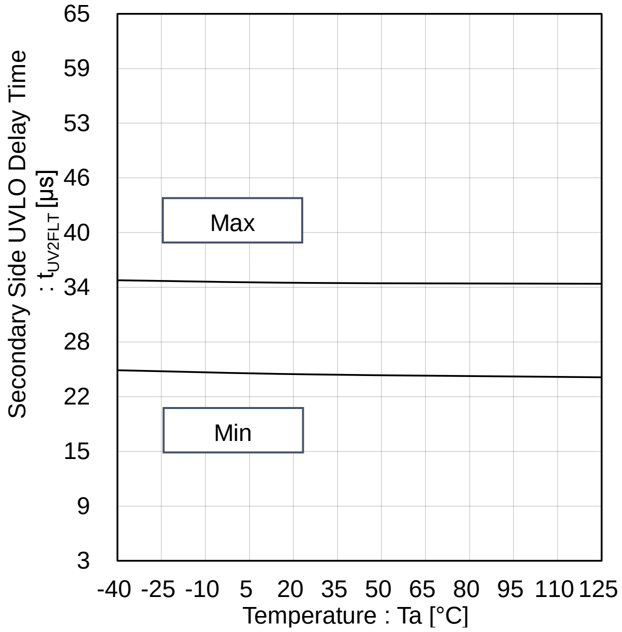


Figure 51. Secondary Side UVLO Delay Time vs Temperature (FLT1, FLT2)

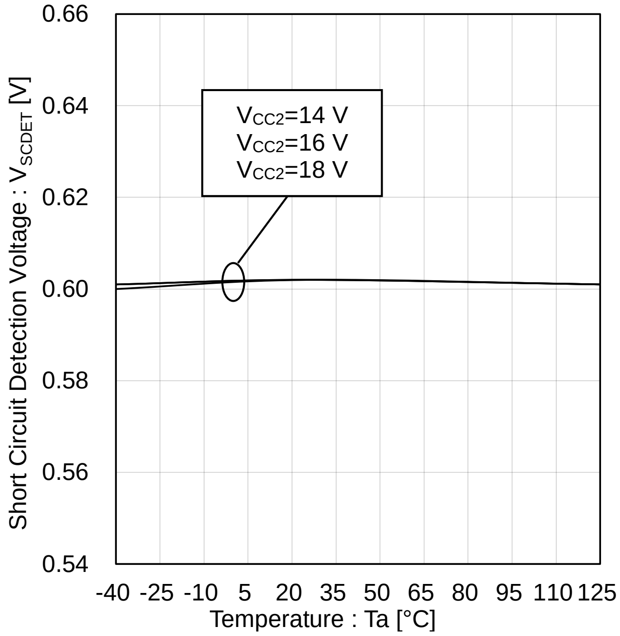


Figure 52. Short Circuit Detection Voltage vs Temperature

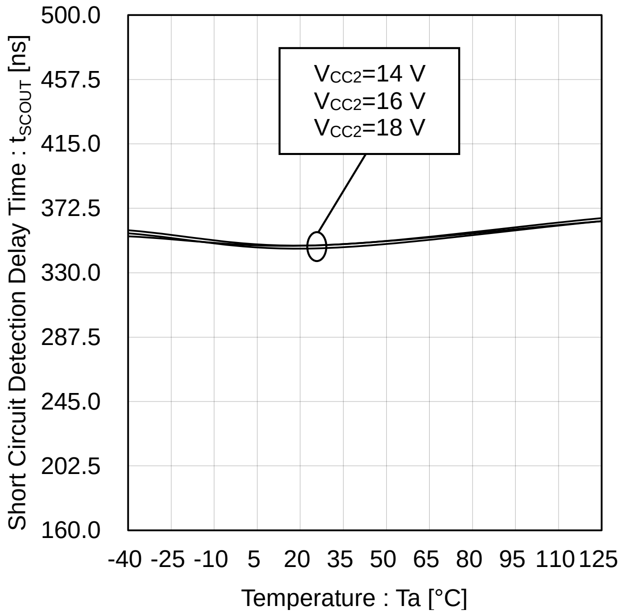


Figure 53. Short Circuit Detection Delay Time vs Temperature (OUT1H, OUT1L)

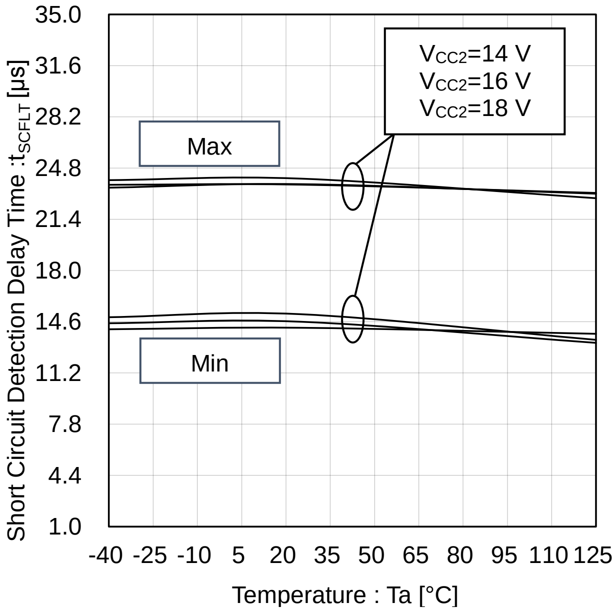


Figure 54. Short Circuit Detection Delay Time vs Temperature (FLT1, FLT2)

Typical Performance Curves - continued

(Reference data)

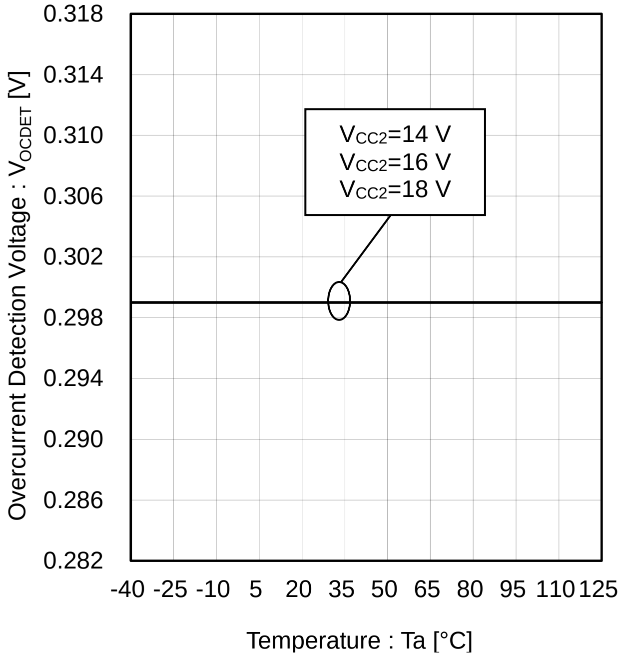


Figure 55. Overcurrent Detection Voltage vs Temperature

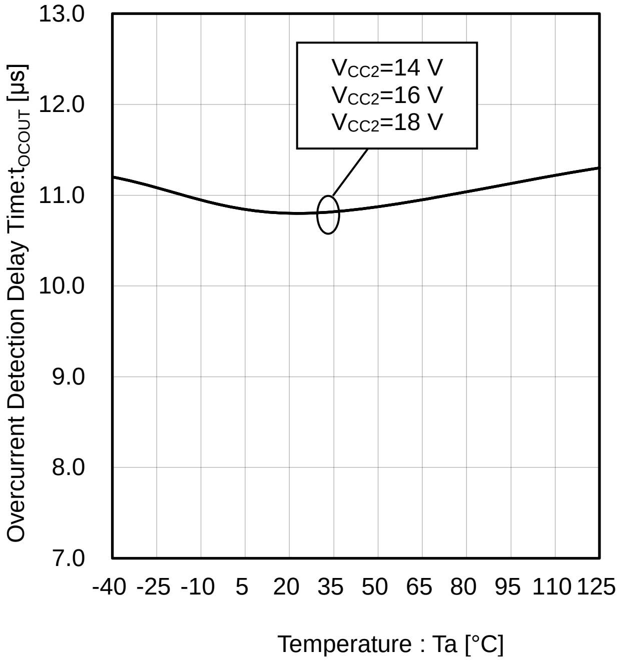


Figure 56. Overcurrent Detection Delay Time vs Temperature (OUT1H, OUT1L)

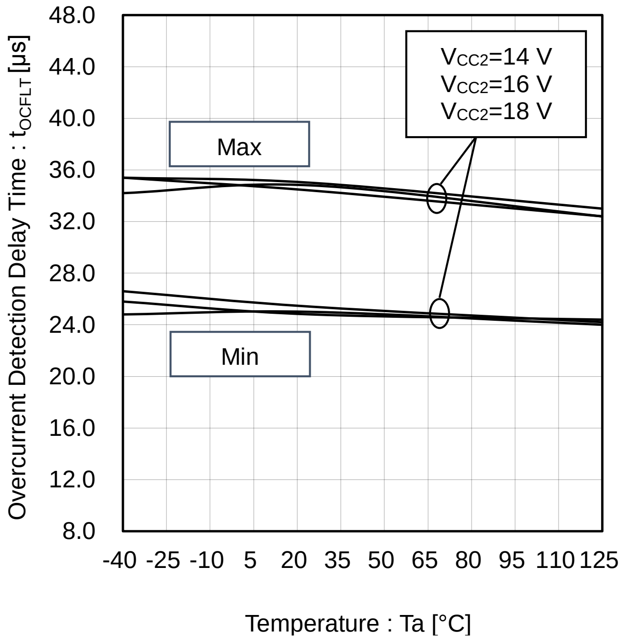


Figure 57. Overcurrent Detection Delay Time vs Temperature (FLT1, FLT2)

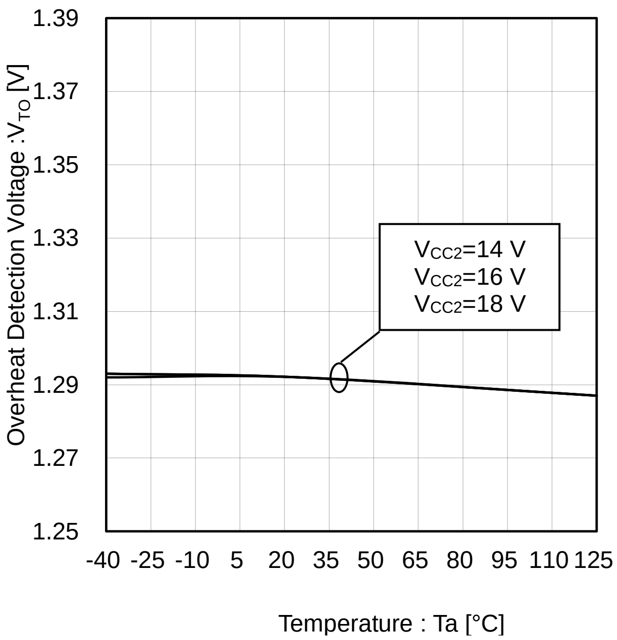


Figure 58. Overheat Detection Voltage vs Temperature

Typical Performance Curves - continued

(Reference data)

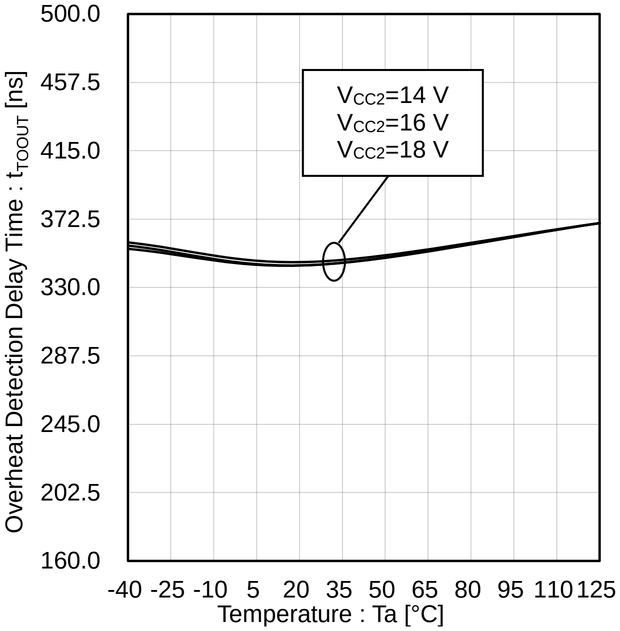


Figure 59. Overheat Detection Delay Time vs Temperature (OUT1H, OUT1L)

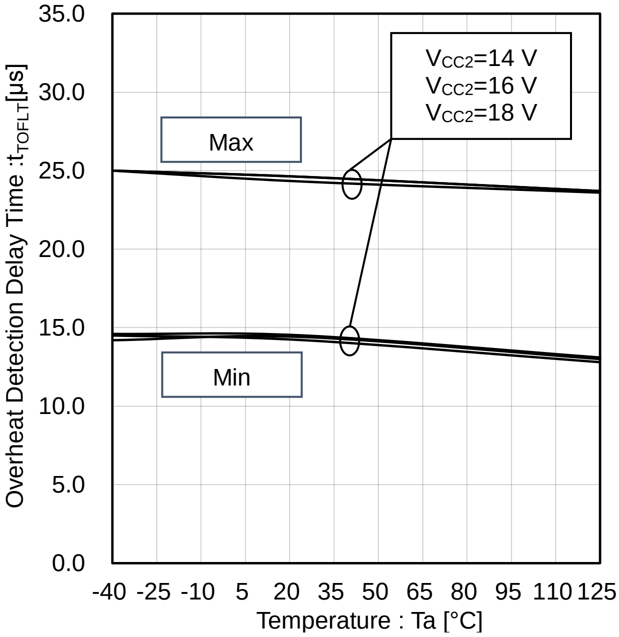


Figure 60. Overheat Detection Delay Time vs Temperature (FLT1, FLT2)

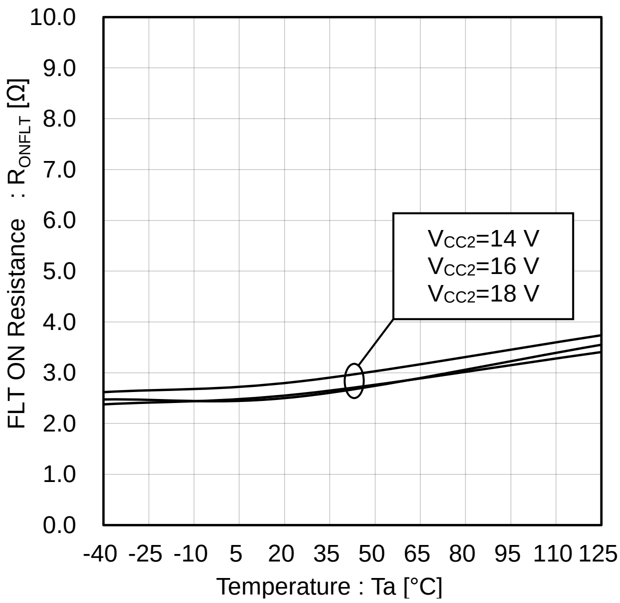


Figure 61. FLT ON Resistance vs Temperature

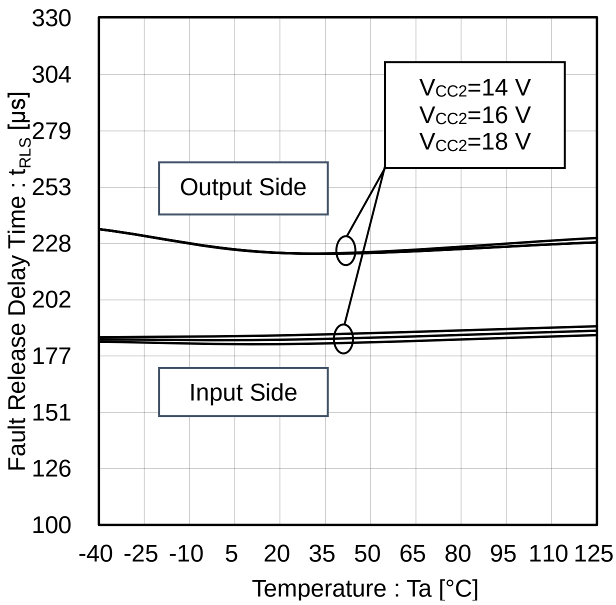


Figure 62. Fault Release Delay Time vs Temperature

Typical Performance Curves - continued
(Reference data)

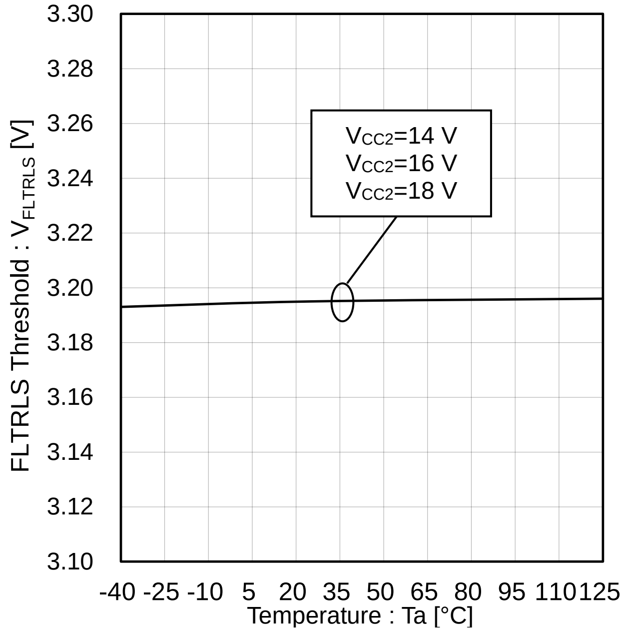


Figure 63. FLTRLS Threshold vs Temperature

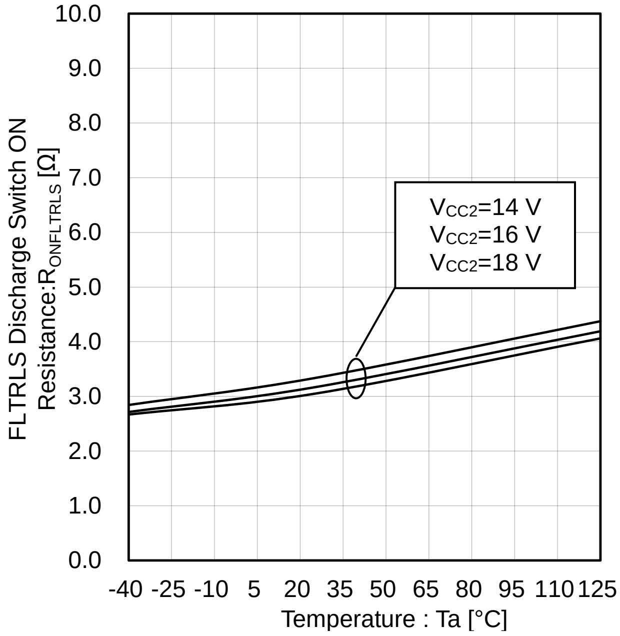


Figure 64. FLTRLS Discharge Switch ON Resistance vs Temperature

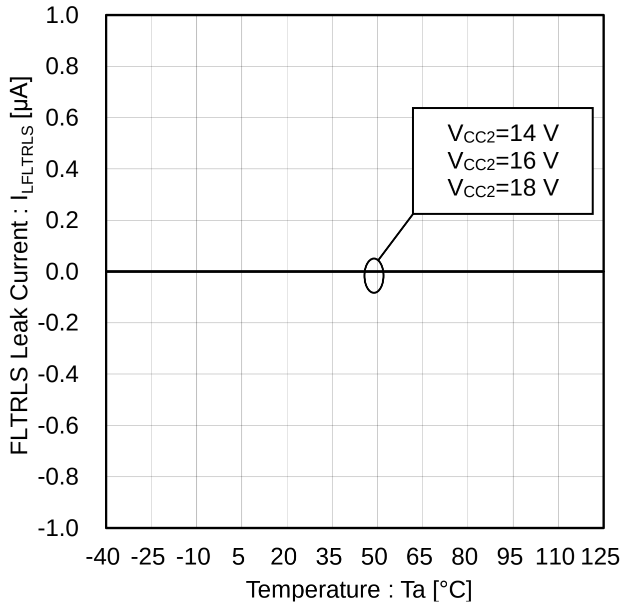


Figure 65. FLTRLS Leak Current vs Temperature

Description of Pins and Cautions on Layout of Board

1. VCC1 (Primary side power supply pin)
   This is the primary side power supply pin. Connect a bypass capacitor between the VCC1 and the GND1 pins in order to suppress voltage variations by the driving current flowing in the IC's internal transformer.

2. GND1 (Primary side ground pin)
   This is the primary side ground pin.

3. VCC2 (Secondary side power supply pin)
   This is the secondary side power supply pin. Connect a bypass capacitor between the VCC2 and the GND2 pins in order to suppress voltage variations by the driving current and output current flowing in the IC's internal transformer.

4. GND2 (Secondary side ground pin)
   This is the secondary side ground pin. Connect the output device's emitter/source to this pin.

5. VREG (Secondary side internal power supply pin)
   This is the secondary side internal power supply pin. Connect a bypass capacitor between the VREG and the GND2 pins in order to prevent oscillation.

6. INA, INB and SSDIN (Control input pins and soft shutdown control input pin)
   These are pins for determining the output logic. For SSDIN=H, OUT1L will be turned on after the miller clamp function is activated.

SSDIN	INB	INA	OUT1H	OUT1L	PROOUT
L	L	L	OFF	ON	OFF
L	L	H	ON	OFF	OFF
L	H	L	OFF	ON	OFF
L	H	H	OFF	ON	OFF
H	X	X	OFF	OFF	ON

X: Don't care

7. OUT1H and OUT1L (Source side output / Gate voltage input pin and sink side output pin)
   These are gate driving pins. For output logic, see the truth table for IN and SSDIN pins shown in item 6 above. The OUT1H pin is used also as a gate voltage input pin for the miller clamp function.

8. OUT2 (Control pin for Miller clamp)
   This is the miller clamp pin for controlling Nch MOSFET to prevent the gate voltage from rising due to the miller current flowing in the output element that is connected to the OUT1H and OUT1L pins. The OUT2 pin should be open when the miller clamp function is not used.

9. PROOUT (Soft shutdown output pin)
   This pin is used for operation of soft shutdown of the output element during short circuit protection, overcurrent protection or overheat protection.

10. SCPIN1 and SCPIN2 (Short circuit and overcurrent detection pins)
    These pins are current detection pins for short circuit and overcurrent protections. If the SCPIN1 or SCPIN2 pin voltage of V_{SCDET} or more lasts t_{SCOUT} or more, the short circuit protection function is activated. If the SCPIN1 or SCPIN2 pin voltage of V_{OCDET} or more lasts t_{OCOUT} or more, the overcircuit protection function is activated. In the open state, the IC may possibly malfunction. To avoid this risk, if the SCPIN1 pin or the SCPIN2 pin is not used, keep it connected to the GND2 pin.

11. FLT1 and FLT2 (Fault signal output pin)
    These pins are used for outputting fault signals. In the event of a fault (leading to the operation of the protection against low primary/secondary voltage (UVLO), short circuit protection (SCP), overcurrent protection (OCP) or overheat protection (OT)), the Nch MOS FET inserted between FLT1 and FLT2 pins will be turned OFF.

State	FLT
Normal	ON
Fault (primary side UVLO, secondary side UVLO, SCP, OCP or OT)	OFF

12. FLTRLS (Fault output holding time setup pin)
    This pin is used for specifying the holding time of a fault signal. Connect a capacitor between GND1 pin. Connect resistor between the VCC1 pin.
    A fault signal is retained until the FLTRLS pins voltage reaches V_{FLTRLS} or higher. If set the holding time to 0 ms, do not insert a capacitor. When it shorts to the VCC1 pin, large current flows into the FLTRLS pin and could lead to malfunction in the open state. To avoid this risk, please insert a resistor between the VCC1 pin.

Description of Pins and Cautions on Layout of Board-continued

13. TC (Constant current setting resistor connection pin)
    The TC pin has a resistor connection for setting the constant current output. By inserting arbitrary resistance between the TC and the GND2 pins, the current from the TO1 pin and the TO2 pin are set to a constant value.

14. TO1 and TO2 (Constant current output / Sensor voltage input pin)
    These are constant current output / voltage input pins. Insert impedance between the TO1 and the GND2 pins, and between the TO2 and the GND2 pins. They can be used as a sensor input. Furthermore, the TO1 pin and TO2 pin disconnect detection function is built-in.

15. TOUT (Temperature information output pin)
    This is a pin which outputs the voltage either TO1 or TO2, whichever is lower, converted to Duty cycle, in phase with the clock signal input to the SYNC pin.

16. SYNC (External clock input pin)
    This is an input pin for external clock signal. It can be connected also to the OSC pin. It contains a filter that is effective for removing noise that could lead to erroneous operation.

17. OSC (Output pin for oscillation frequency)
    This is an output pin for clock signals. Oscillation frequency is calculated by substituting the value of the resistance connected to the RT pin to the following equation.

    f_{OSC} [kHz] = 2000 / R_{RT} [kΩ]

18. RT (Oscillation frequency setup resistor connection pin)
    This pin is used for connecting a resistor that determines the oscillation frequency of the clock signal output from the OSC pin. Regardless of clock signal being used or not, insert a resistance between the RT and the GND1 pins.

Description of Functions and Examples of Constant Setting

1. Fault Status Output

When a fault occurs (the primary side or secondary side under voltage lockout function (UVLO), short circuit protection (SCP), overcurrent protection (OCP) or overheat protection (OT) occurs), the Nch MOS FET between the FLT1 and FLT2 pins are turned OFF whereby a fault signal output. The signal retains until the elapse of fault output holding time t_{FLTRLS} is cleared. The fault output holding time is determined by the following equation that consists of the capacitor C_{FLTRLS} and resistor R_{FLTRLS} connected to the FLTRSL pin, and the fault release delay time t_{RLS}.

$$t_{FLTRLS}=C_{FLTRLS} \times R_{FLTRLS} + t_{RLS}$$

State	Nch MOS FET between the FLT1 and FLT2 pins
Normal	ON
Fault	OFF

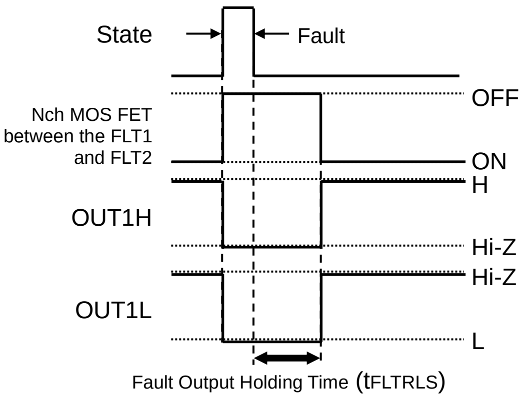
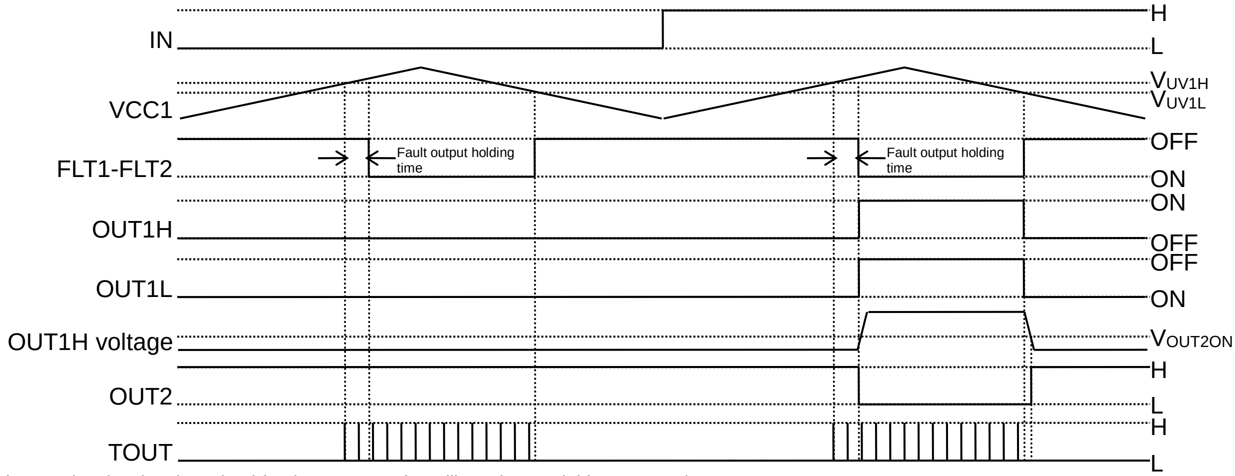


Figure 66. Fault Output Timing Chart

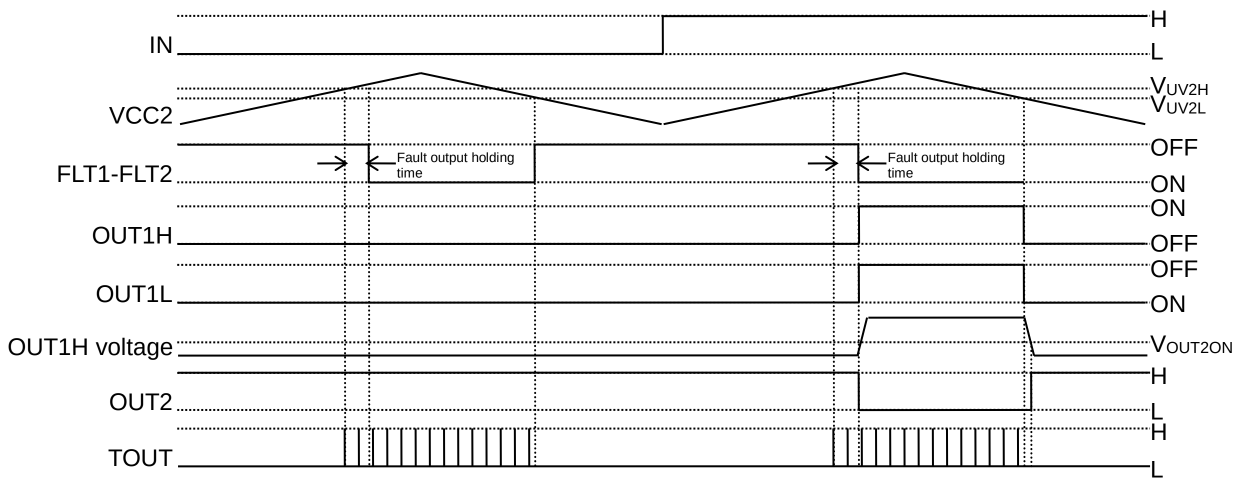
2. Under Voltage Lockout (UVLO)

Function both the primary side power supply (VCC1) and secondary side power supply (VCC2) have an under voltage lockout (UVLO) function. When the power supply voltage drops to the UVLO ON voltage, the OUT1H and OUT1L pins are turned OFF and ON respectively, and the interconnection between the FLT1 and FLT2 pins are turned OFF. When the power supply voltage rises to the UVLO OFF voltage, these pins will revert. However, during the fault output holding time as specified by item 1 above, the OUT1H and OUT1L pins remain OFF and ON respectively, and the interconnection between FLT1 and FLT2 pins remain OFF. During the operation of the under voltage lockout (UVLO) function, the miller clamp function as described by item 5 below remains effective. In addition, to remove noise that could lead to malfunction, both the primary side and secondary side power supplies have a filter.



(Note 11) Delay time is omitted for the purpose of readily understandable presentation

Figure 67. Primary Side UVLO Operation Timing Chart

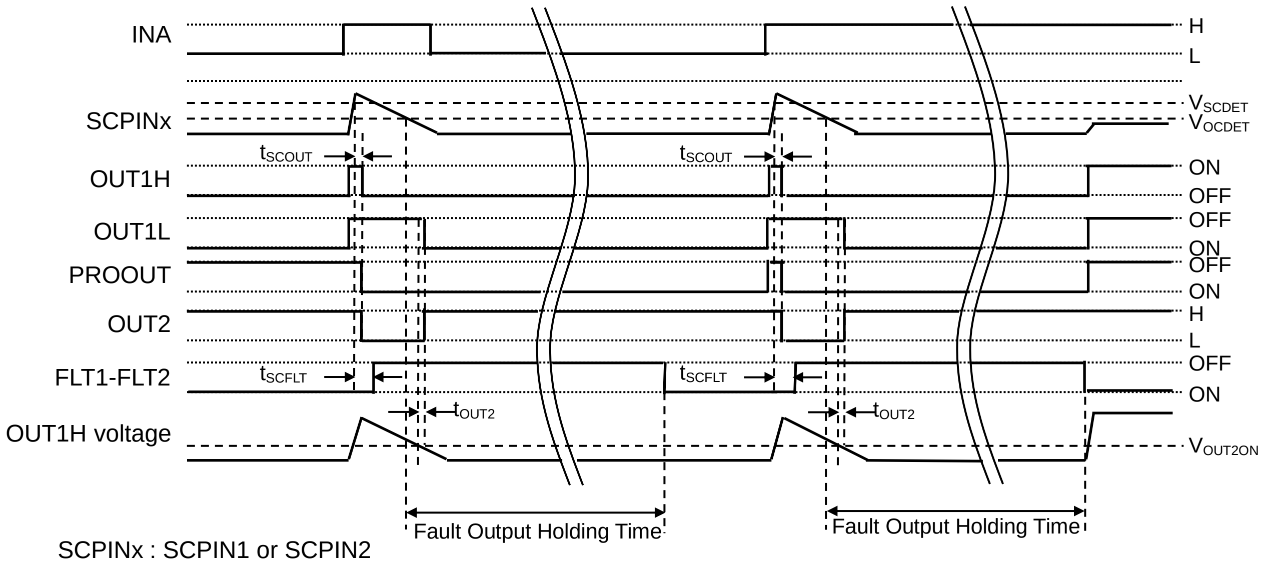


(Note 12) Delay time is omitted for the purpose of readily understandable presentation

Figure 68. Secondary Side UVLO Operation Timing Chart

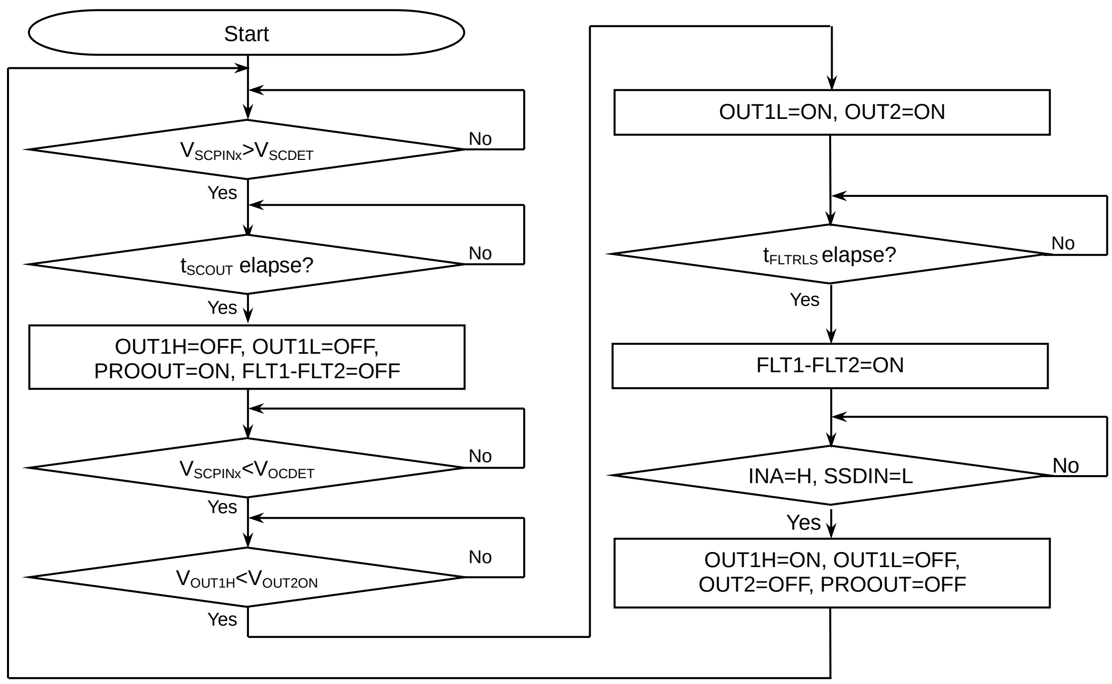
Description of Functions and Examples of Constant Setting - continued

3. Short Circuit Protection (SCP) Function
   When the SCPIN1 pin or the SCPIN2 pin voltage continues to exceed V_{SCDET} for t_{SCOUT} or more, the short circuit protection function is activated. Once the function is activated, both the OUT1H and the OUT1L pins turn OFF, the PROOUT pin turns ON, and the interconnection between the FLT1 and the FLT2 pins turn off. After the elapse of a specified fault output holding time since the voltage of both the SCPIN1 and the SCPIN2 pins decreases to V_{OCDET} or below, the short circuit protection is deactivated. However, if the INA pin = L when the function is deactivated, the PROOUT pin will remain ON until the INA pin changes to H. Even if the short circuit protection function is active, the miller clamp function as described by the item 5 below is kept available.



SCPINx : SCPIN1 or SCPIN2

Figure 69. SCP Operation Timing Chart



SCPINx : SCPIN1 or SCPIN2

Figure 70. SCP Operation Flowchart

Description of Functions and Examples of Constant Setting - continued

4. Overcurrent Protection (OCP) Function

If the SCPIN1 pin or the SCPIN2 pin voltage over V_{OCDET} lasts for t_{OCOUT} or more, the overcurrent protection function is activated. Once the function is activated, both the OUT1H and the OUT1L pins turn off, the PROOUT pin turn on, and the interconnection between the FLT1 and the FLT2 pins turn off. After the elapse of a specified fault output holding time since the voltage of both the SCPIN1 and the SCPIN2 pins decreases to V_{OCDET} or below, the overcurrent protection is deactivated. However, if the INA pin = L when the function is deactivated, the PROOUT pin will remain ON until the INA pin changes to H. Even if the overcurrent protection is active, the miller clamp function as described by the item 5 below is kept available.

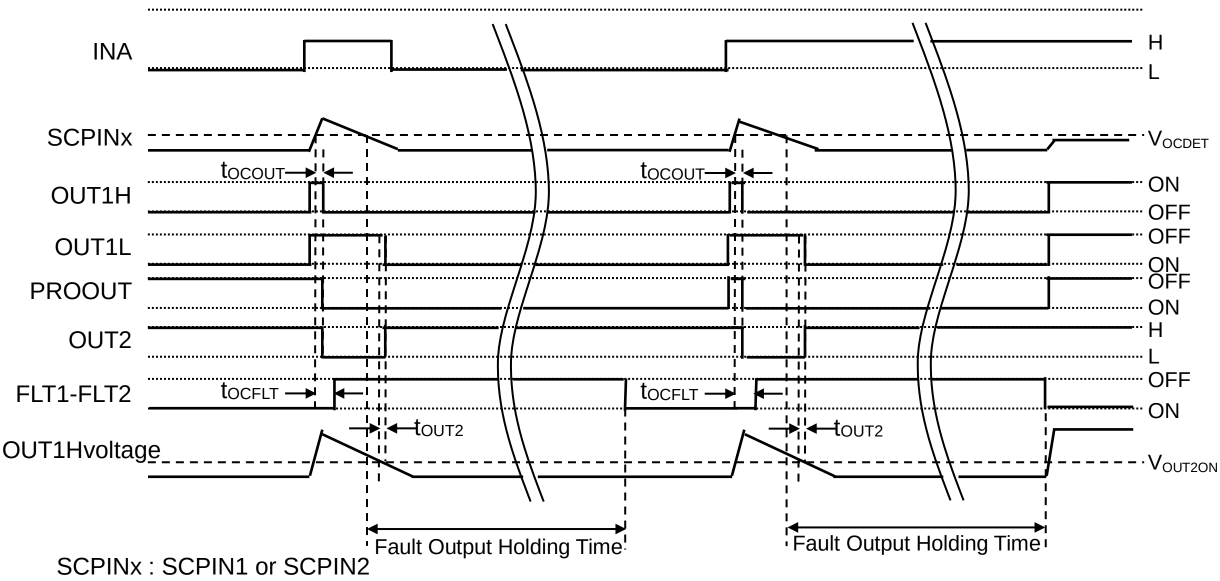


Figure 71. OCP Operation Timing Chart

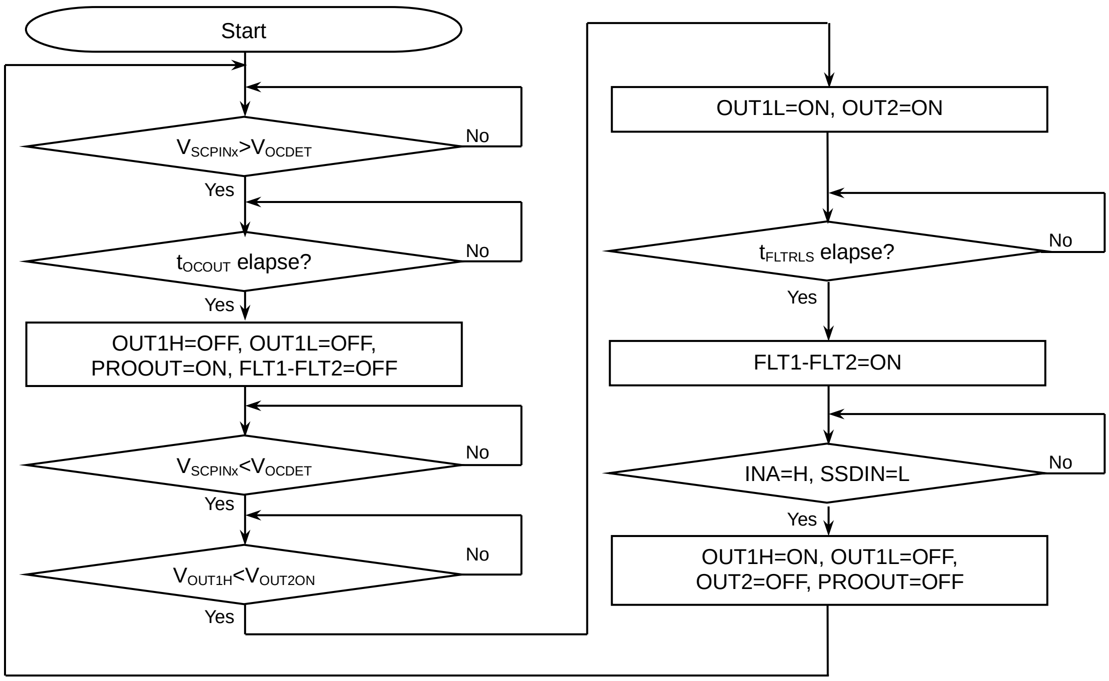


Figure 72. OCP Operation Flowchart

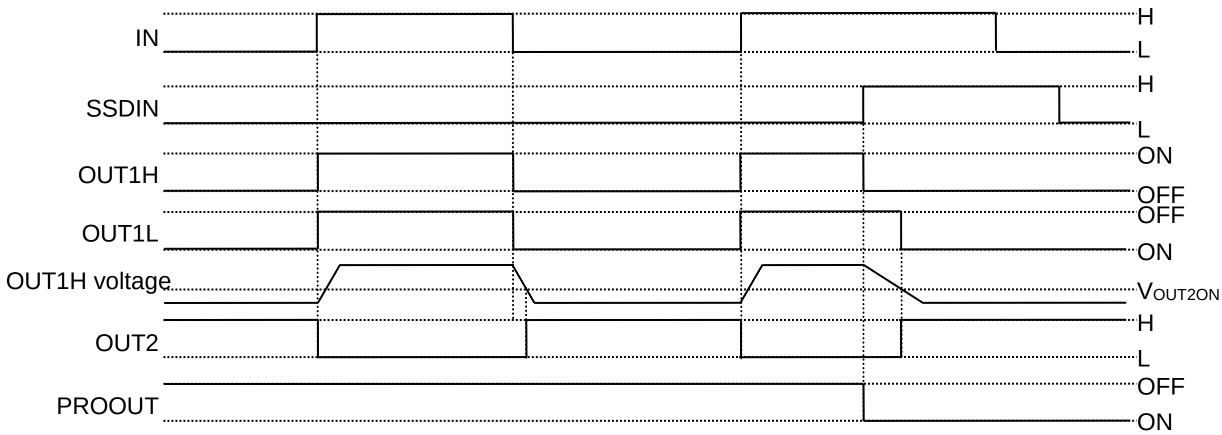
Description of Functions and Examples of Constant Setting - continued

5. Miller Clamp Function

When the OUT1H pin=OFF and the OUT1H pin voltage < V_{OUT2ON}, the OUT2 pin outputs H and miller clamp function is activated. After miller clamp function is activated, the OUT2 pin=H remains until the OUT1H pin=ON occurs. With the SSDIN pin=H, even while a fault protection (the primary side or secondary side under voltage lockout function (UVLO), short circuit protection (SCP), overcurrent protection (OCP) or overheat protection (OT) is active), the miller clamp function is kept available.

State	IN	OUT1H voltage	OUT2
Normal	H	X	L
	L	V_{OUT2ON} or larger	L
	L	Smaller than V_{OUT2ON}	H
SSDIN=H	X	V_{OUT2ON} or larger	L
	X	Smaller than V_{OUT2ON}	H
Fault	X	V_{OUT2ON} or larger	L
	X	Smaller than V_{OUT2ON}	H

X: Don't care



(Note 13) Delay time is omitted for understandable presentation

Figure 73. Miller Camp Function Operation Timing Chart

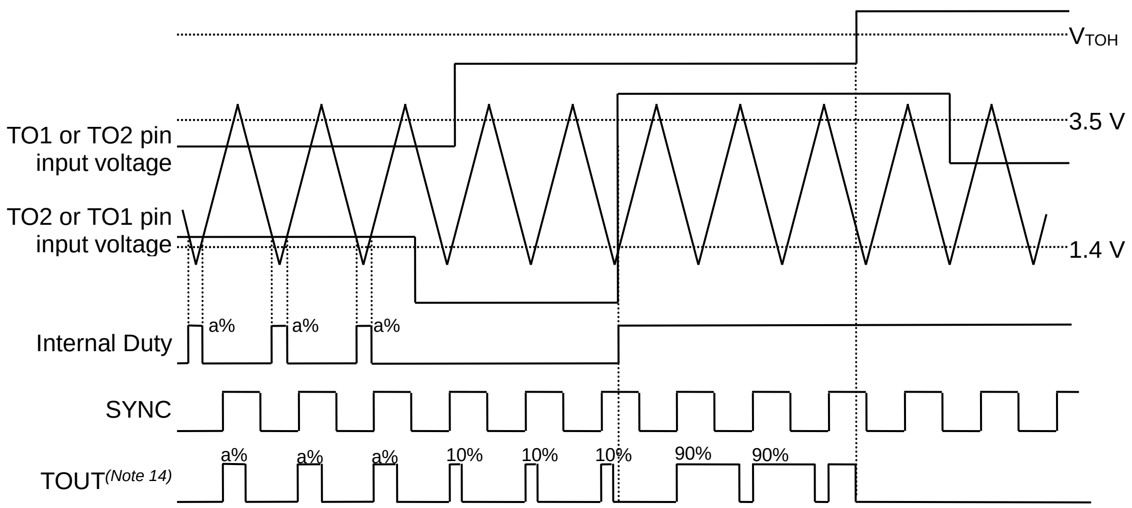
Description of Functions and Examples of Constant Setting - continued

6. Temperature Monitor Function

This IC has a built-in constant current circuit in which a constant current is supplied from TO1 and TO2 pins. This current value can be adjusted in accordance to the resistance value connected between the TC pin and the GND2 pin. Furthermore, TO1 and TO2 pins have voltage input function, and outputs the TO1 pin or the TO2 pin voltage which is smaller, as converted to Duty, from the TOUT pin. The Duty ranging between 10% and 90% is output in phase with the clock signal input to the SYNC pin. The IC has a built-in clock signal generator that uses the OSC pin to output the clock signal. Oscillation frequency can be adjusted by using the resistance between RT pin and GND1 pin. To make the clock signal generator available, connect between OSC pin and SYNC pin. However, even if the generator is not used, connect a resistor between RT pin and GND1 pin to prevent erroneous operation.

When the primary side or secondary side under voltage lockout function (UVLO) is active, or either of the TO1 pin or the TO2 pin measures a voltage over the “not connected” detection voltage V_{TOH}, the TOUT pin outputs L. Therefore, if using one the TO1 pin or the TO2 pin only, connect a resistor between the other pin and the GND2 pin to keep the voltage V_{TOH} or less.

$$\text{Constant current value} = \frac{V_{TC}}{R_{TC}}$$

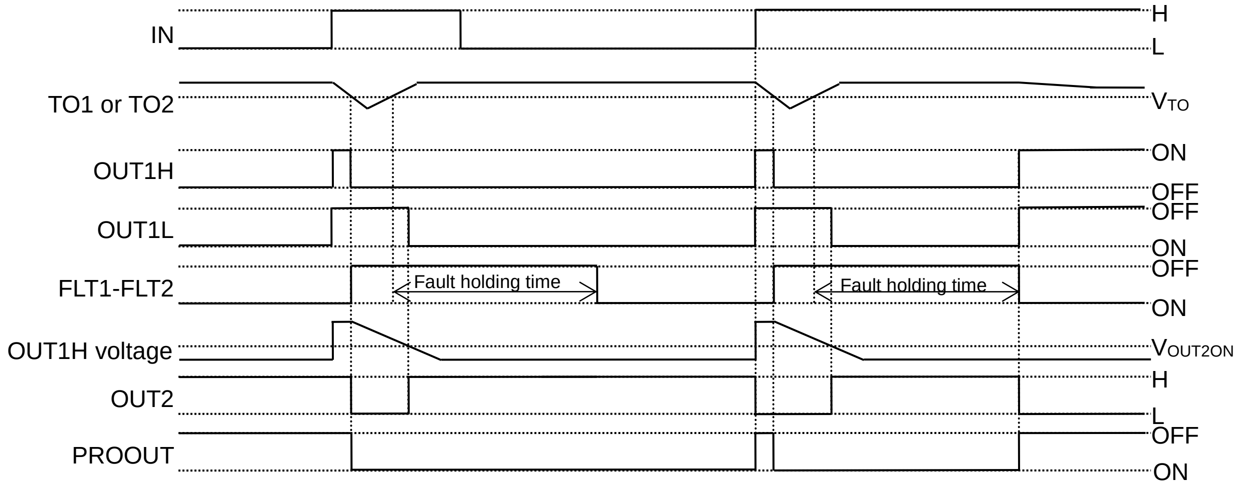


(Note 14) Delay time is omitted for a readily understandable presentation

Figure 74. Temperature Monitor Timing Chart

7. Overheat Protection (OT) Function

If the TO1 pin or the TO2 pin voltage below V_{TO} lasts for t_{TOOUT} or more, the overheat protection function is activated. Once the function is activated, both OUT1H and OUT1L pins turn off, the PROOUT pin will turns on, and the interconnection between FLT1 and FLT2 pins turn off. After the elapse of the specified fault output holding time since the voltage of both TO1 and TO2 pins increases to V_{TO} or above, the overheat protection is deactivated. However, if the INA pin = L when the function is deactivated, the PROOUT pin will remain ON until the INA pin changes to H. Even if the overheat protection is active, the miller clamp function as described by the item 5 above is kept available.



(Note 15) Delay time is omitted for the purpose of readily understandable presentation

Figure 75. Overheat protection timing chart

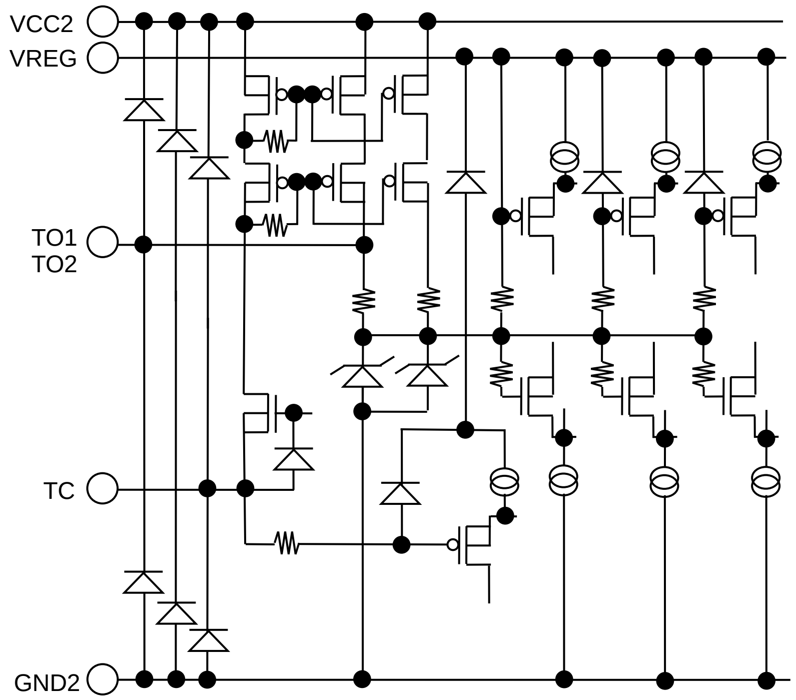
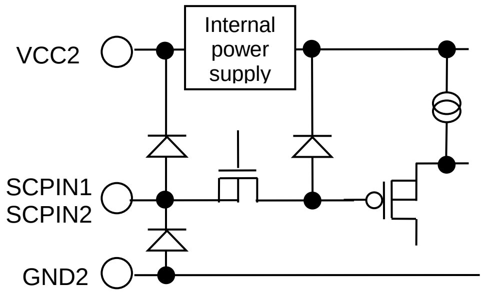
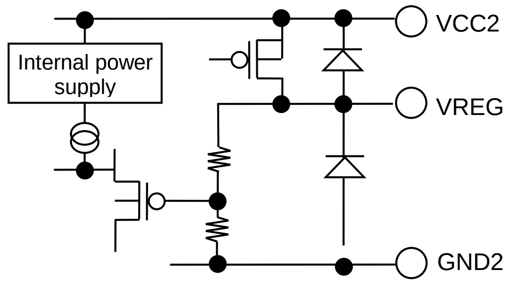
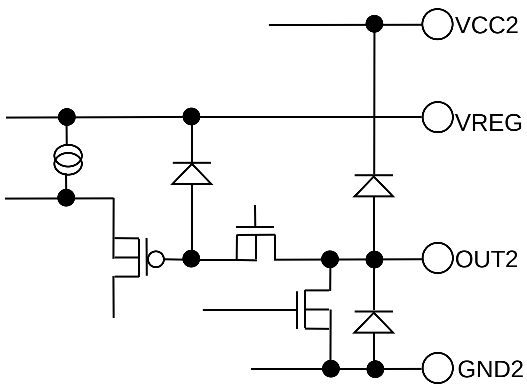
Description of Functions and Examples of Constant Setting - continued

8. Operation Truth Table

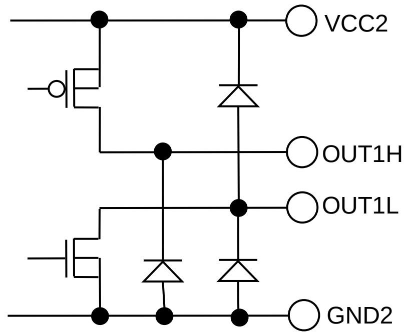
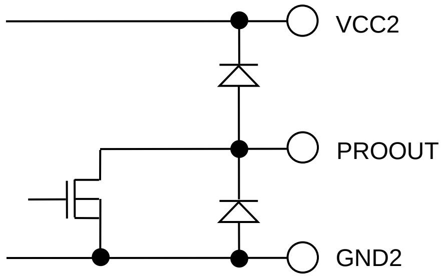
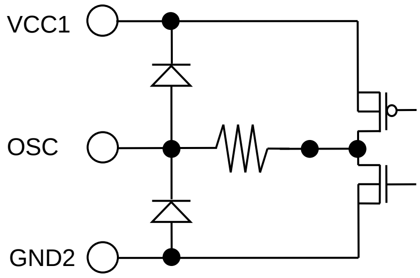
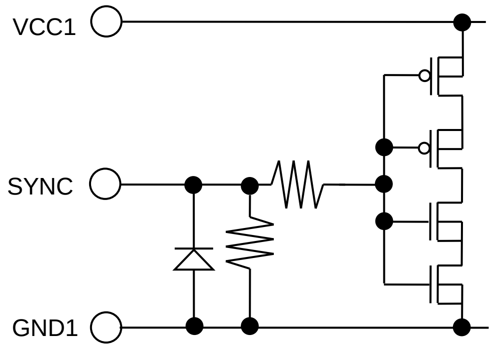
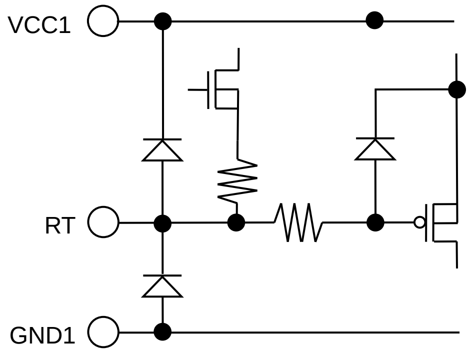
Condition	State	Input								Output				
		VCC1	VCC2	SCPIN1 or SCPIN2	TO1 or TO2	INB	INA	SSDIN	OUT1H voltage	OUT1H	OUT1L	PROOUT	OUT2	FLT1, FLT2
1	VCC1 UVLO	UVLO	X	X	X	X	X	X	H	OFF	ON	OFF	L	OFF
2		UVLO	X	X	X	X	X	X	L	OFF	ON	OFF	H	OFF
3	VCC2 UVLO	X	UVLO	X	X	X	X	X	H	OFF	ON	OFF	L	OFF
4		X	UVLO	X	X	X	X	X	L	OFF	ON	OFF	H	OFF
5	Overcurrent protection	○	○	OCP	X	L	H	L	H	OFF	OFF	ON	L	OFF
6		○	○	OCP	X	L	H	L	L	OFF	ON	ON	H	OFF
7	Short circuit protection	○	○	SCP	X	L	H	L	H	OFF	OFF	ON	L	OFF
8		○	○	SCP	X	L	H	L	L	OFF	ON	ON	H	OFF
9	Overheat protection	○	○	L	L	X	X	X	H	OFF	OFF	ON	L	OFF
10		○	○	L	L	X	X	X	L	OFF	ON	ON	H	OFF
11	External SSD	○	○	L	H	X	X	H	H	OFF	OFF	ON	L	ON
12		○	○	L	H	X	X	H	L	OFF	ON	ON	H	ON
13	Normal operation	○	○	L	H	H	X	L	H	OFF	ON	OFF	L	ON
14		○	○	L	H	H	X	L	L	OFF	ON	OFF	H	ON
15		○	○	L	H	L	L	L	H	OFF	ON	OFF	L	ON
16		○	○	L	H	L	L	L	L	OFF	ON	OFF	H	ON
17		○	○	L	H	L	H	L	X	ON	OFF	OFF	L	ON

○ : VCC1, VCC2 > UVLO, X: Don't care

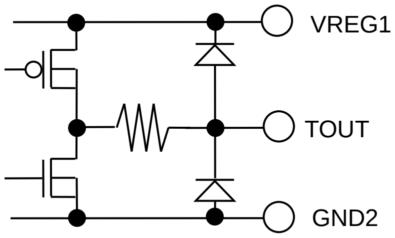
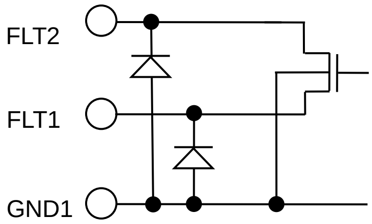
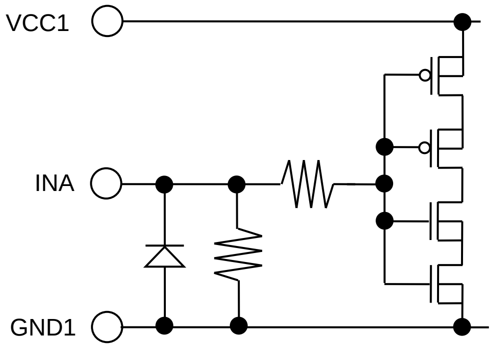
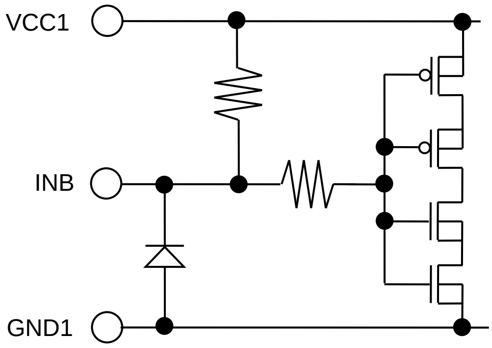
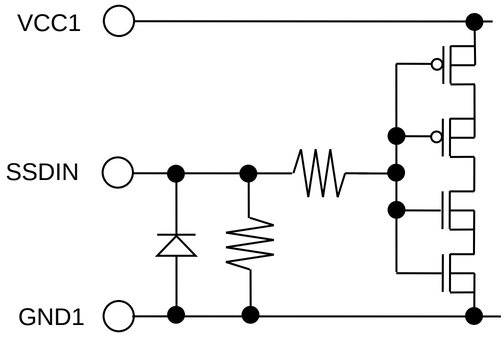
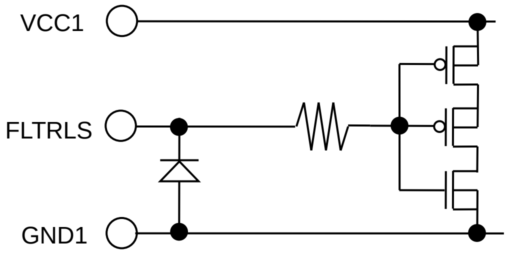
I/O Equivalence Circuits

<table>
<tr><th rowspan="2">Pin No.</th><th>Pin Name</th><th rowspan="2">Input Output Equivalent Circuit Diagram</th></tr>
<tr><th>Pin Function</th></tr>
<tr><td rowspan="2">2</td><td>TO1</td><td rowspan="6">
</td></tr>
<tr><td>Constant current output
/ Sensor voltage input pin 1</td></tr>
<tr><td rowspan="2">3</td><td>TO2</td></tr>
<tr><td>Constant current output
/ Sensor voltage input pin 2</td></tr>
<tr><td rowspan="2">4</td><td>TC</td></tr>
<tr><td>Constant current setting resistor connection pin</td></tr>
<tr><td rowspan="2">5</td><td>SCPIN1</td><td rowspan="4">
</td></tr>
<tr><td>Short circuit and overcurrent detection pin 1</td></tr>
<tr><td rowspan="2">6</td><td>SCPIN2</td></tr>
<tr><td>Short circuit and overcurrent detection pin 2</td></tr>
<tr><td rowspan="2">7</td><td>VREG</td><td rowspan="2">
</td></tr>
<tr><td>Secondary side internal power supply pin</td></tr>
<tr><td rowspan="2">8</td><td>OUT2</td><td rowspan="2">
</td></tr>
<tr><td>Miller Clamp Control pin</td></tr>
</table>

I/O Equivalence Circuits - continued

<table>
<tr><th rowspan="2">Pin No.</th><th>Pin Name</th><th rowspan="2">Input Output Equivalent Circuit Diagram</th></tr>
<tr><th>Pin Function</th></tr>
<tr><td rowspan="2">10</td><td>OUT1H</td><td rowspan="4">
</td></tr>
<tr><td>Source side output
/ Gate voltage input pin</td></tr>
<tr><td rowspan="2">12</td><td>OUT1L</td></tr>
<tr><td>Sink side output pin</td></tr>
<tr><td rowspan="2">13</td><td>PROOUT</td><td rowspan="2">
</td></tr>
<tr><td>Soft shutdown output pin</td></tr>
<tr><td rowspan="2">16</td><td>OSC</td><td rowspan="2">
</td></tr>
<tr><td>Output pin for oscillation frequency</td></tr>
<tr><td rowspan="2">17</td><td>SYNC</td><td rowspan="2">
</td></tr>
<tr><td>External clock input pin</td></tr>
<tr><td rowspan="2">18</td><td>RT</td><td rowspan="2">
</td></tr>
<tr><td>Oscillation frequency setup resistor connection pin</td></tr>
</table>

I/O Equivalence Circuits - continued

Pin No.	Pin Name / Pin Function	Input Output Equivalent Circuit Diagram
19	TOUT Temperature information output pin	
20	FLT2 Fault signal output pin	
22	FLT1 Fault signal output pin	
23	INA Control input pin	
24	INB Control input pin	
26	SSDIN Soft shutdown control input pin	
27	FLTRLS Fault output holding time setup pin	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

    When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
    When GND > Pin B, the P-N junction operates as a parasitic transistor.

    Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

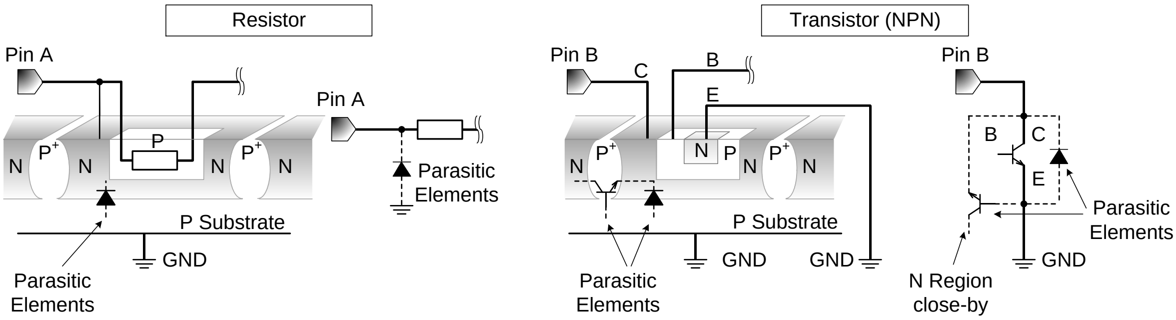
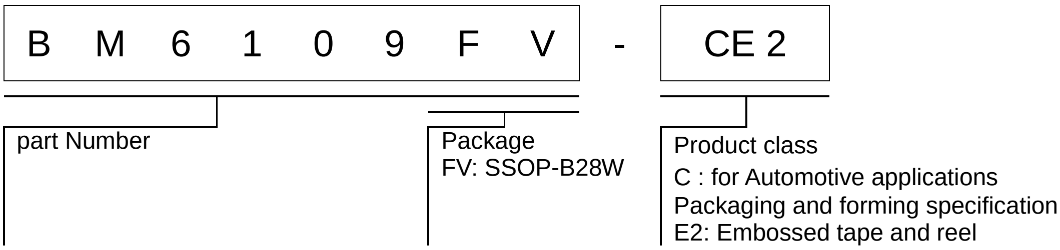


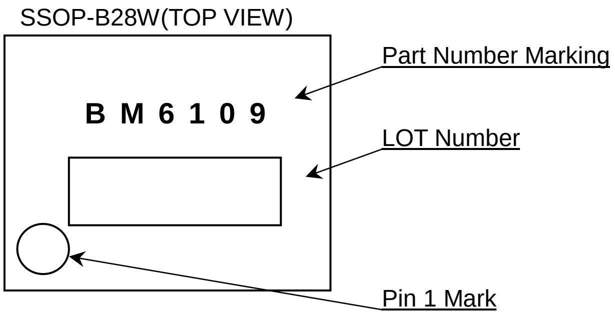
Figure 76. Example of IC Structure

11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

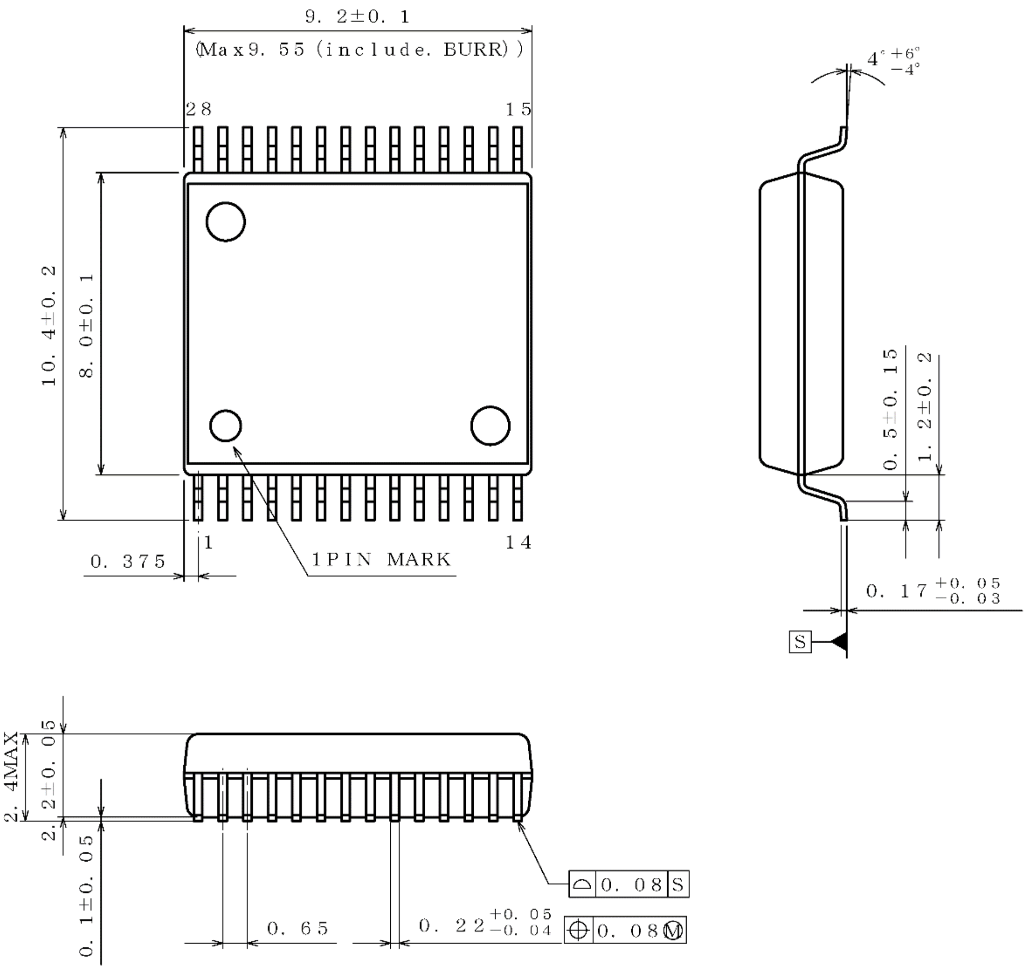


Marking Diagram



Physical Dimension and Packing Information

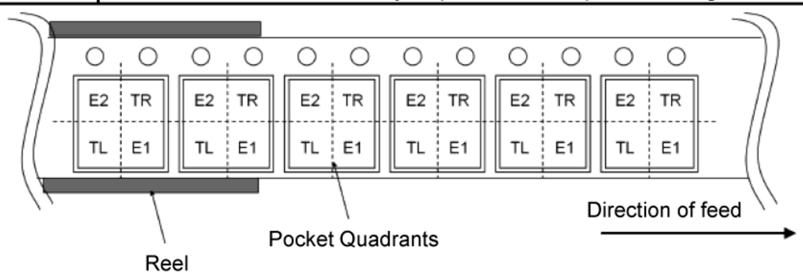
Package Name	SSOP-B28W



(UNIT : mm)
PKG : SSOP−B28W
Drawing No. EX072−5002

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
25.Oct.2018	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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