Datasheet

LED Drivers for LCD Backlights

PFC Direct Current Resonance Type White LED Driver for Large LCD

BD94122F

General Description

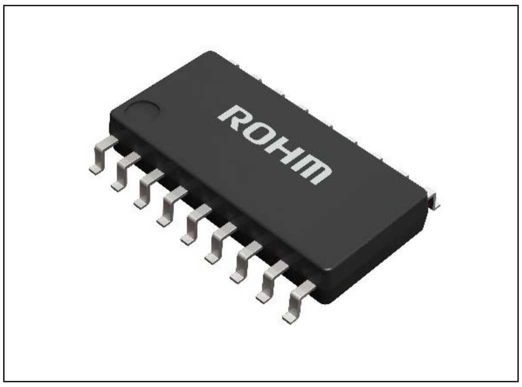
BD94122F is a current resonance type LED Driver, which can connect to PFC directly. LED current is controlled by driving output frequency. Because this IC can use half bridge structure, it can reduce the number of external components.
BD94122F has some protection functions against fault conditions such as Over Voltage Protection(OVP), LED Short Protection(LSP) and LED Open Protection Detection(LOP).

Key Specifications

- Power Supply Voltage Range: V_{CC}: 9.0V to 18.0V
- Output Driving Frequency (Minimum Frequency Setting): 60kHz(R_{RT}=68kΩ)
- Circuit Current: 5.0mA(Typ)
- Operating Temperature Range: -40°C to +85°C

Package

Package	W(Typ) x D(Typ) x H(Max)
SOP18	11.20mm x 7.80mm x 2.01mm



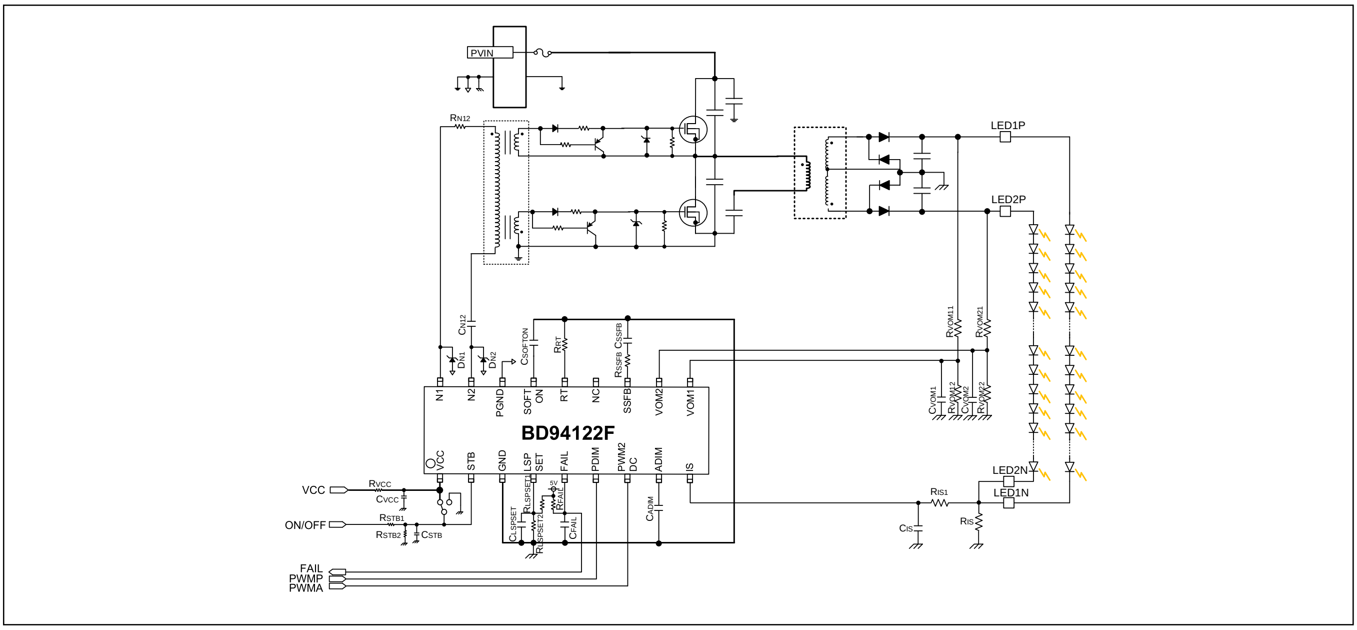
Features

- 1 Channel Push Pull Control
- Current Feedback by Driving Frequency Resolution
- Timer Latch Circuit
- Under Voltage Detection for IC's Power Line (VCC UVLO)
- Output Over Voltage Protection
- Driving Output Frequency (Minimum Frequency Setting) Tolerance: ±5%
- Error Signal Output from FAIL Pin
- Control IC Power On and Off by STB Pin
- Burst Control by External PWM
- Analog Dimming by External DC
- Pulse/DC Conversion Function for ADIM

Applications

- TV, Computer Display, LCD Backlighting

Typical Application Circuit

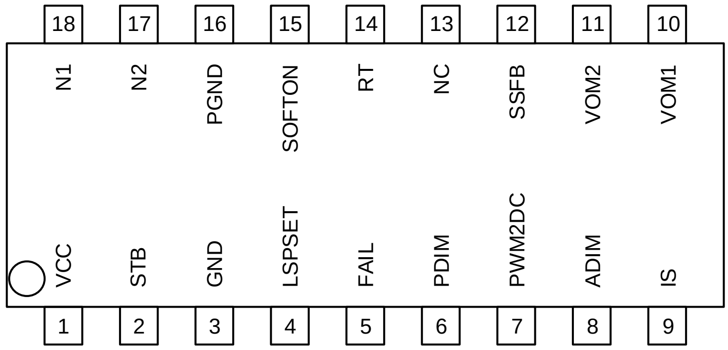


〇Product structure: Silicon monolithic integrated circuit 〇This product has no designed protection against radioactive rays

Contents

Pin Configuration

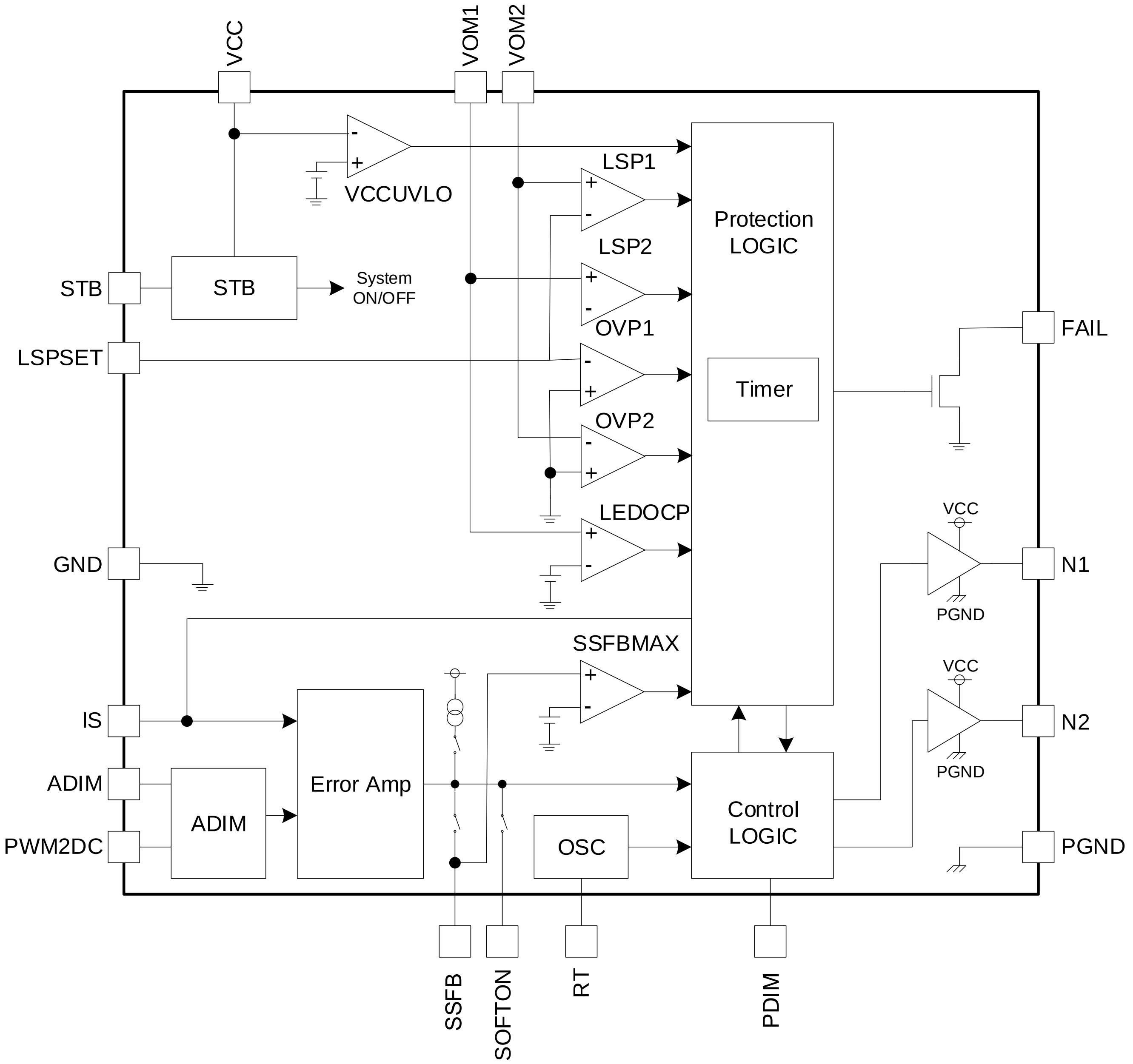
(TOP VIEW)



Pin Description

Pin No.	Pin Name	IN/OUT	Function
1	VCC	IN	Power supply for IC (built in UVLO function).
2	STB	IN	Power ON/OFF control for IC (STB=L: Power OFF, STB=H: Power ON).
3	GND	IN	Ground for internal signal in IC.
4	LSPSET	IN	LED short protection voltage setting.
5	FAIL	OUT	Error signal output (Normal: L, Error: Open).
6	PDIM	IN	PWM signal input for burst dimming.
7	PWM2DC	IN	Pulse/DC converting. Pulse signal is translated to flat by 100kΩ resistor in IC and the capacitor connected to ADIM.
8	ADIM	IN/OUT	DC signal output of Pulse/DC converting and DC signal input for analog dimming.
9	IS	IN	Error amplifier input for LED current feedback. IS Low detection and IS High detection input.
10	VOM1	IN	Channel 1 over voltage protection and LED short protection.
11	VOM2	IN	Channel 2 over voltage protection and LED short protection.
12	SSFB	OUT	Set phase compensation of feedback loop. When V_{SSFB} is 3.5V or more, LED OPEN protection and LED SHORT protection are enable. When V_{SSSB} is 4.0V or more, SSFB MAX protection is enable.
13	NC	-	No Connection(Open).
14	RT	OUT	Minimum driving frequency and dead time setting. Basic frequency and dead time are set by the resistor between RT and GND, and driving frequency modulation range is set by RT resistor.
15	SOFTON	OUT	Soft on. When PDIM is set from high to low (or from low to high), a driving frequency changes from normal to maximum (or maximum to normal), the frequency changing speed can be adjusted by SOFTON capacitor setting.
16	PGND	IN	Power ground for N1 and N2 drivers.
17	N2	OUT	Gate drive output for low side external FET.
18	N1	OUT	Gate drive output for high side external FET.

Block Diagram



Pin Function Descriptions

If there is no description, the mentioned values are typical value.

PIN 1: VCC

This is power supply pin for the IC. Normal operation range is from 9V to 18V. Place ceramic capacitor 0.1µF or more as bypass capacitor between VCC and GND. It is for noise elimination.

PIN 2: STB

This pin is for setting of ON/OFF. It is possible to use as reset when shutting down. Depending on input voltage to the STB pin, the status of IC might be switched(ON/OFF). Avoid using between the two statuses (0.8V to 2.0V).

PIN 3: GND

This is signal system GND for IC inside. Make it independent from PGND as much as possible. (We recommend this because it has less influence with switching noise which comes from short circuit of PGND and GND at connector close to the GND pin.)

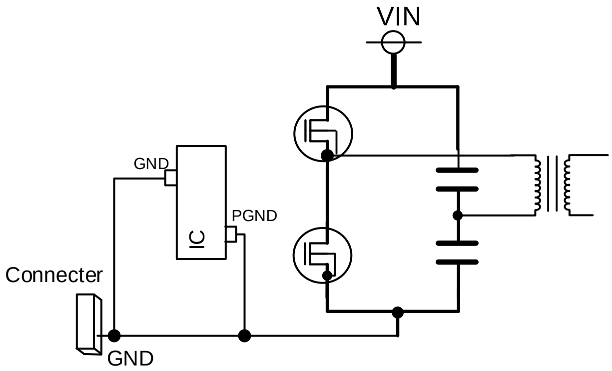


Figure 1. Connection Method between GND and PGND

PIN 4: LSPSET

LED short protection voltage setting pin. 32CLK timer will be started if VOM1 or VOM2 pin's voltage is under LSPSET pin's voltage after IS reaches to setting voltage or SSFB reaches to 3.5V at the first time while PDIM=H. If VOM1 voltage exceeds LSPSET voltage within 32CLK or PDIM become Low, the timer will be re-set. After time out, system will stop N1, N2, discharge SSFB, pull-up FAIL and latch off.

PIN 5: FAIL

This is error signal output pin of IC. At normal situation, it outputs GND level and it becomes open after timer latch in case any abnormality is detected. The pull-up voltage during open must be set less than rated voltage 18V of the FAIL pin. Connect about 0.1µF capacitor for noise reduction to the FAIL pin.

Condition	FAIL Output
Normal Operation	GND Level
Abnormal Operation	Open

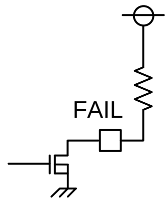


Figure 2. FAIL Block Diagram

PIN 6: PDIM

By inputting PWM pulse signal at the PDIM pin, it is possible to adjust burst dimming. (High level: 1.8V or more, Low level: 0.8V or less).

Condition	LED Condition
PDIM: 1.8V to 5.0V	Turn On
PDIM: -0.3V to +0.8V	Turn Off

Avoid using between the two statuses (0.8V < V_{PDIM} < 1.8V).

Pin Function Descriptions - continued

If there is no description, the mentioned values are typical value.

PIN 7: PWM2DC, PIN 8: ADIM

Pulse signal inputs to PWM2DC pin and IC can average it by IC internal 100kΩ and the capacitor connected to ADIM pin (This means pulse to DC signal transfer circuit.). At this time, ADIM ripple is changed by ADIM's capacitance, therefore please set suitable capacitance according to set specification. While the PWM2DC pin is forced 8.5V or more, a buffer output in the IC becomes high impedance and the ADIM pin is enable to input DC voltage directly. According to PWM2DC input level, each pin's function is changed as the followings. Pulse/DC translation circuit is shown in Pulse/DC Transfer Block Diagram.

PWM2DC Input Level	PWM2DC Function	ADIM Function	Needed Signal from External
$-0.3V \le V_{PWM2DC} \le +6.5V$	Pulse Signal Input for Analog Dimming	DC Signal Output for Analog Dimming	DUTY Signal for Analog Dimming
$8.5V \le V_{PWM2DC} \le 18.0V$	Mask Pulse/DC Translation Function	DC Signal Input for Analog Dimming	DC Signal for Analog Dimming

Avoid using between the two statuses ($6.5V < V_{PWM2DC} < 8.5V$).

The voltage that ADIM voltage multiplies by (1/2.75) becomes IS threshold voltage and it has linear characteristic. But, ADIM voltage becomes 0.55V or less, IS threshold voltage is clamped at 0.55V/2.75=0.2V. And ADIM becomes 2.2V or more, IS threshold voltage is clamped at 2.2V/2.75=0.8V. When IS threshold voltage is used for linear characteristic, set $0.6V \le V_{ADIM} \le 2.1V$.

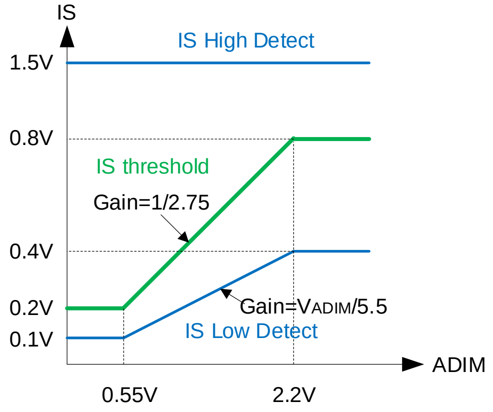


Figure 3. IS Threshold Voltage vs ADIM Voltage

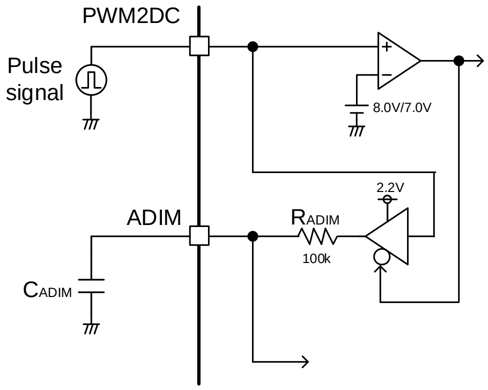


Figure 4. Pulse/DC Transfer Block Diagram

PIN 9: IS

This is input pin of LED current feedback error amplifier. Set the IS pin to (ADIM/2.75V) in the normal operation. And the IS pin has IS Low detect and IS High detect. IS Low detect works as LED open protection. IS Low detection voltage is changed following with ADIM voltage (Refer to the Figure 3. IS Threshold Voltage vs ADIM Voltage). IS High detect works as LED OCP. About each detection voltage and condition, refer to the Detection Condition List of the Protection Functions.

PIN 10: VOM1

The VOM1 pin is an input pin for channel 1 over voltage protection and LED short protection. If over voltage is detected, N1 and N2 outputs are stopped and a timer will start counting at the same time. If VOM1 voltage is lower than over voltage release threshold, N1 and N2 will restart to output. If over voltage is detected and released 3 times within 4096CLK, system will stop N1 and N2, discharge SSFB, pull-up FAIL and latch off. If over-voltage is detected and released less than 3 times within 4096CLK, system will not discharge SSFB, will not pull-up FAIL, and will not latch off. Timer counter will be reset at 4096CLK counting. When the LED short protection(LSP) function is activated, the LLC converter will stop operation and latch off after 32CLK. The VOM1 pin is the high impedance type and involves no pull-down resistor, resulting in unstable potential in the open circuited state. To avoid this problem, be sure to make input voltage setting with the use of a resistive divider.

PIN 11: VOM2

The VOM2 pin is an input pin for channel 2 over voltage protection and LED short protection. The function is same to the VOM1 pin.

PIN 12: SSFB

The SSFB pin is a phase compensation pin of the feedback loop. When the SSFB pin voltage is 3.5V or more, LED Open Protection(LOP) can be detected. When the SSFB pin voltage is 3.5V or more or IS voltage reach to ADIM/2.75 at the first time after system start up, LED Short Protection(LSP) can be detected. After the first time, even if the SSFB pin voltage is lower than 3.5V or IS voltage do not reach to ADIM/2.75, LSP still can be detected. When the SSFB pin voltage is higher than 3.5V, or IS voltage reach to setting voltage(ADIM/2.75), start up stage is completed. When start up state is under operation (the SSFB pin voltage is less than 3.5V or IS voltage do not reach to setting voltage at first time), LSP timer counter latch protection circuit will not operate. But OVP timer counter latch protection circuit can still operate.

PIN 12: SSFB - continued
If there is no description, the mentioned values are typical value.

When the SSFB pin voltage is 4.0V or more, SSFB MAX Protection (SSFB MAX) can be detected. When SSFB MAX is detected, a timer will start counting at the same time. When SSFB voltage is 3.5V or less, SSFB MAX is released. When SSFB MAX is detected 3 times within 4096CLK, system will stop N1 and N2, discharge the SSFB pin, pull-up the FAIL pin and latch off. When SSFB MAX is detected less than 3 times within 4096CLK, system will not discharge the SSFB pin, will not pull up the FAIL pin, and will not latch off. Timer will be reset at 4096CLK counting.

PIN 13: NC
NC is no connection pin. Set this pin as open.

PIN 14: RT
Set up the minimum driving frequency. By changing the resistance value between the RT pin and GND, it is possible to set up minimum driving frequency as following formula;

$$f_{MIN} = \frac{4080}{R_{RT}} \quad \text{[kHz]} \qquad (f_{MIN} \leq 168kHz)$$

$$f_{MIN} = \frac{4374}{R_{RT}+1.75} \quad \text{[kHz]} \qquad (f_{MIN} > 168kHz)$$

Once minimum driving frequency is decided, maximum driving frequency is also decided. As following formula;

$$f_{MAX} = 4.491 \times f_{MIN} \quad \text{[kHz]} \qquad (f_{MIN} \leq 168kHz)$$

$$f_{MAX} = \frac{6 \times f_{MIN}}{1+0.002+f_{MIN}} \quad \text{[kHz]} \qquad (f_{MIN} > 168kHz)$$

There is a discrepancy between theoretical formula and actual device. For frequency setting, please thoroughly verify it with actual application. If minimum driving frequency is decided, Dead Time is also decided as the following formula;

$$t_{OFF} = 8.2353 \times R_{RT} = \frac{33600}{f_{MIN}} \quad \text{[ns]} \qquad (f_{MIN} \leq 168kHz)$$

$$t_{OFF} = 200 \quad \text{[ns]} \qquad (f_{MIN} > 168kHz)$$

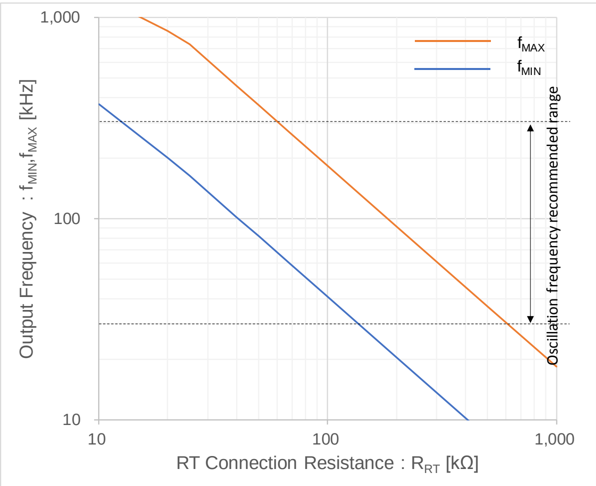


Figure 5. Output Frequency vs RT Connection Resistance

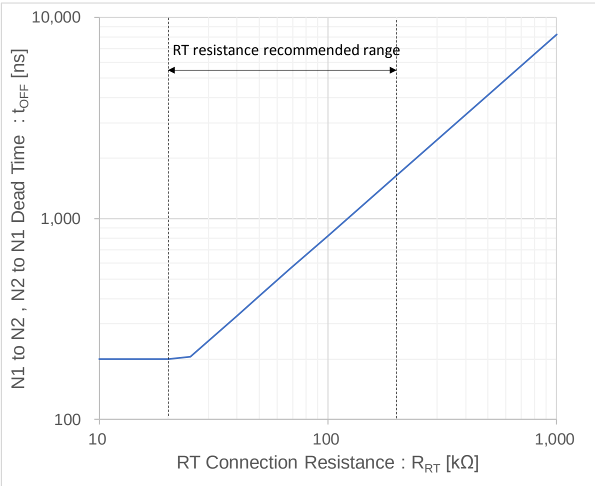


Figure 6. N1 to N2, N2 to N1 Dead Time vs RT Connection Resistance

PIN 15: SOFTON
This is soft ON/OFF time set up pin when PWM logic is changed. A capacitor (0.01µF to 0.1µF) is connected to SOFTON pin to decide soft ON/OFF time.

PIN 15: SOFTON - continued
If there is no description, the mentioned values are typical value.

$$t_{SOFTON} = 0.633 \times C_{SOFTON} \times \frac{V_{SSFB}}{I_{SOFTON}} = 0.633 \times \frac{C_{SOFTON} \times V_{SSFB}}{1.0 \times 10^{-4}} \quad [s]$$

V_{SSFB} is SSFB pin's voltage. It is decided by system feedback loop.

PIN 16: PGND
This is Power GND pin for output pin N1 and N2 at driver part. Make it independent from the GND pin (Pin 3) on PCB. This pin is not connected to GND pin in IC inside.

PIN 17: N2
This is gate drive output pin for Low Side external FET. Normally connect it to the FET gate through about 10Ω resistor. Internal has 100Ω pull down resistor for noise reduction when STB=L.

PIN 18: N1
This is gate drive output pin for High Side external FET. Normally connect it to the FET gate through about 10Ω resistor. Internal has 100Ω pull down resistor for noise reduction when STB=L.

Detection Condition List of the Protection Functions

If there is no description, the mentioned values are typical value.

Protect Function	Detection pin	Detect Condition		Release Condition	Timer Operation	Protection Type
		Detection Pin Condition	SSFB			
LED OPEN (IS Low Detect)	IS	$V_{IS} \le 0.1V$ and $V_{ADIM} < 0.55V$	$V_{SSFB} \ge 3.5V$	$V_{IS} > 0.1V$ and $V_{ADIM} < 0.55V$	16CLK	Latch Off
		$V_{IS} \le V_{ADIM}/5.5$ and $0.55V \le V_{ADIM} \le 2.2V$		$V_{IS} > V_{ADIM}/5.5$ and $0.55V \le V_{ADIM} \le 2.2V$		
		$V_{IS} \le 0.4V$ and $V_{ADIM} > 2.2V$		$V_{IS} > 0.4V$ and $V_{ADIM} > 2.2V$		
LED SHORT	VOM1 VOM2	$V_{VOMx} \le V_{LSPSET}$	(PDIM=H and $V_{SSFB} \ge 3.5V$) or (PDIM=H And LEDOK=H)	$V_{VOMx} > V_{LSPSET}$	32CLK	Latch Off
LED OCP (IS High Detect)	IS	$V_{IS} \ge 1.5V$	-	$V_{IS} \le 1.3V$	16CLK	Latch Off
OVP	VOM1 VOM2	$V_{VOMx} \ge 3.0V$	-	$V_{VOMx} \le 2.9V$	3 times within 4096CLK	Latch Off
VCC UVLO	VCC	$V_{CC} \le 7.5V$	-	$V_{CC} \ge 8.0V$	-	Restart by Release
SSFB MAX	SSFB	-	$V_{SSFB} \ge 4.0V$	$V_{SSFB} \le 3.5V$	3 times within 4096CLK	Latch Off

In order to reset the latch off condition, to set the STB pin to low or detection of VCCUVLO is required. The count number in the list is calculated with output driving frequency.

Operation List of the Protection Function

Protect Function	Operation of the Protect Function		
	N1, N2 Output	SSFB Pin	FAIL Output
LED OPEN	Stop after latch	Low after latch	High after latch
LED SHORT	Stop after latch	Low after latch	High after latch
LED OCP	Stop after latch	Low after latch	High after latch
OVP	Stop immediately	Low after latch	High after latch
VCC UVLO	Stop immediately	Low immediately	High immediately
SSFB MAX	Stop after latch	Low after latch	High after latch

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	-0.3 to +18	V
STB, PWM2DC, N2, N1, LSPSET, FAIL, PDIM, ADIM, VOM1, VOM2 Pin Voltage	V_{STB}, V_{PWM2DC}, V_{N2}, V_{N1}, V_{LSPSET}, V_{FAIL}, V_{PDIM}, V_{ADIM}, V_{VOM1}, V_{VOM2}	-0.3 to +18	V
RT, SSFB, IS, SOFTON Pin Voltage	V_{RT}, V_{SSFB}, V_{IS}, V_{SOFTON}	-0.3 to +5.5	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SOP18				
Junction to Ambient	θ_{JA}	179.3	119.9	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	20	17	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	Topr	-40	-	+85	°C
Power Supply Voltage	V_{CC}	9.0	-	18.0	V
PDIM Input Frequency Range	f_{PWMIN}	60	-	500	Hz
Oscillation Frequency Range	f_{OUT}	30	-	300	kHz
PWM2DC Input Frequency Range	f_{PWM2DC}	0.09	-	30.00	kHz
ADIM Input Voltage Range	V_{ADIM}	0	-	5	V
ADIM Range with Linearity IS	$V_{ADIMLIN}$	0.6	-	2.1	V

External Components Recommended Ranges

Parameter	Symbol	Min	Typ	Max	Unit
RT Connection Resistance	R_{RT}	20	-	200	kΩ
SOFTON Connection Capacitance	C_{SOFTON}	0.01 *(Note 5)*	-	0.10	μF
ADIM Connection Capacitance	C_{ADIM}	0.22 *(Note 5)*	-	10.00	μF
SSFB Connection Capacitance	C_{SSFB}	0.01 *(Note 5)*	-	1.00	μF

(Note 5) Please set connection capacitance above minimum value of External Components Recommended Ranges according to temperature characteristic and DC bias characteristic.

Electrical Characteristics(Unless otherwise specified V_{CC}=12V Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Whole Device						
Circuit Current	I_{CC1}	-	5.0	10.0	mA	f_{OUT}=60kHz, V_{PDIM}=3V
Circuit Current at Stand by	I_{CC2}	-	1.5	20.0	μA	V_{STB}=0V
STB Control						
STB High Voltage	V_{STH}	2.0	-	V_{CC}	V	System ON
STB Low Voltage	V_{STL}	-0.3	-	+0.8	V	System OFF
VCC UVLO						
VCC Operation Start Voltage	V_{VCCUVP}	7.5	8.0	8.5	V	VCC Sweep Up
VCC UVLO Hysteresis	ΔV_{VCCUVP}	0.37	0.50	0.63	V	
OSC						
RT Pin Voltage	V_{RT}	2.5	3.1	3.7	V	
PDIM						
PDIM High Voltage	V_{PWMINH}	1.8	-	5.0	V	
PDIM Low Voltage	V_{PWMINL}	-0.3	-	+0.8	V	
Start						
Start Ended Voltage	V_{STEND}	3.20	3.50	3.80	V	
Feedback						
IS Threshold Voltage 1	V_{IS1}	0.746	0.764	0.782	V	V_{ADIM}=2.1V, V_{PWM2DC}=12V
IS Threshold Voltage 2	V_{IS2}	0.382	0.400	0.418	V	V_{ADIM}=1.1V, V_{PWM2DC}=12V
IS Threshold Voltage 3	V_{IS3}	0.203	0.227	0.251	V	V_{ADIM}=0.625V, V_{PWM2DC}=12V
SSFB Source Current	I_{SSFBSO}	-120	-100	-80	μA	V_{SSFB}=2.0V, V_{ADIM}=5.0V, V_{IS}=0.0V
SSFB Sink Current	I_{SSFBSI}	80	100	120	μA	V_{SSFB}=2.0V, V_{ADIM}=0.0V, V_{IS}=1.2V
SOFTON Charge Current	I_{SFTONC}	-120	-100	-80	μA	V_{SSFB}=3.0V, V_{SOFTON}=2.0V
SOFTON Discharge Current	I_{SFTOND}	80	100	120	μA	V_{SSFB}=1.0V, V_{SOFTON}=2.0V
IS Low Detection Voltage	V_{ISLOW}	0.040	0.100	0.160	V	IS Sweep Down V_{ADIM}=0.5V
IS High Detection Voltage	V_{ISHIGH}	1.35	1.50	1.65	V	IS Sweep Up
OVP						
OVP Detection Voltage	V_{OVP}	2.85	3.00	3.15	V	VOM1,VOM2 Sweep Up
OVP Detection Hysteresis	V_{OVP_HYS}	50	100	200	mV	VOM1,VOM2 Sweep Down
SSFB MAX						
SSFB MAX Detection Voltage	$V_{SSFBMAX}$	3.8	4.00	4.2	V	SSFB Sweep Up
SSFB MAX Detection Hysteresis	$V_{SSFBMAXHYS}$	250	500	1000	mV	SSFB Sweep Down

Electrical Characteristics(Unless otherwise specified V_{CC}=12V Ta=25°C) - continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
OUTPUT						
N1 Output Sink Resistance	R_{N1SI}	1.5	3.0	6.0	Ω	
N1 Output Source Resistance	R_{N1SO}	4.5	9.0	18.0	Ω	
N1 Pull-Down Resistance	R_{N1PD}	50	100	200	Ω	STB=L
N2 Output Sink Resistance	R_{N2SI}	1.5	3.0	6.0	Ω	
N2 Output Source Resistance	R_{N2SO}	4.5	9.0	18.0	Ω	
N2 Pull-Down Resistance	R_{N2PD}	50	100	200	Ω	STB=L
N1 to N2, N2 to N1 Dead Time	t_{OFF}	280	560	1120	ns	V_{SSFB}=4.0V, R_{RT}=68kΩ
N1to N2, N2 to N1 Minimum Dead Time	t_{OFFMIN}	100	200	400	ns	
Driving Output Frequency (Minimum Frequency Setting)	f_{OUTMIN}	57.0	60.0	63.0	kHz	V_{SSFB}=4.0V, R_{RT}=68kΩ
Timer						
OVP Timer Number	N_{OVP}	-	4096	-	CLK	
ADIM						
ADIM Inflow Current 1	I_{ADIM1}	-5	0	+5	µA	V_{ADIM}=2.2V, V_{PWM2DC}=12V
ADIM Inflow Current 2	I_{ADIM2}	19	28	37	µA	V_{ADIM}=5V, V_{PWM2DC}=12V
PWM2DC Inflow Current	I_{PWM2DC}	4	6	8	µA	V_{PWM2DC}=3V
PWM2DC High Voltage	$V_{PWM2DCH}$	1.8	-	5.0	V	
PWM2DC Low Voltage	$V_{PWM2DCL}$	-0.3	-	+0.8	V	
PWM2DC Selected Voltage to High Impedance	$V_{PWM2DCZ}$	7.5	8.0	8.5	V	PWM2DC Sweep Up
FAIL						
FAIL ON Resistance	R_{FAIL}	-	100	200	Ω	

Typical Performance Curves

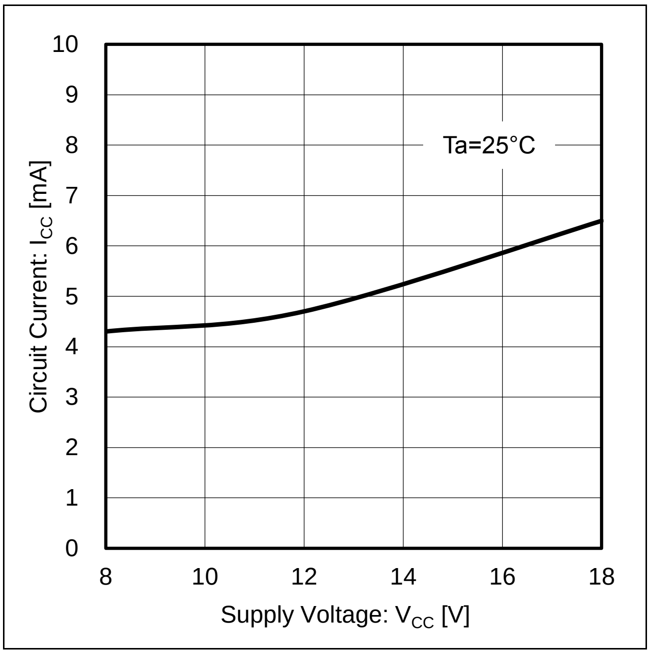


Figure 7. Circuit Current vs Supply Voltage

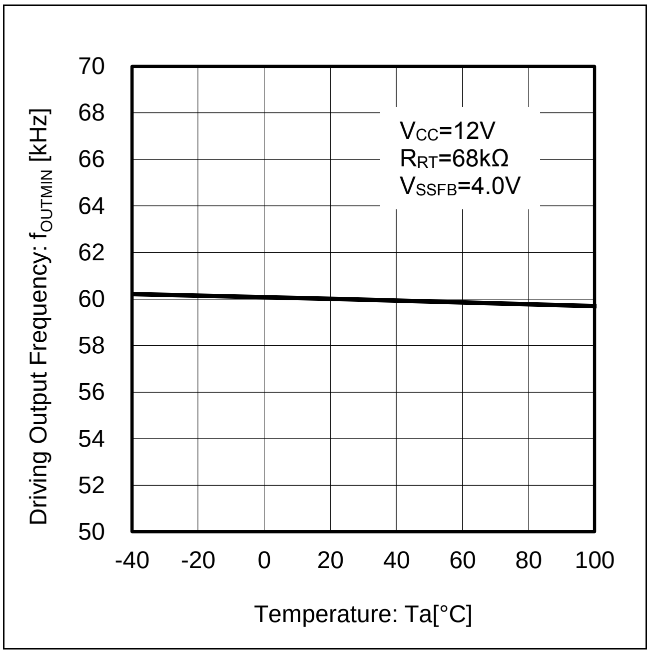


Figure 8. Driving Output Frequency vs Temperature

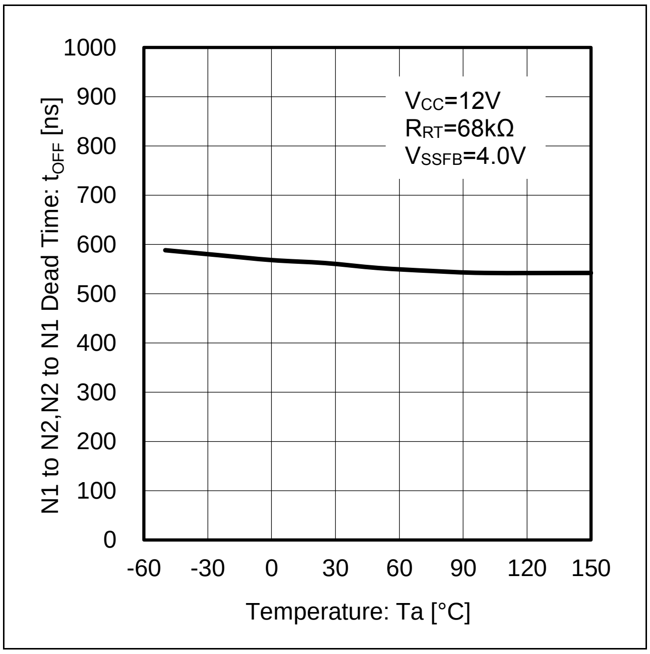


Figure 9. N1 to N2,N2 to N1 Dead Time vs Temperature

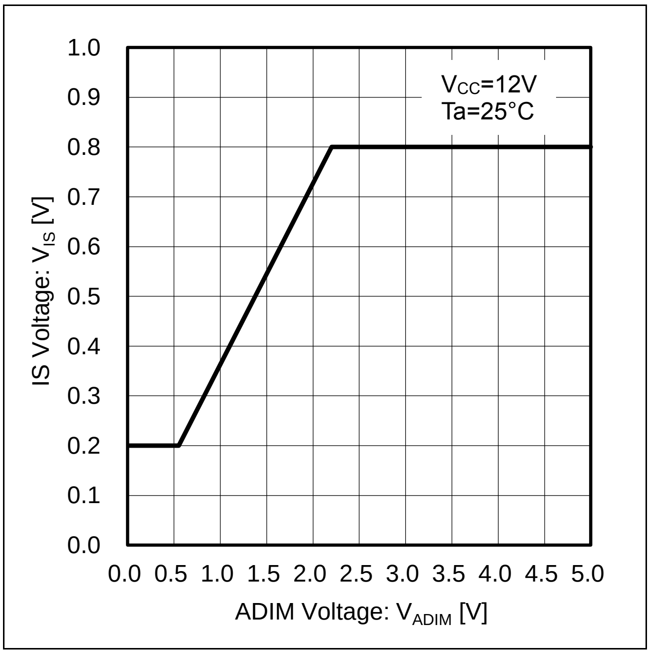


Figure 10. IS voltage vs ADIM Voltage

Timing Chart

If there is no description, the mentioned values are typical value.

OVP and LED SHORT Protection(LSP)

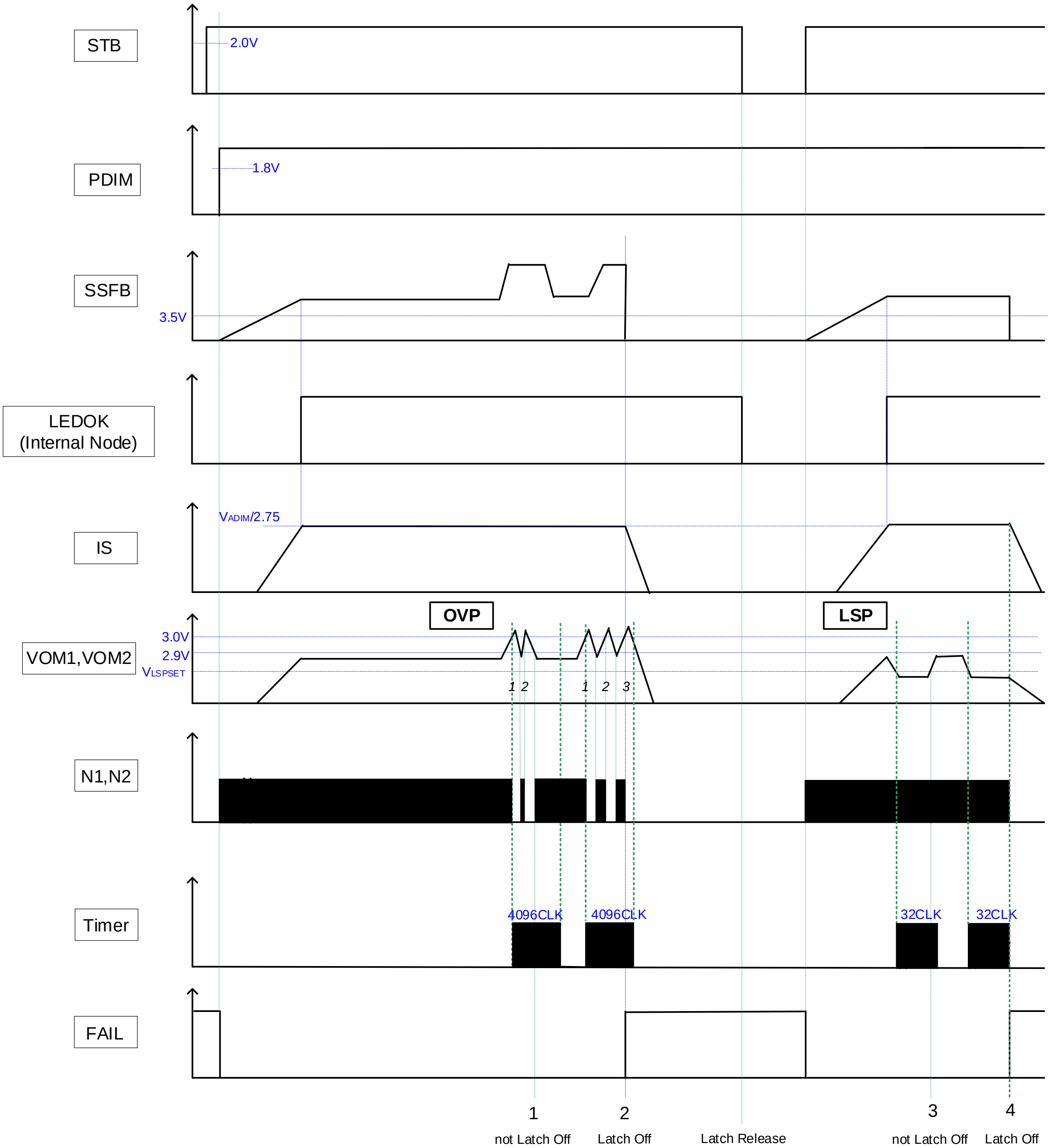


Figure 11. Timing Chart 1

LEDOK signal is internal signal that latches to high while IS voltage becomes ADIM/2.75.

No.	Error Detect Content	Error Detect Condition
1	OVP detection (not Latch Off)	Detect V_{VOMx} ≥ 3.0V less than 3times in 4096CLK
2	OVP detection (Latch Off)	Detect V_{VOMx} ≥ 3.0V 3times in 4096CLK
3	LSP detection (not Latch Off)	Return to V_{VOMx} ≥ V_{LSPSET} in less than 32CLK
4	LSP detection (Latch Off)	Detect V_{VOMx} ≤ V_{LSPSET} in 32CLK

Timing Chart - continued

If there is no description, the mentioned values are typical value.

LED OPEN Protection(LOP) and LED OCP

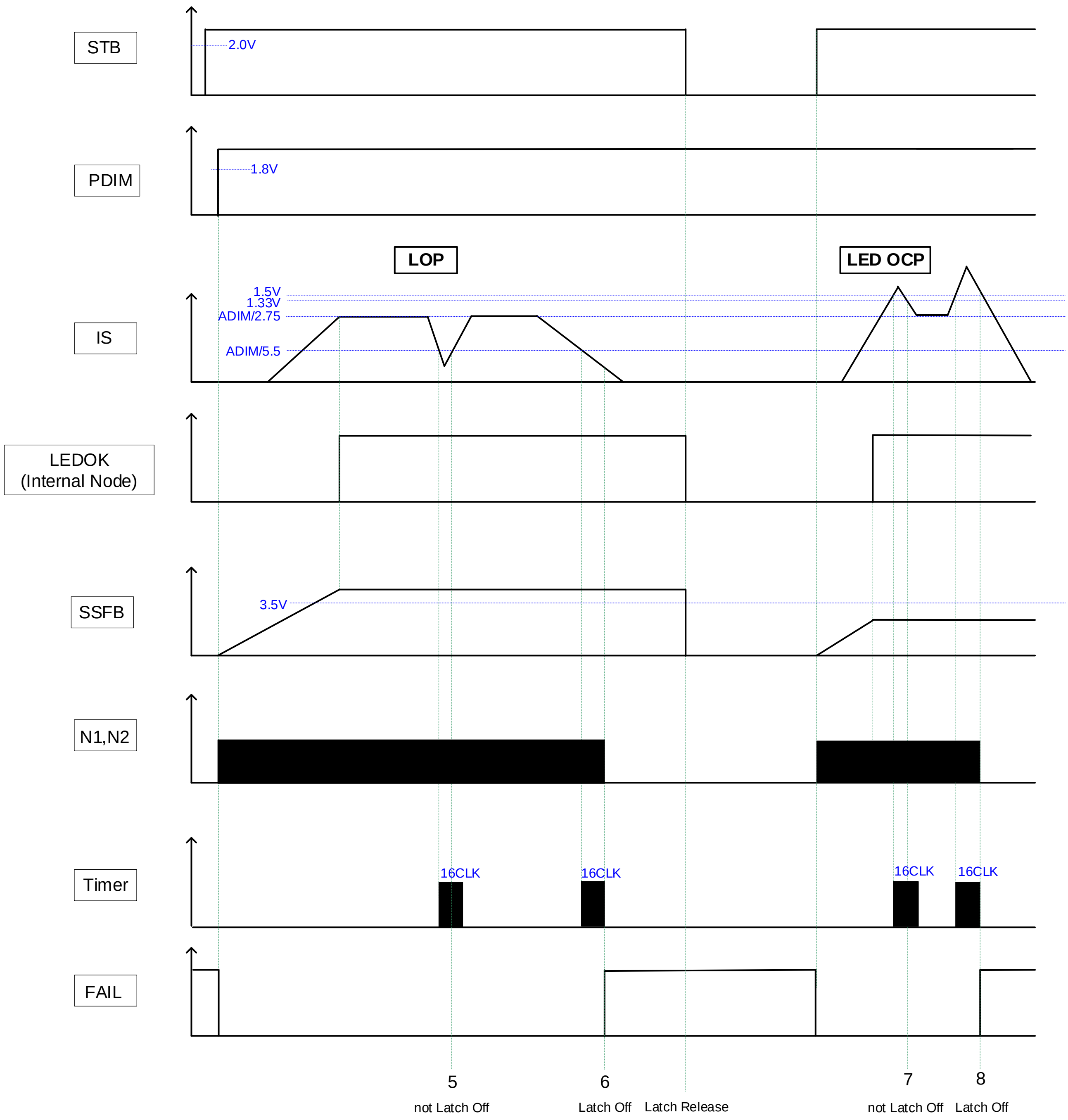


Figure 12. Timing Chart 2

Detection voltage of LED open protection in this timing chart is the condition of $0.55V \leq V_{ADIM} \leq 2.2V$. Detection voltage of LED open protection is changed by ADIM voltage setting (Refer to the Detection Condition List of the Protection Functions.).
LEDOK signal is internal signal that latches to high while IS voltage becomes ADIM/2.75.

No.	Error Detect Content	Error Detect Condition
5	LOP detection (not Latch Off)	Return to $V_{IS} > V_{ADIM}/5.5$ in less than 16CLK
6	LOP detection (Latch Off)	Detect $V_{IS} \leq V_{ADIM}/5.5$ and $V_{SSFB} \geq 3.5V$ in 16CLK
7	LED OCP detection (not Latch Off)	Return to $V_{IS} \leq 1.3V$ in less than 16CLK
8	LED OCP detection (latch Off)	Detect $V_{IS} \geq 1.5V$ in 16CLK

Timing Chart - continued

If there is no description, the mentioned values are typical value.

SSFB MAX Protection

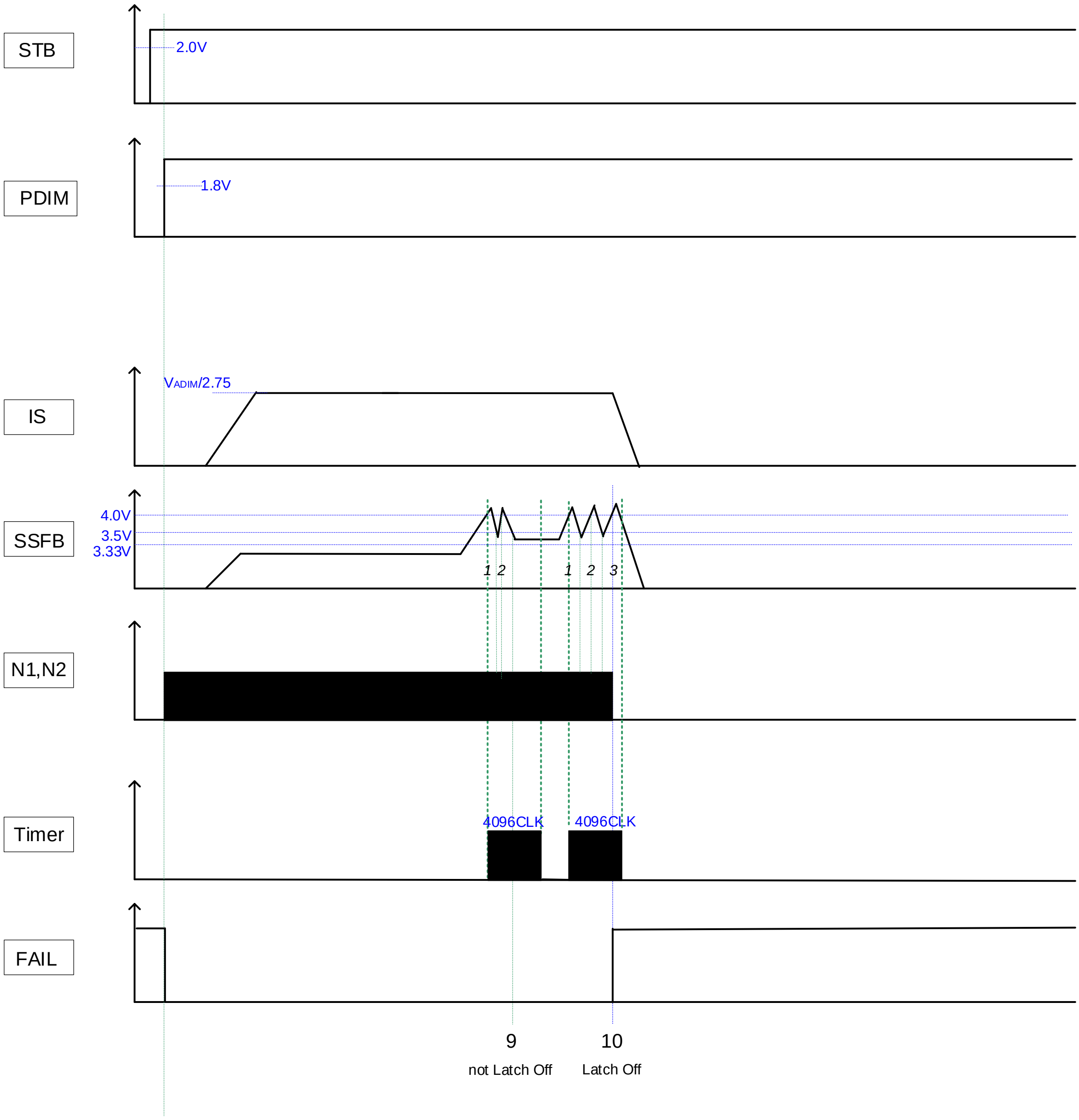


Figure 13. Timing Chart 3

No.	Error Detect Content	Error Detect Condition
9	SSFB MAX detection (not Latch Off)	Detect V_{SSFB} ≥ 4.0V less than 3times in 4096CLK
10	SSFB MAX detection (Latch Off)	Detect V_{SSFB} ≥ 4.0V 3times in 4096CLK

Timing Chart - continued

If there is no description, the mentioned values are typical value.

Output Timing Chart

BD94122F outputs the signal that operates the Push Pull or Half Bridge which is made up of Nch FET.
The output timing of drive signal is shown in the following chart.

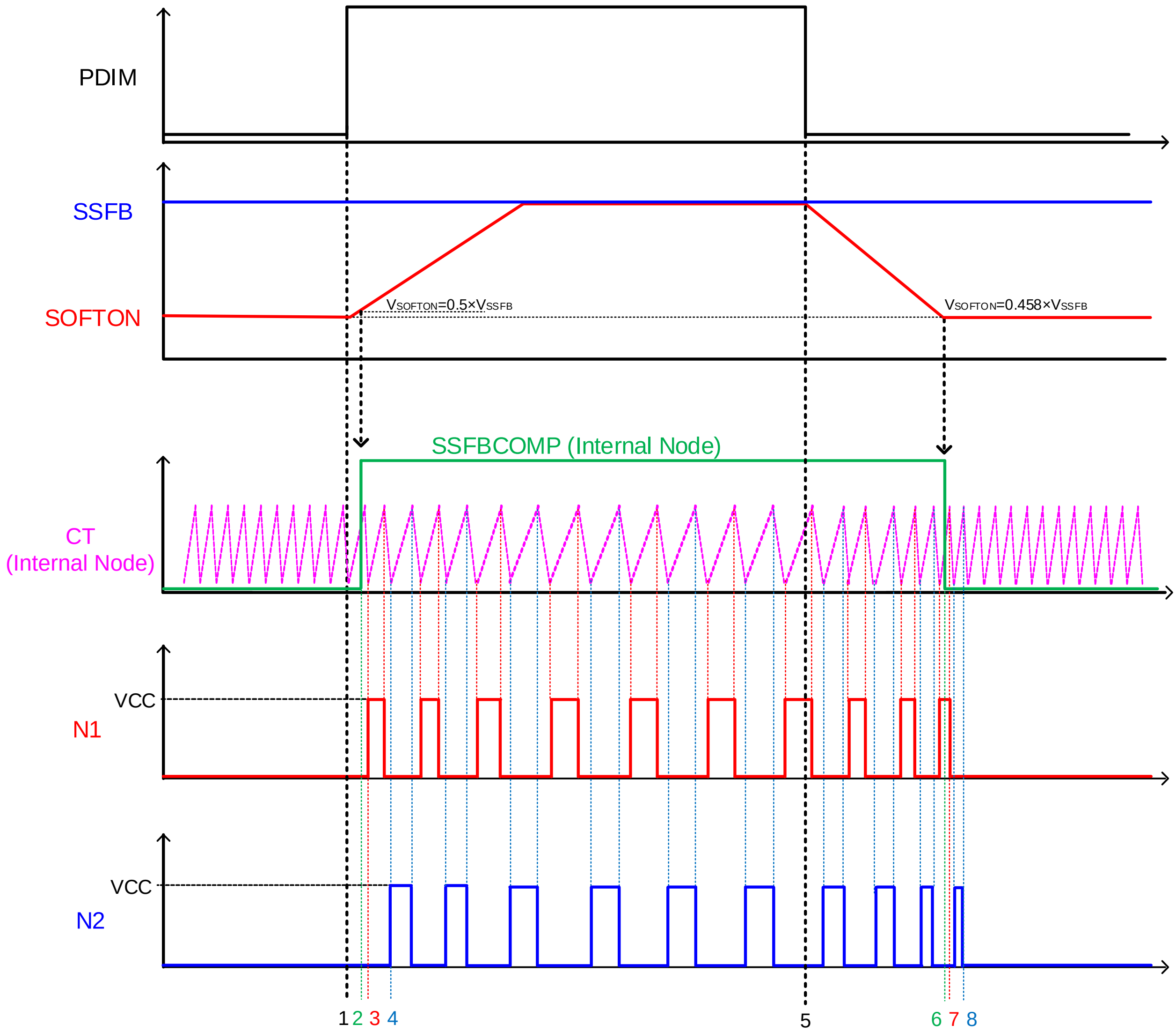


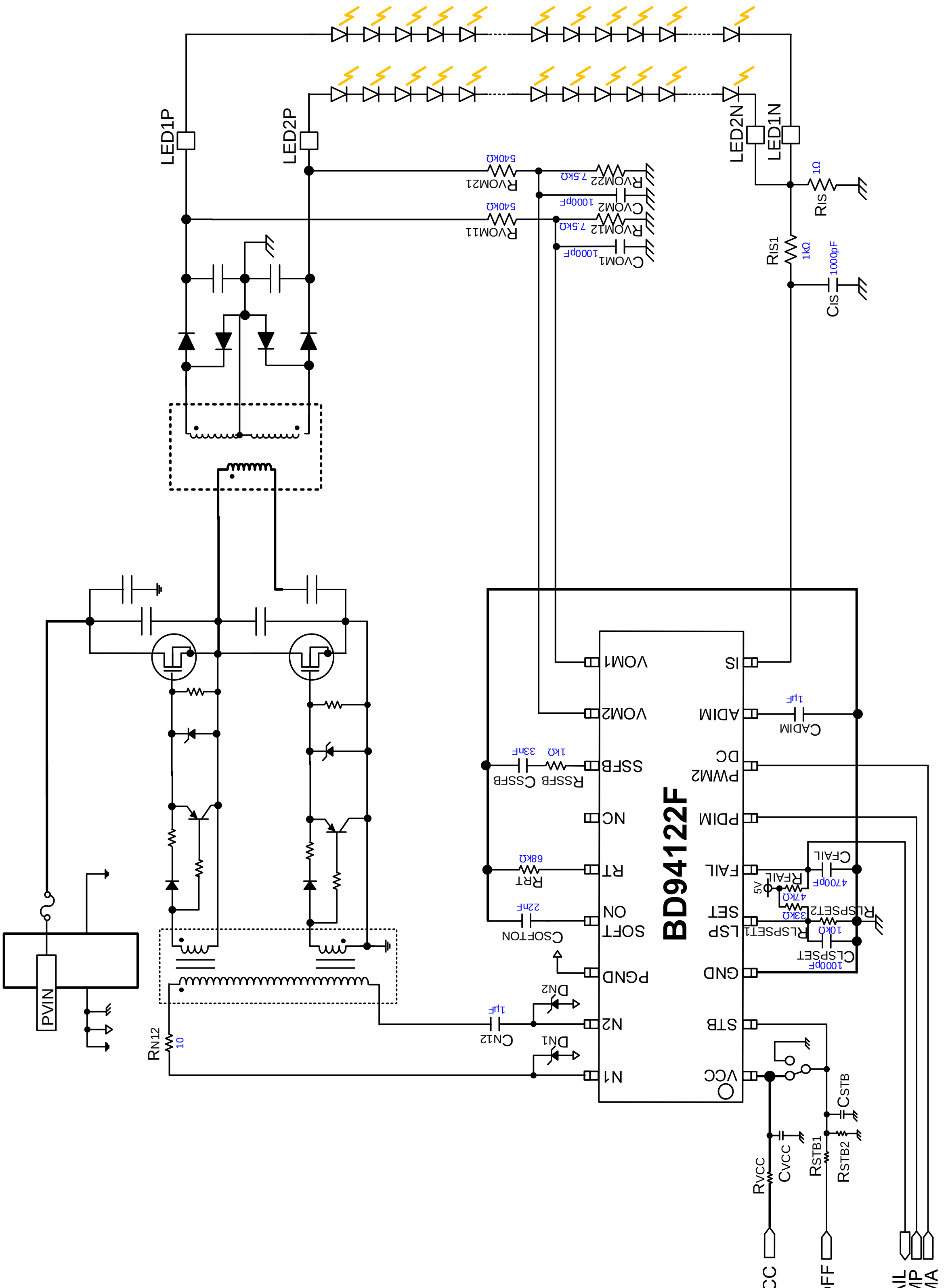
Figure 14. Timing Chart 4

CT is internal signal of an oscillator based on N1 and N2 driving frequency.
SSFBCOMP is internal signal that is enable to output N1 and N2 when V_{SOFTON} becomes 0.5 x V_{SSFB}.

1. When PDIM is changed from Low to High, SOFTON voltage is increased.
2. When V_{SOFTON} is 0.5 x V_{SSFB}, SSFBCOMP is changed from Low to High and N1 and N2 outputs are enable.
3. N1 outputs pulse first.
4. And then N2 outputs pulse. When SOFTON voltage shifts from 0.5 x V_{SSFB} to SSFB voltage, N1 and N2 driving frequency shifts from maximum to normal.
5. When PDIM is changed from High to Low, SOFTON voltage is decreased. When SOFTON voltage shifts from SSFB voltage to 0.458 x V_{SSFB}, N1 and N2 driving frequency shifts from normal to maximum.
6. When V_{SOFTON} is 0.458 x V_{SSFB}, SSFBCOMP is changed from High to Low.
7. After N1 outputs a pulse decided by the level of the SOFTON pin, N1 stops output.
8. After N2 outputs a pulse decided by the level of the SOFTON pin, N2 stops output.

Application Example

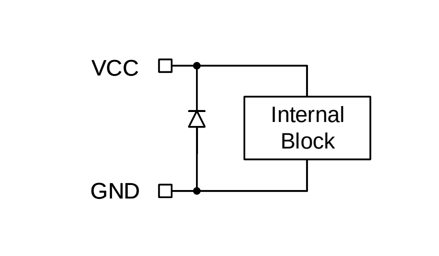
Introduce an application example with BD94122F.



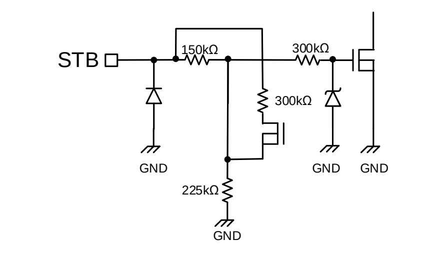
(Note 5) LED dimming setting is decided by ADIM voltage setting and PWM Duty setting, but actual lowest dimming value is depended on application's responsibility, so check set's behavior and then decide each setting.

I/O Equivalence Circuits

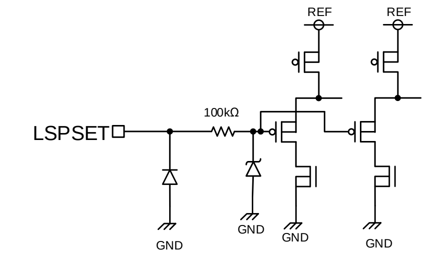
Pin1: VCC / Pin3: GND



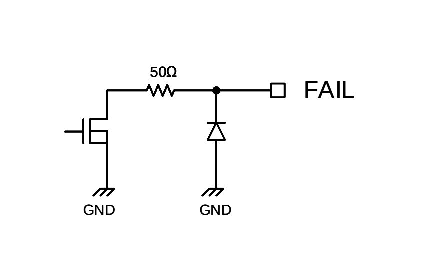
Pin2: STB



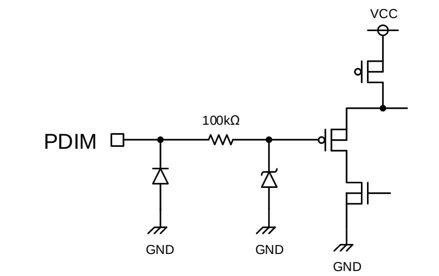
Pin4: LSPSET



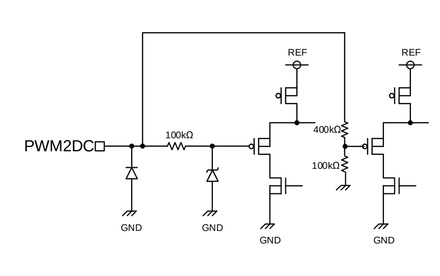
Pin5: FAIL



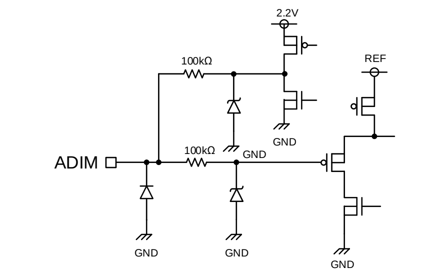
Pin6: PDIM



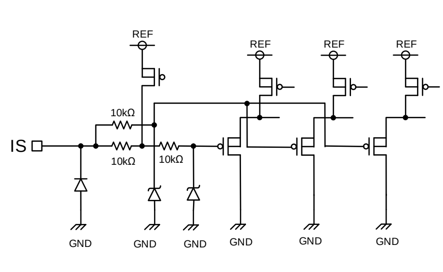
Pin7: PWM2DC



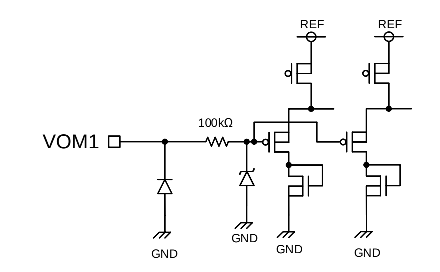
Pin8: ADIM



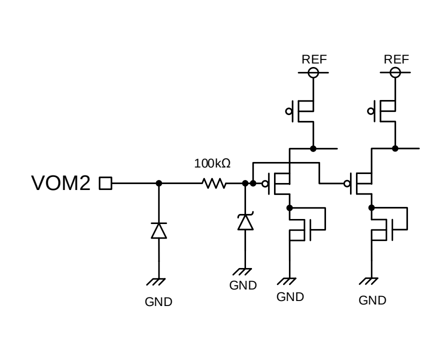
Pin9: IS



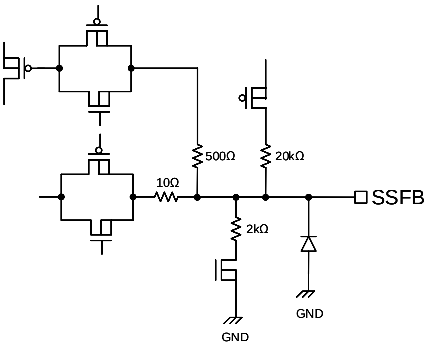
Pin10: VOM1



Pin11: VOM2



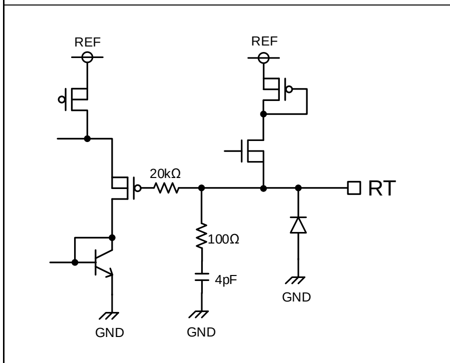
Pin12: SSFB



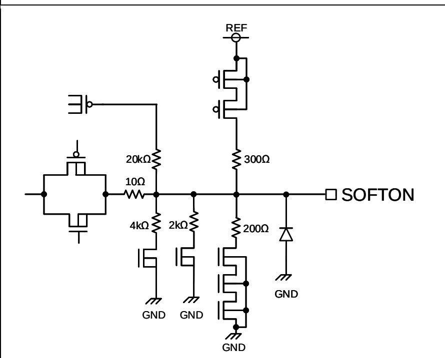
Pin13: NC

—

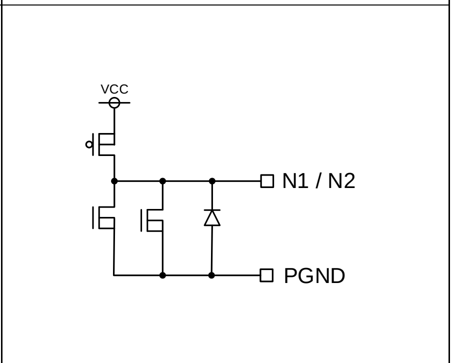
Pin14: RT



Pin15: SOFTON



Pin16: PGND / Pin17: N2 / Pin18: N1



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

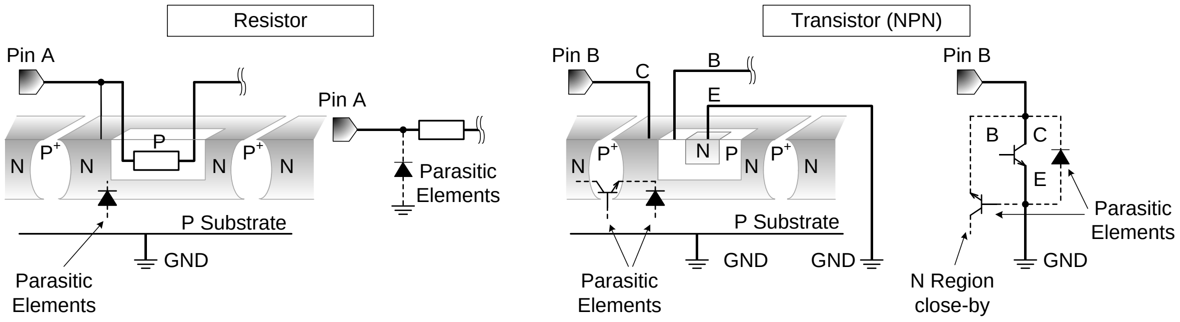


Figure 15. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

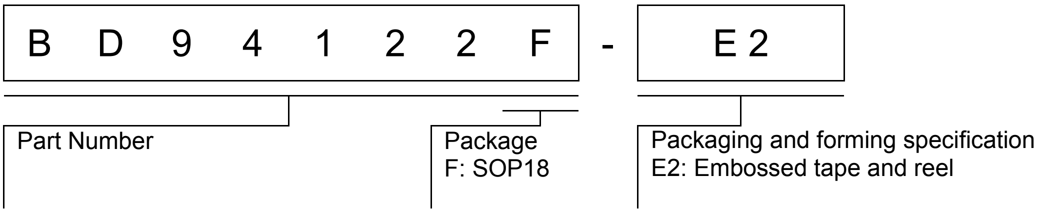
14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

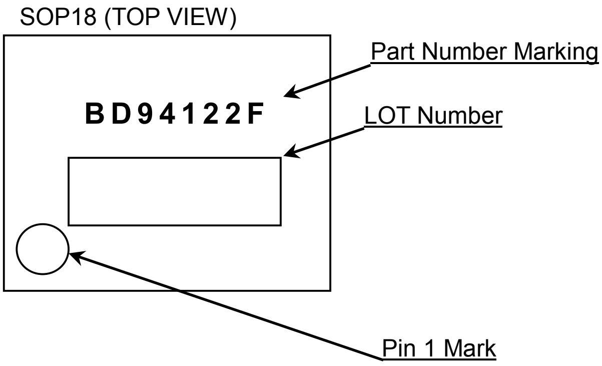
15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

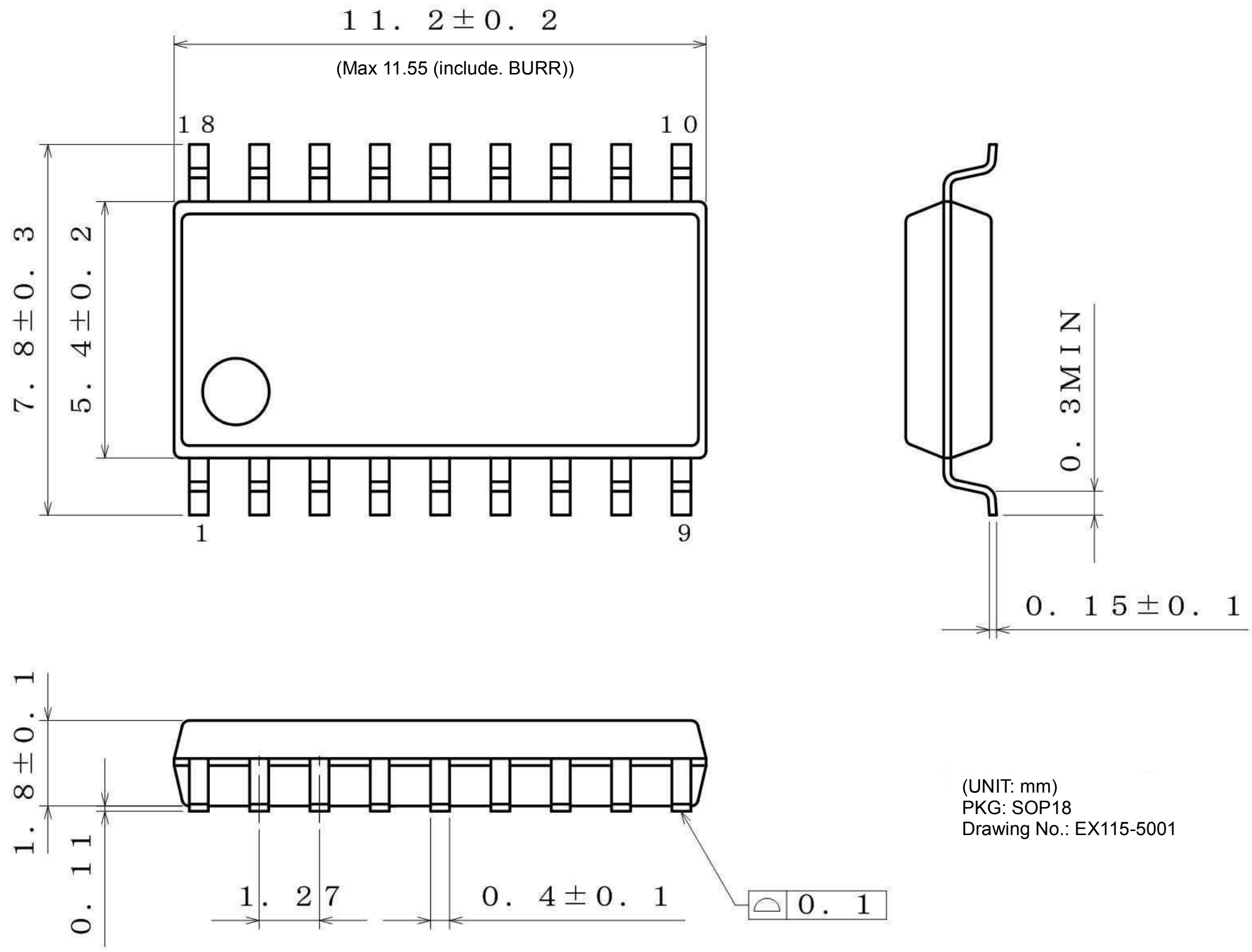


Marking Diagram



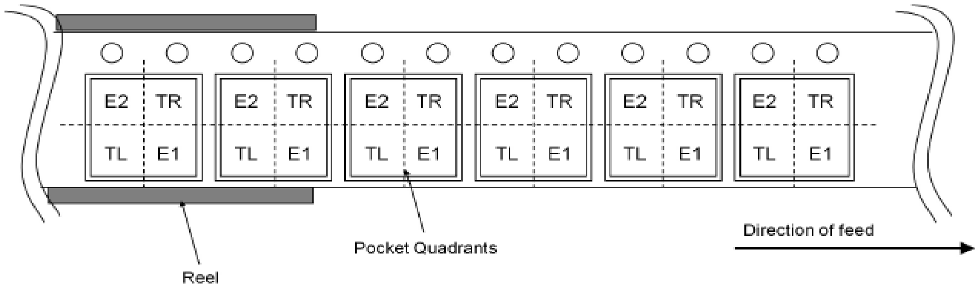
Physical Dimension and Packing Information

Package Name	SOP18



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
23.Mar.2018	001	New Release

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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