Secondary LDO Regulators

Secondary Variable Output LDO Regulator

BD00IC0WEFJ

No.11026EBT11

●Description

BD00IC0WEFJ is a LDO regulator with output current 1.0A. The output accuracy is ±1% of output voltage. With external resistance, it is available to set the output voltage at random (from 0.8V to 4.5V) and also provides output voltage fixed type without external resistance. It is used for the wide applications of digital appliances. It has package type: HTSOP-J8. Over current protection (for protecting the IC destruction by output short circuit), circuit current ON/OFF switch (for setting the circuit 0μA at shutdown mode), and thermal shutdown circuit (for protecting IC from heat destruction by over load condition) are all built in. It is usable for ceramic capacitor and enables to improve smaller set and long-life.

●Features

1) Output current 1.0A
2) High accuracy reference voltage circuit
3) Built-in Over Current Protection circuit (OCP)
4) Built-in Thermal Shut Down circuit (TSD)
5) With shut down switch
6) Output voltage variable type (0.8V to 4.5V)
7) Package: HTSOP-J8

●Output voltage differential Line up

Product name	Variable	Package
BD00IC0WEFJ	O	HTSOP-J8

Product name : B D 0 0 I C 0 W E F J

a b c d e

Signal	Description	
a	Output voltage	
	00	Variable
b	Voltage resistance	
	G	15V
	H	10V
	I	7V
c	Output current	
	A3	0.3A (G/H series)
	A5	0.5A (G/H/I series)
	C0	1.0A (G/H/I series)
	C5	1.5A (H series)
d	Shutdown switch	
	“W”	Shutdown switch is built in
e	Package	
	EFJ	HTSOP-J8

●**Absolute maximum ratings** (Ta=25℃)

Parameter		Symbol	Ratings	Unit
Power supply voltage		VCC	7.0 *1	V
EN voltage		VEN	7.0	V
Power dissipation	HTSOP-J8	Pd	2110 *2	mW
Operating Temperature Range		Topr	-25～+85	℃
Storage Temperature Range		Tstg	-55～+150	℃
Junction Temperature		Tjmax	+150	℃

*1 Not to exceed Pd
*2 Reduced by 16.9mW/℃ for each increase in Ta of 1℃ over 25℃. (when mounted on a board 70mm×70mm×1.6mm glass-epoxy board, two layer)

●**Operating conditions** (Ta=25℃)

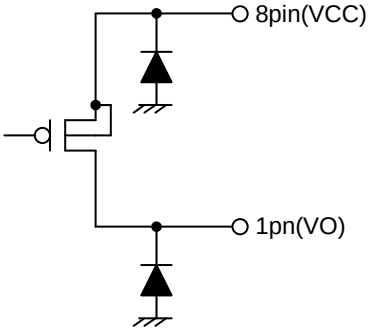
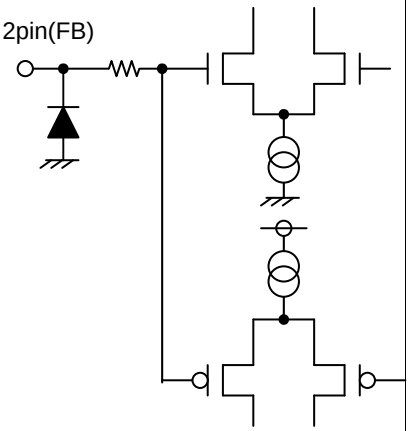
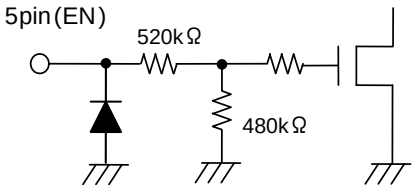
Parameter	Symbol	Ratings		Unit
		Min.	Max.	
Input power supply voltage	VCC	2.4	5.5	V
EN voltage	VEN	0.0	5.5	V
Output voltage setting range	VO	0.8	4.5	V
Output current	IO	0.0	1.0	A

This product should not be used in a radioactive environment.

●**Electrical characteristics** (Unless otherwise noted, Ta=25℃, EN=3V, VCC=3.3V, R1=16kΩ, R2=7.5kΩ)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Circuit current at shutdown mode	ISTB	-	0	5	μA	EN=0V, OFF mode
Bias current	ICC	-	250	500	μA	
Line regulation	Reg.Ii	-	25	50	mV	VCC=(VO+0.6V)→5.5V
Load regulation	Reg Io	-	25	75	mV	IO=0→1.0A
Minimun dropout Voltage	VCO	-	0.4	0.6	V	VCC=3.3V, IO=1.0A
Output reference voltage	VFB	0.792	0.800	0.808	V	IO=0A
EN Low voltage	VEN(Low)	0	-	0.8	V	
EN High voltage	VEN(High)	2.4	-	5.5	V	
EN Bias current	IEN	1	3	9	μA	

●**I/O Equivalent circuits**

8pin(VCC) / 1pin(VO)	2pin(FB)	5pin(EN)
		

●**Reference data (Unless otherwise noted, Ta=25℃, EN=3V, VCC=3.3V, R1=16kΩ, R2=7.5kΩ)**

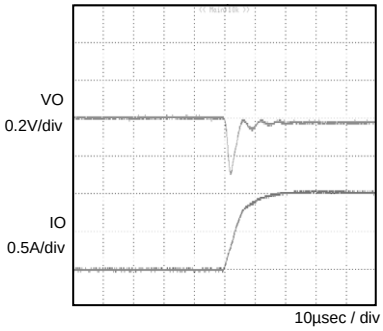


Fig.1 Transient Response(0→1.0A)
Co=2.2µF

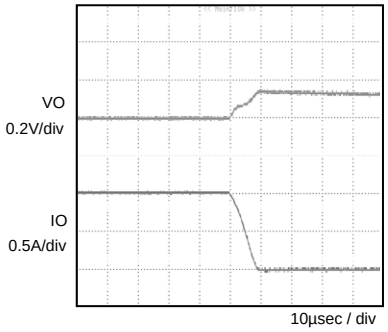


Fig.2 Transient Response(1.0→0A)
Co=2.2µF

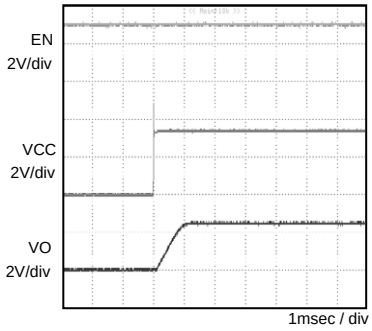


Fig.3 Input sequence1
Co=2.2µF

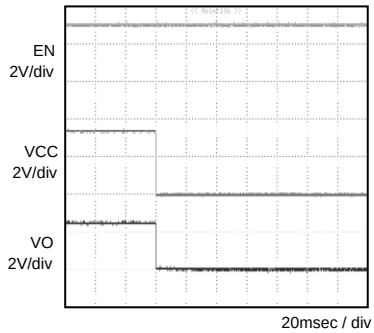


Fig.4 OFF sequence 1
Co=2.2µF

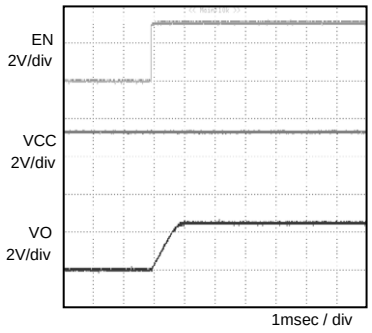


Fig.5 Input sequence2
Co=2.2µF

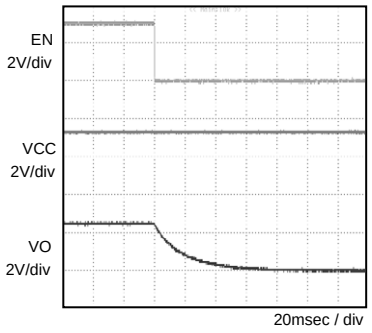


Fig.6 OFF sequence 2
Co=2.2µF

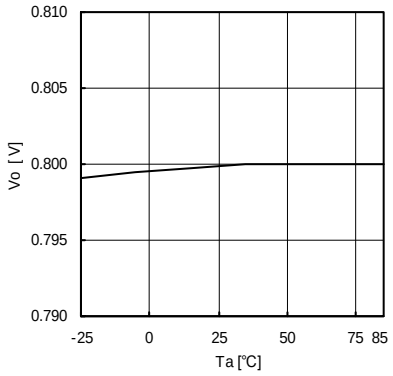


Fig.7 Ta-VFB

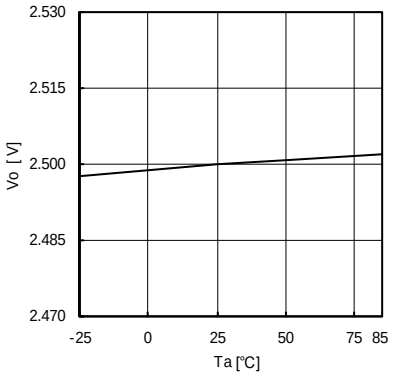


Fig.8 Ta-VO (IO=0A)

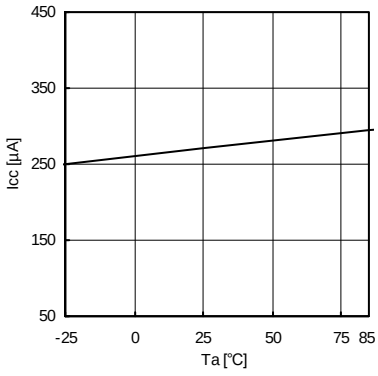


Fig.9 Ta-ICC

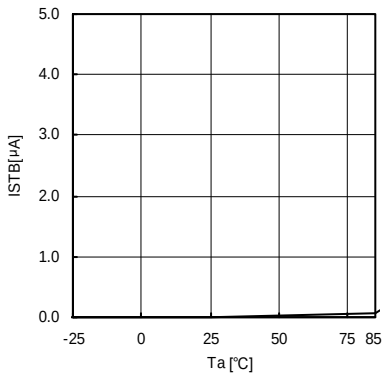


Fig.10 Ta-ISTB (VEN=0V)

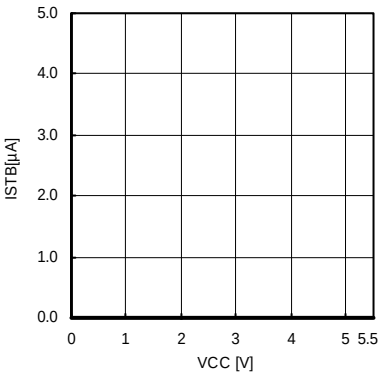


Fig.11 VCC-ISTB (VEN=0V)

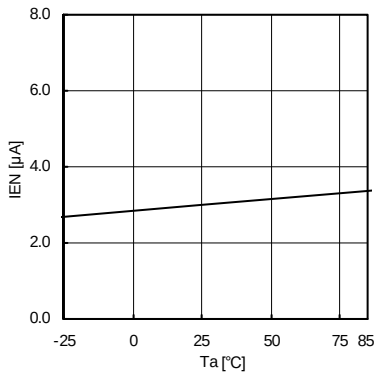


Fig.12 Ta-IEN

●Reference data

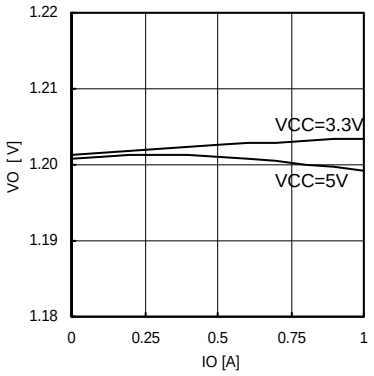


Fig.13 IO-VO (VO=1.2V)

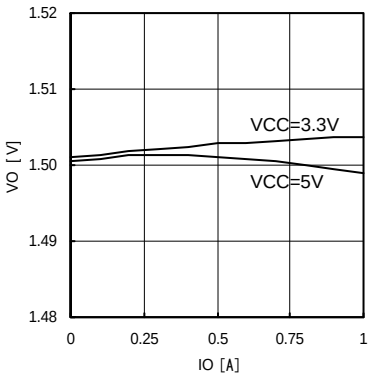


Fig.14 IO-VO (VO=1.5V)

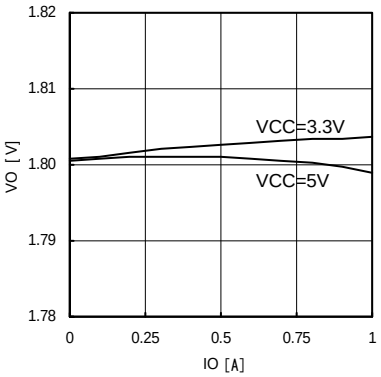


Fig.15 IO-VO (VO=1.8V)

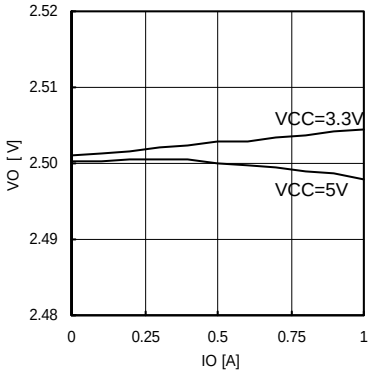


Fig.16 IO-VO (VO=2.5V)

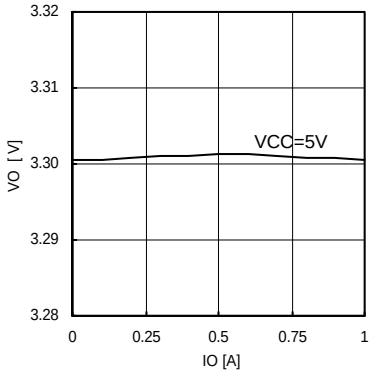


Fig.17 IO-VO (VO=3.3V)

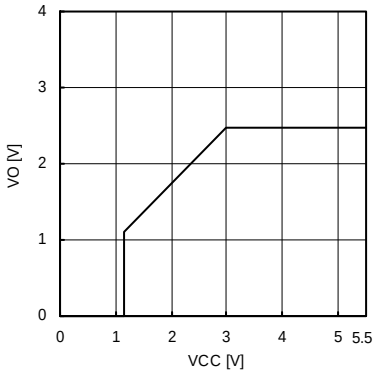


Fig.18 VCC-VO (IO=0A)

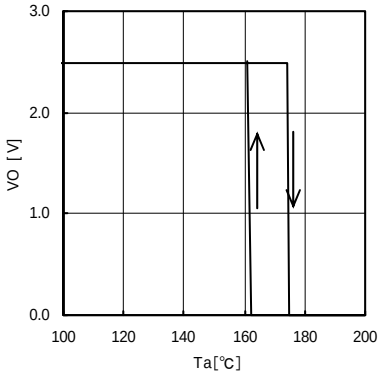


Fig.19 TSD (IO=0A)

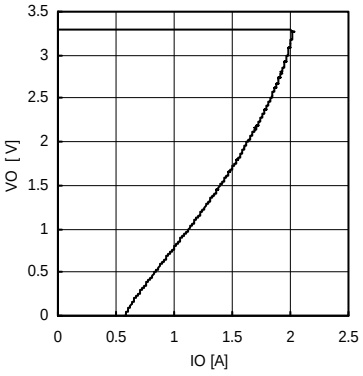


Fig.20 OCP
(VCC=5V, VO=3.3V)

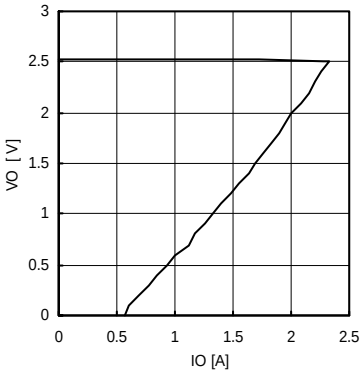


Fig.21 OCP
(VCC=5V, VO=2.5V)

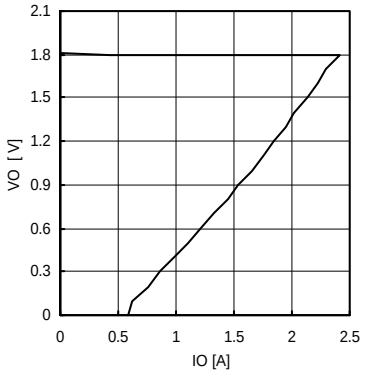


Fig.22 OCP
(VCC=5V, VO=1.8V)

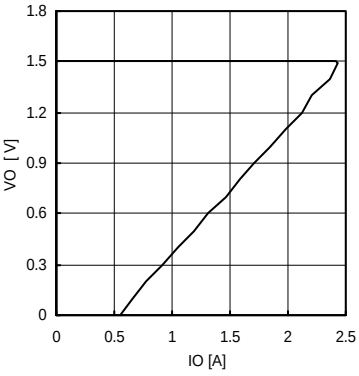


Fig.23 OCP
(VCC=5V, VO=1.5 V)

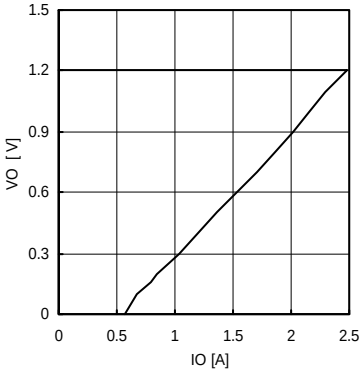


Fig.24 OCP
(VCC=5V, VO=1.2 V)

●Reference data

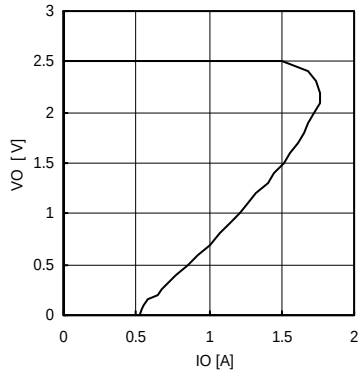


Fig.25 OCP
(VCC=3.3V, VO=2.5V)

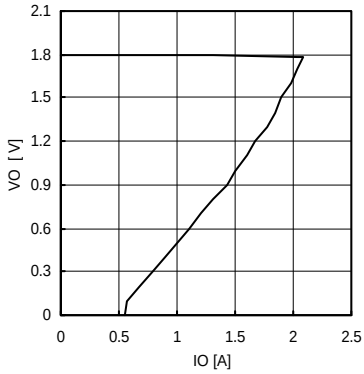


Fig.26 OCP
(VCC=3.3V, VO=1.8V)

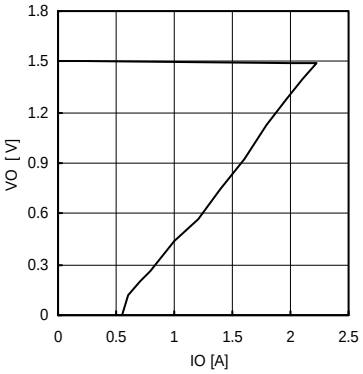


Fig.27 OCP
(VCC=3.3V, VO=1.5 V)

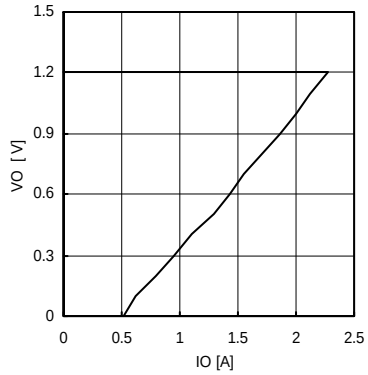


Fig.28 OCP
(VCC=3.3V, VO=1.2 V)

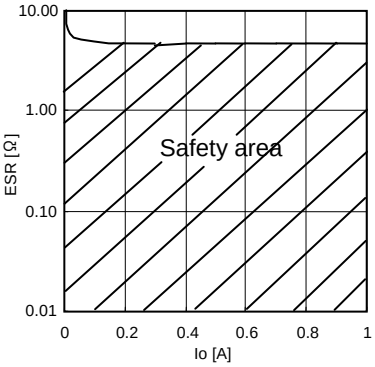


Fig.29 ESR-IO characteristics
(Co=2.2µF)

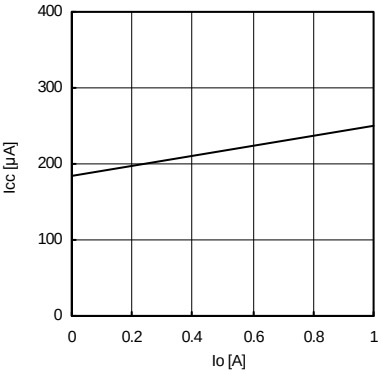


Fig.30 IO-ICC

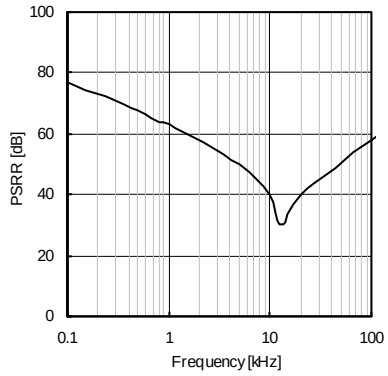


Fig.31 PSRR(IO=0A)

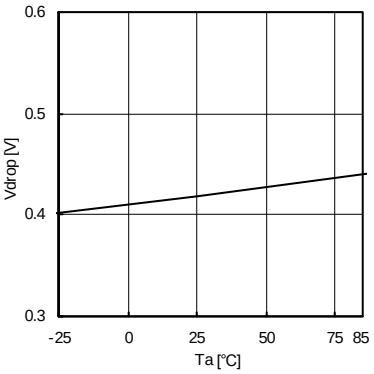


Fig.32 Minimum dropout Voltage 1
(VCC=3.3V, IO=1.0A)

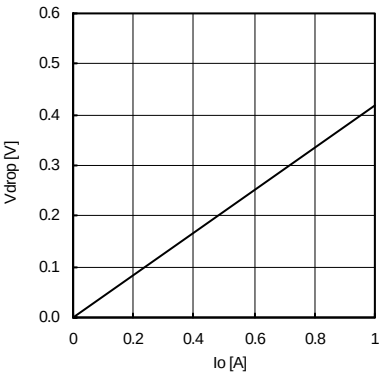


Fig.33 Minimum dropout Voltage2
(VCC=2.4V)

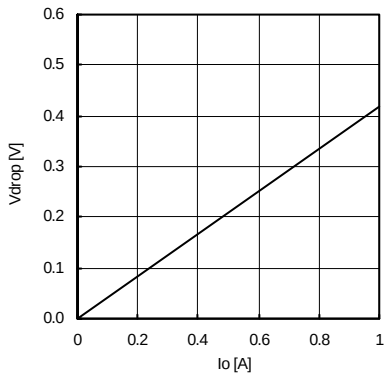


Fig.34 Minimum dropout Voltage3
(VCC=3.3V)

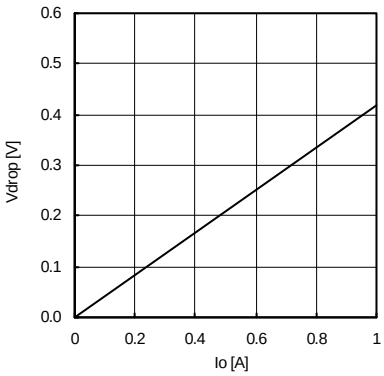
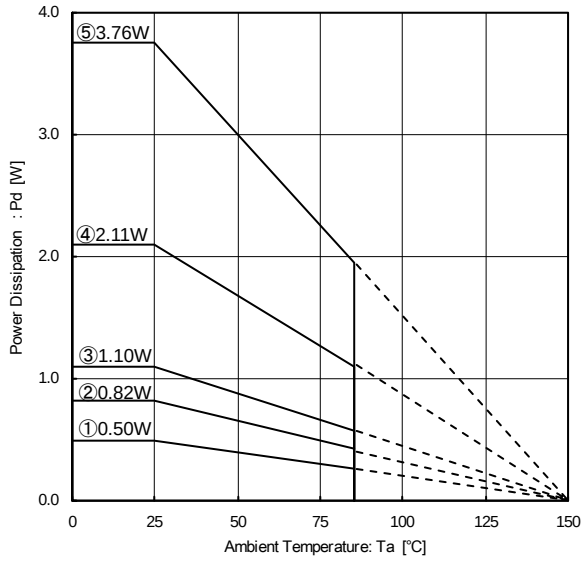


Fig.35 Minimum dropout Voltage4
(VCC=5.0V)

●Heat dissipation characteristics

◎HTSOP-J8



Measure condition: mounted on a ROHM board, and IC
Substrate size: 70mm × 70mm × 1.6mm
・Solder the substrate and package reverse exposure heat radiation part

① IC only
θj-a=249.5℃/W
② 1-layer(copper foil are :0mm×0mm)
θj-a=153.2℃/W
③ 2-layer(copper foil are :15mm×15mm)
θj-a=113.6℃/W
④ 2-layer(copper foil are :70mm×70mm)
θj-a=59.2℃/W
⑤ 4-layer(copper foil are :70mm×70mm)
θj-a=33.3℃/W

●Heat Loss

Thermal design should allow operation within the following conditions. Note that the temperatures listed are the allowed temperature limits, and thermal design should allow sufficient margin from the limits.

1. Ambient temperature Ta can be no higher than 85℃.
2. Chip junction temperature (Tj) can be no higher than 150℃.

Chip junction temperature can be determined as follows:

Calculation based on ambient temperature (Ta)
$Tj = Ta + \theta j\text{-}a \times P$

＜Reference values＞

θj-a：HTSOP-J8	153.2℃/W	1-layer substrate (copper foil density 0mm×0mm)
	113.6℃/W	2-layer substrate (copper foil density 15mm×15mm)
	59.2℃/W	2-layer substrate (copper foil density 70mm×70mm)
	33.3℃/W	4-layer substrate (copper foil density 70mm×70mm)
		Substrate size: 70mm×70mm×1.6mm (substrate with thermal via)

Most of the heat loss that occurs in the BD00IC0WEFJ is generated from the output Pch FET. Power loss is determined by the total VCC-VO voltage and output current. Be sure to confirm the system input and output voltage and the output current conditions in relation to the heat dissipation characteristics of the VCC and VO in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD00IC0WEFJ make certain to factor conditions such as substrate size into the thermal design.

$$\text{Power consumption [W]} = \left\{ \text{Input voltage (VCC) - Output voltage (VO)} \right\} \times \text{IO(Ave)}$$

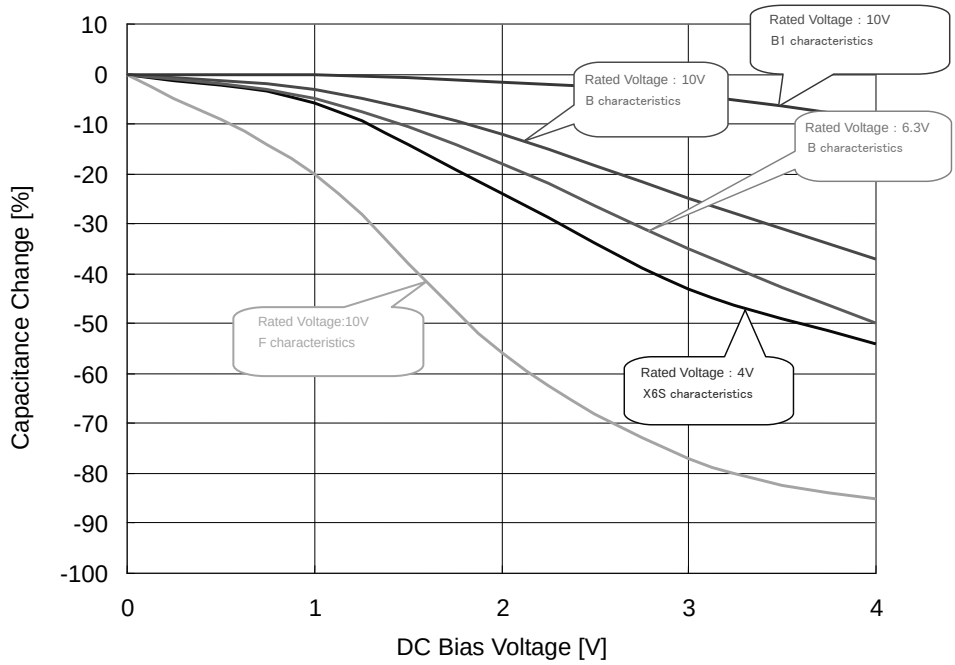
Example) When VCC=3.3V, VO=2.5V, IO(Ave) = 0.1A

$$\text{Power consumption [W]} = \left\{ 3.3\text{V} - 2.5\text{V} \right\} \times 0.1\text{A}$$

$$= 0.08\text{[W]}$$

●About Input-to-output capacitor

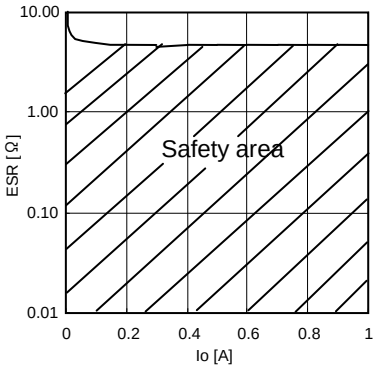
It is recommended that a capacitor is placed nearby pin between Input pin and GND, output pin and GND.
A capacitor, between input pin and GND, is valid when the power supply impedance is high or drawing is long. Also as for a capacitor, between output pin and GND, the greater the capacity, more sustainable the line regulation and it makes improvement of characteristics by load change. However, please check by mounted on a board for the actual application. Ceramic capacitor usually has difference, thermal characteristics and series bias characteristics, and moreover capacity decreases gradually by using conditions.
For more detail, please be sure to inquire the manufacturer, and select the best ceramic capacitor.



Ceramic capacitor capacity – DC bias characteristics
(Characteristics example)

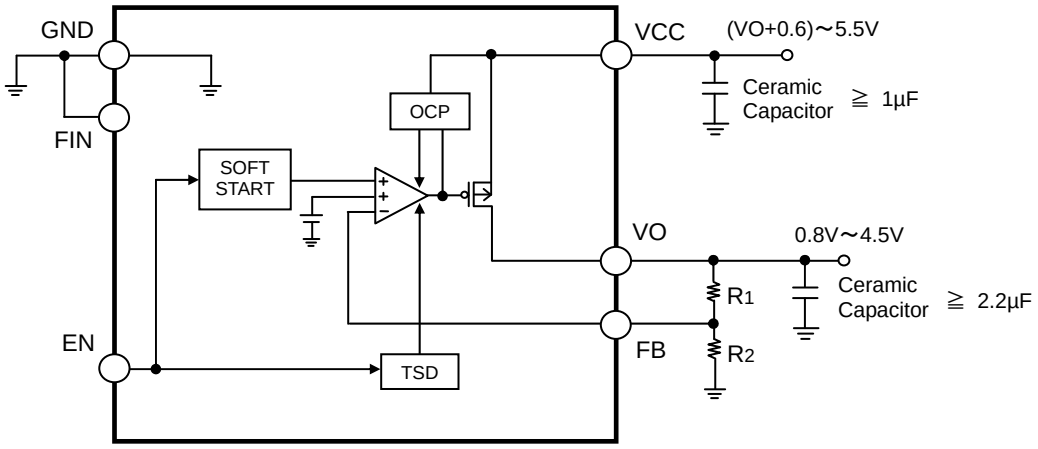
●About equivalent series resistance ESR (Output capacitor)

Please attach an anti-oscillation capacitor between VO and GND. Capacitor usually has ESR(Equivalent Series Resistance), and operates stable in ESR-IO range, showed right. Generally, ESR of ceramic, tantalum and electronic capacitor etc. is different for each, so please be sure to check a capacitor which is going to use, and use it inside the stable operating region, showed right. Then, please evaluate for the actual application.

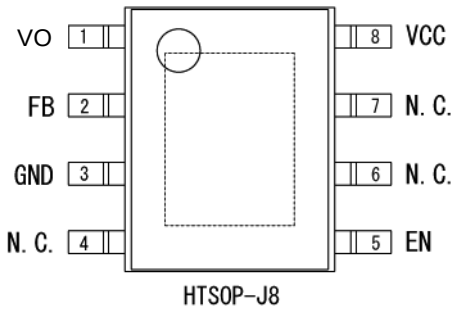


Stable area characteristics

●Block diagram

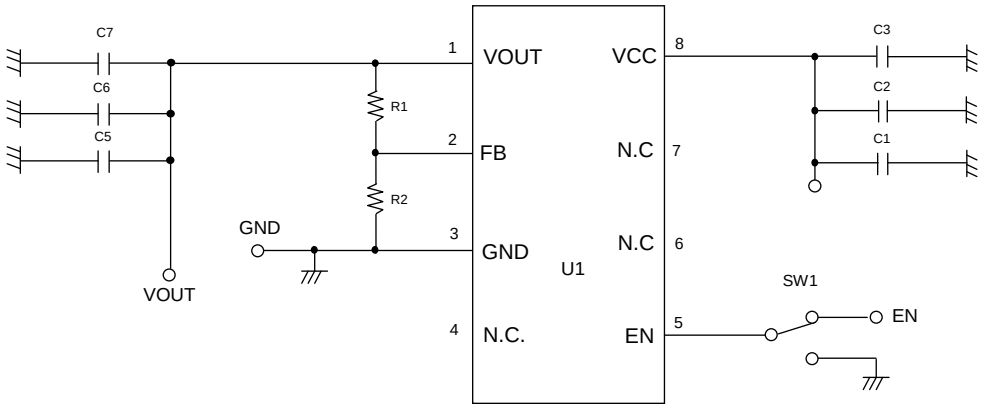


●Pin number・Pin name



Pin No.	Pin name	Pin Function
1	VO	Output pin
2	FB	Feedback pin
3	GND	GND pin
4	N.C.	Non Connection (Used to connect GND or OPEN state.)
5	EN	Enable pin
6	N.C.	Non Connection (Used to connect GND or OPEN state.)
7	N.C.	Non Connection (Used to connect GND or OPEN state.)
8	VCC	Input pin
Reverse	FIN	Substrate (Connect to GND)

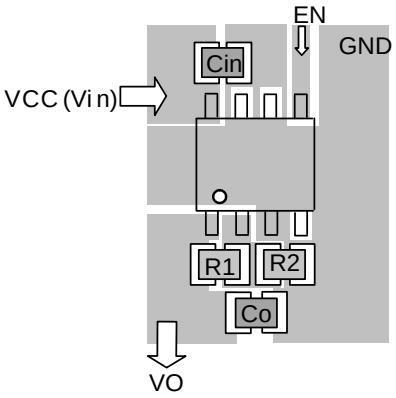
●Evaluation board circuit



●Evaluation board parts list

Designation	Value	Part No.	Company	Designation	Value	Part No.	Company
R1	16kΩ	MCR01PZPZF1602	ROHM	C4	-	-	-
R2	7.5kΩ	MCR01PZPZF7501	ROHM	C5	2.2µF	CM105B225K16A	KYOCERA
R3	-	-	-	C6	-	-	-
R4	-	-	-	C7	-	-	-
R5	-	-	-	C8	-	-	-
R6	-	-	-	C9	-	-	-
C1	1µF	CM105B105K16A	KYOCERA	C10	-	-	-
C2	-	-		U1	-	BD00IC0WEFJ	ROHM
C3	-	-		U2	-	-	-

●About board layout



- Input capacitor Cin of VCC (Vin) should be placed very close to VCC(Vin) pin as possible, and used broad wiring pattern. Output capacitor Co also should be placed close to IC pin as possible. In case connected to inner layer GND plane, please use several through hole.
- VFB pin has comparatively high impedance, and is apt to be effected by noise, so floating capacity should be minimum as possible. Please be careful in wiring drawing
- Please take GND pattern space widely, and design layout to be able to increase radiation efficiency.
- For output voltage setting
  Output voltage can be set by FB pin voltage(0.800V typ.)and external resistance R1, R2.

$$VO = VFB \times \frac{R_1+R_2}{R_2}$$

(The use of resistors with R1+R2=1k to 90k is recommended)

●Notes for use

(1) Absolute maximum ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

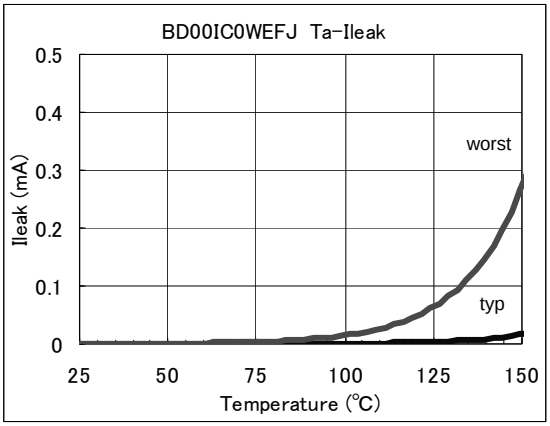
(2) Connecting the power supply connector backward
Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply lines
Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND voltage
The potential of GND pin must be minimum potential in all operating conditions.

(5) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6) Off-leak in high temperature.
Off-leak in high temperature may increase because of manufacturing of IC diviation.
Design in cousideration with graph of typ, worst is shown below.



(7) Inter-pin shorts and mounting errors
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

(8) Actions in strong electromagnetic field
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(9) ASO
When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(10) Thermal shutdown circuit
The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD ON Temperature[℃] (typ.)	Hysteresis Temperature [℃] (typ.)
BD00IC0WEFJ	175	15

(11) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

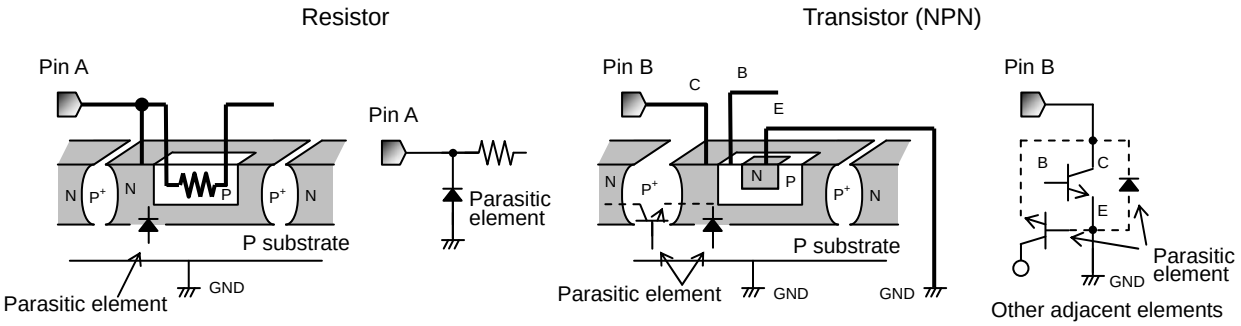
(12) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



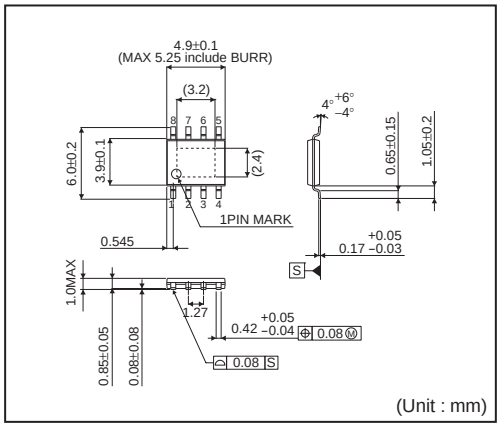
(13) Ground Wiring Pattern.

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●Ordering part number

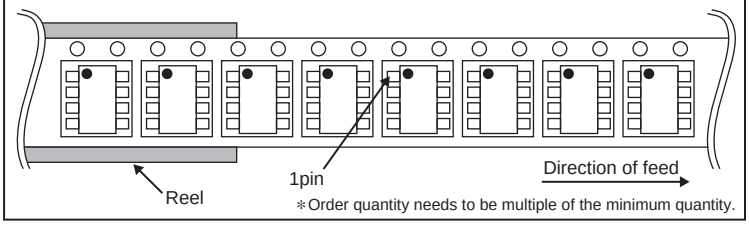
B D	0 0	I	C 0	W	E F J	-	E 2
ROHM Part Number	Output voltage 00 : Variable	Voltage resistance G :15V H :10V I :7V	Output cuurent A3:0.3A A5:0.5A C0:1.0A C5:1.5A	Shutdown switch "W" : Built in	Package EFJ : HTSOP-J8		Packaging specifications E2: Emboss tape reel

HTSOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

Notes

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