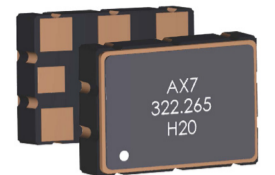


CLEARCLOCK™ | POWER OPTIMIZED 0.12ps 5x7mm XO



7.0 x 5.0 x 1.8 mm

RoHS/RoHS II Compliant

MSL = 1



ESD SENSITIVE

AX7

FEATURES

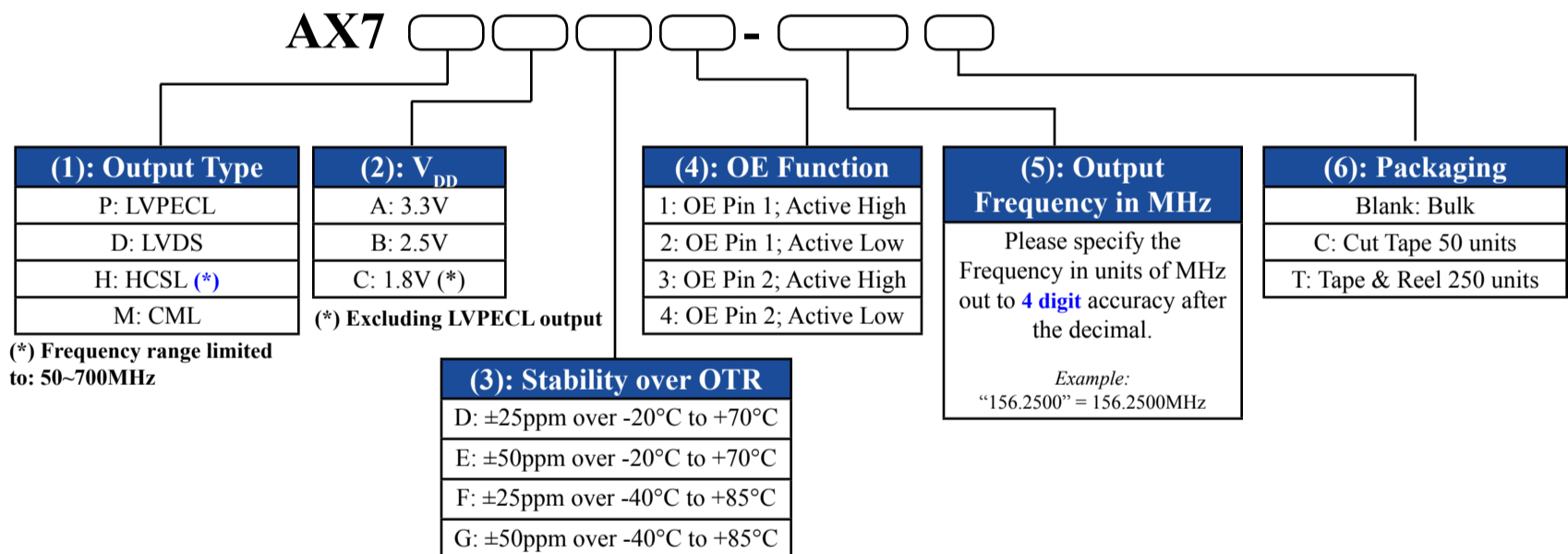
- 0.125ps typ jitter (150fs MAX $f > 200\text{MHz}$, 25°C)
- Highest in-class frequency range from 50 to 2100MHz
- Excellent spurious suppression
- 70mA MAX I_{DD} (LVDS, any V_{DD})
- Lowest in-class power consumption
- Supports LVPECL, HCSL, LVDS, CML
- Supports $\pm 50\text{ppm}$ or $\pm 100\text{ppm}$ all inclusive stability
- -40°C to 85°C or -20°C to 70°C operation
- Industry standard 5x7mm footprint

APPLICATIONS

- Networking and communications
- RF systems, base stations (BTS)
- Test and measurement
- Cloud, server and storage, Fibre Channel
- 100/400GbEthernet
- PCI Express

OPTIONS AND PART IDENTIFICATION [Note 1]

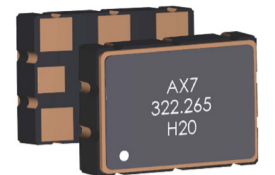
Note 1: Contact Abracon for part number requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal.



Part Number Example:

AX7PAF1-644.53125C

CLEARCLOCK™ | POWER OPTIMIZED 0.12ps 5x7mm XO



AX7

7.0 x 5.0 x 1.8 mm

RoHS/RoHS II Compliant

MSL = 1

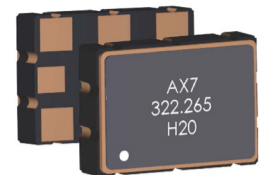


ESD SENSITIVE

COMMON KEY ELECTRICAL SPECIFICATIONS

Parameters		Min.	Typ.	Max.	Unit	Notes
Frequency Range	LVPECL	50		2100	MHz	Option "P"
	LVDS	50		2100		Option "D"
	HCSL	50		700		Option "H"
	CML	50		2100		Option "M"
Power Supply Voltage (V_{DD}) [Note 1]		2.97	3.3	3.63	V	Option "A"
		2.25	2.5	2.75		Option "B"
		1.71	1.8	1.89		Option "C"
Current Consumption (I_{DD})	LVPECL		87	94	mA	@ $V_{DD}=3.3V$
	LVDS		64	70		
	HCSL		75	80		@ $V_{DD}=1.8V$
	CML		63	68		
Set Tolerance (as received) @ 25°C ±3°C		-5.00	<±3.00	+5.00	ppm	Relative to carrier
Operating Temperature Range (OTR)		-40		+85	°C	See Options
Storage Temperature		-55		+155	°C	
Frequency Stability over OTR		-25		+25	ppm	Option "D or F"
		-50		+50		Option "E or G"
Aging over 10-Year Product Life [Note 2]		-15		+15	ppm	
All Inclusive Frequency Accuracy over 10-Year Product Life [Note 2]		-50		+50	ppm	Specific to freq. stability option "D" or "F" (±25ppm)
		-100		+100		Specific to freq. stability option "E" or "G" (±50ppm)
Rise (Tr) / Fall Time (Tf)	LVPECL/LVDS/CML			0.35	nS	20% ↔ 80% waveform
	HCSL			0.40		
Duty Cycle		45		55	%	@ 50% V_{DD}
Start-up Time [Note 2]			< 5.0	10	ms	
Output High Voltage (V_{OH}) Output Low Voltage (V_{OL})	LVPECL	V_{OH}	$V_{DD}-1.165$	$V_{DD}-0.8$	V	50Ω into $V_{DD}-2.0V$ or thevenin equivalent
		V_{OL}	$V_{DD}-2.0$	$V_{DD}-1.55$		
	LVDS	V_{OH}		1.4		100Ω between OUT and OUTN
		V_{OL}	0.9	1.1		
	HCSL	V_{OH}	0.66	1.15		50Ω to V_{DD}
		V_{OL}	0.0	0.15		
	CML	V_{OH}	$V_{DD}-0.085$	$V_{DD}=Max$		50Ω into GND
		V_{OL}	$V_{DD}-0.6$	$V_{DD}-0.32$		
Output Enable (OE) Control			$0.8*(V_{DD})$		V	
				$0.2*(V_{DD})$		

CLEARCLOCK™ | POWER OPTIMIZED 0.12ps 5x7mm XO



AX7

7.0 x 5.0 x 1.8 mm

RoHS/RoHS II Compliant

MSL = 1



ESD SENSITIVE

COMMON KEY ELECTRICAL SPECIFICATIONS

PARAMETERS	MIN.	TYP.	MAX.	UNIT	NOTES
Output Enable Time			2.5	ms	
Output Disable Time			10	µs	
Output Disable Current Consumption	LVPECL	85	86	mA	@ V _{dd} =3.3V
	LVDS	63	65		
	HCSL	77	78		@ V _{dd} =1.8V
	CML	62	67		
RMS Phase Jitter (12kHz -20MHz BW)					
	201.000MHz – 2100.000MHz	125	150	fsec	@ V _{dd} =3.3V
	50.000MHz – 200.000MHz	200	300		

Note 1: Supply Voltage (Vdd) = 1.8V option not available with LVPECL output

Note 2: Relative to initial measured frequency @ 25°C ±3°C

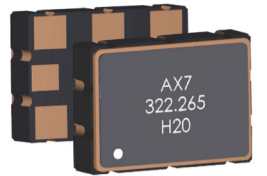
TYPICAL PHASE NOISE AND JITTER CHARACTERISTICS (@25°C ± 3°C) [Note 2]

Frequency (MHz)	148.35	150	155.52	156.25	156.25	200	212.5	312.5
RF Output	LVDS	LVPECL	LVPECL	LVPECL	HCSL	LVPECL	LVDS	LVDS
RMS Phase Jitter (fsec) 12kHz-20MHz BW	125	137	124	123	129	122	127	114
Phase Noise (dBc/Hz)	100Hz	-96	-98	-98	-99	-90	-83	-94
	1kHz	-120	-120	-120	-121	-121	-114	-115
	10kHz	-132	-132	-132	-132	-132	-129	-126
	100kHz	-140	-139	-141	-141	-140	-138	-134
	1MHz	-149	-150	-151	-150	-151	-148	-144
	10MHz	-157	-159	-159	-159	-160	-159	-157
	20MHz	-157	-159	-159	-159	-160	-159	-157

Frequency (MHz)	322.265625	491.52	644.53125	1000	1244.16	1500	2100
RF Output	LVPECL	HCSL	LVPECL	LVPECL	LVDS	LVDS	LVPECL
RMS Phase Jitter (fsec) 12kHz-20MHz BW	121	121	123	127	114	127	138
Phase Noise (dBc/Hz)	100Hz	-91	-92	-91	-77	-76	-78
	1kHz	-113	-114	-111	-107	-102	-102
	10kHz	-125	-125	-122	-119	-115	-113
	100kHz	-133	-133	-131	-127	-124	-122
	1MHz	-144	-144	-138	-138	-134	-131
	10MHz	-157	-157	-154	-154	-150	-149
	20MHz	-159	-159	-154	-155	-152	-150

Note 2: Refer to following Section for selected Phase Noise Plots

CLEARCLOCK™ | POWER OPTIMIZED 0.12ps 5x7mm XO



AX7

7.0 x 5.0 x 1.8 mm

Pb RoHS/RoHS II Compliant

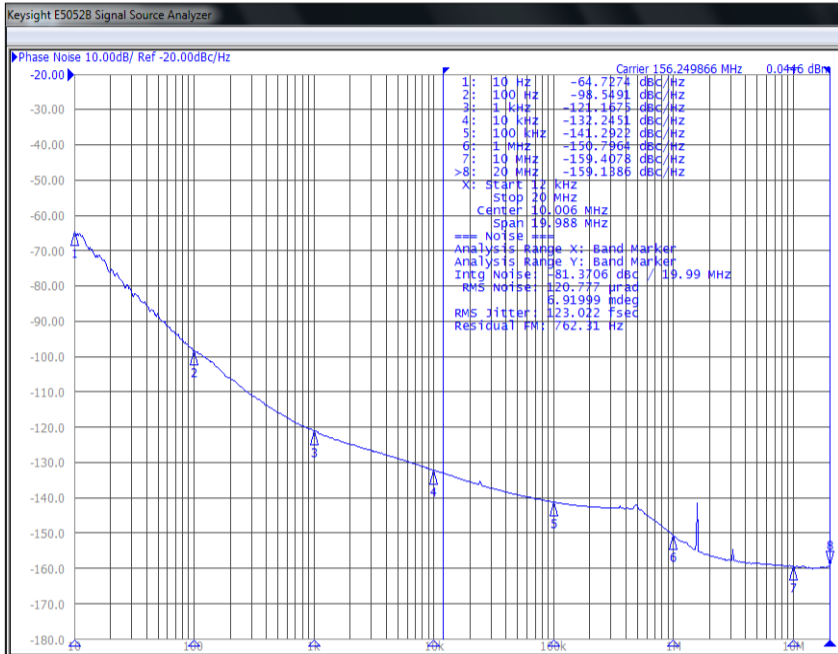
MSL = 1



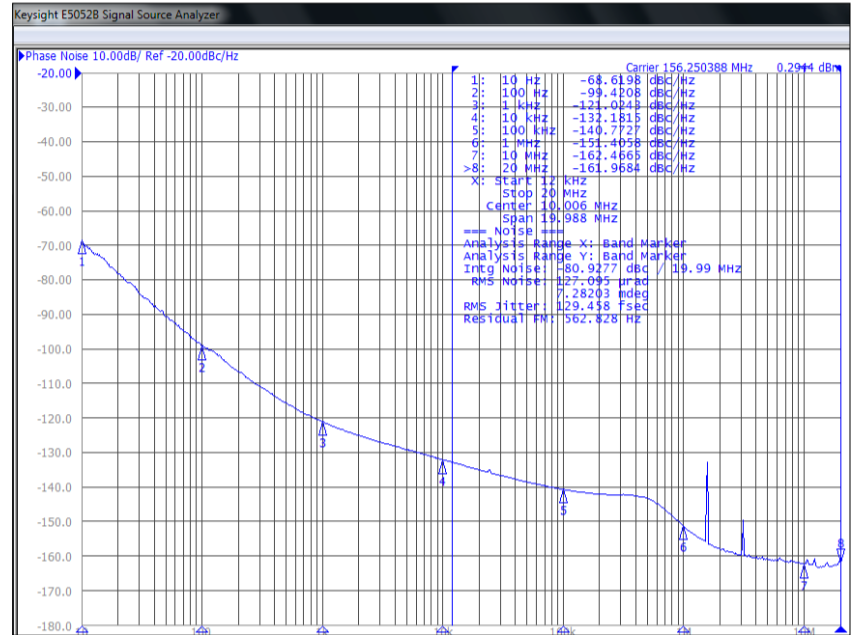
ESD SENSITIVE

SELECTED PHASE NOISE PLOTS (@25°C ± 3°C)

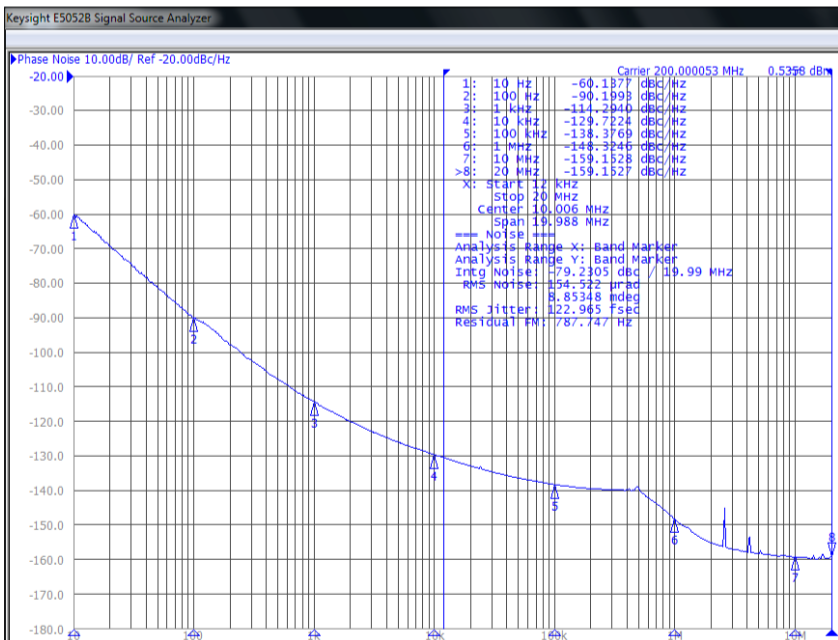
156.25MHz | LVPECL | V_{DD}=3.3V



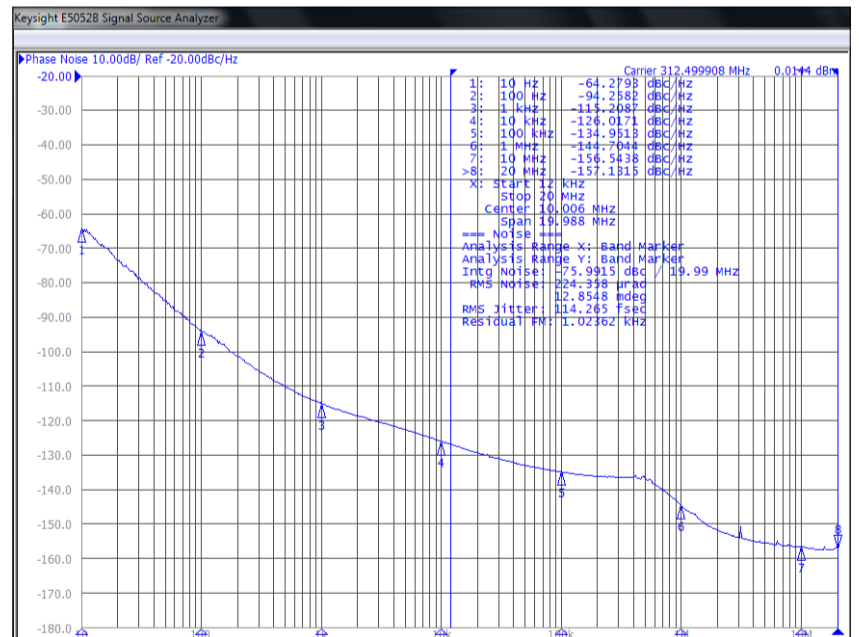
156.25MHz | HCSL | V_{DD}=1.8V



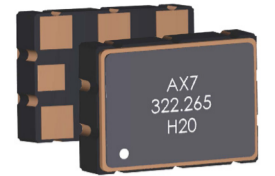
200MHz | LVPECL | V_{DD}=3.3V



312.5MHz | LVDS | V_{DD}=3.3V



CLEARCLOCK™ | POWER OPTIMIZED 0.12ps 5x7mm XO



AX7

7.0 x 5.0 x 1.8 mm

RoHS/RoHS II Compliant

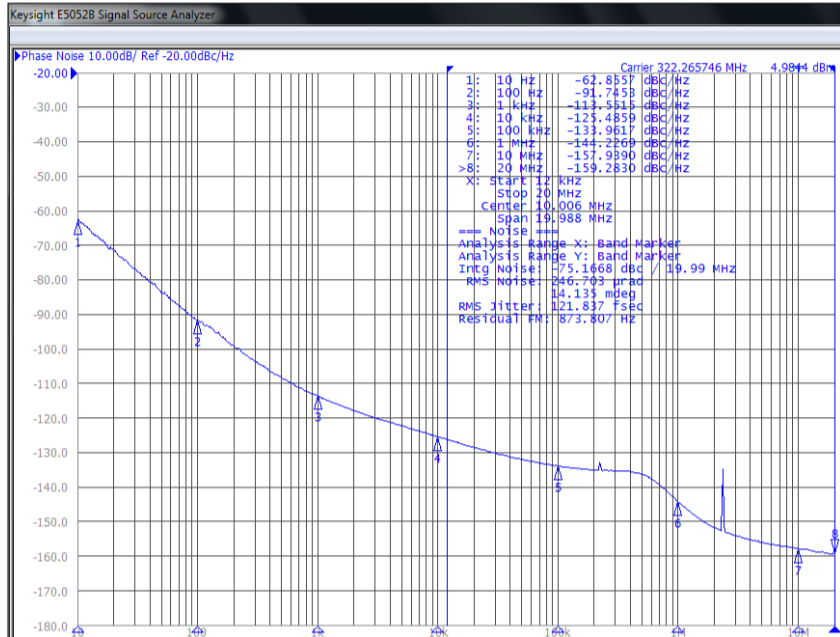
MSL = 1



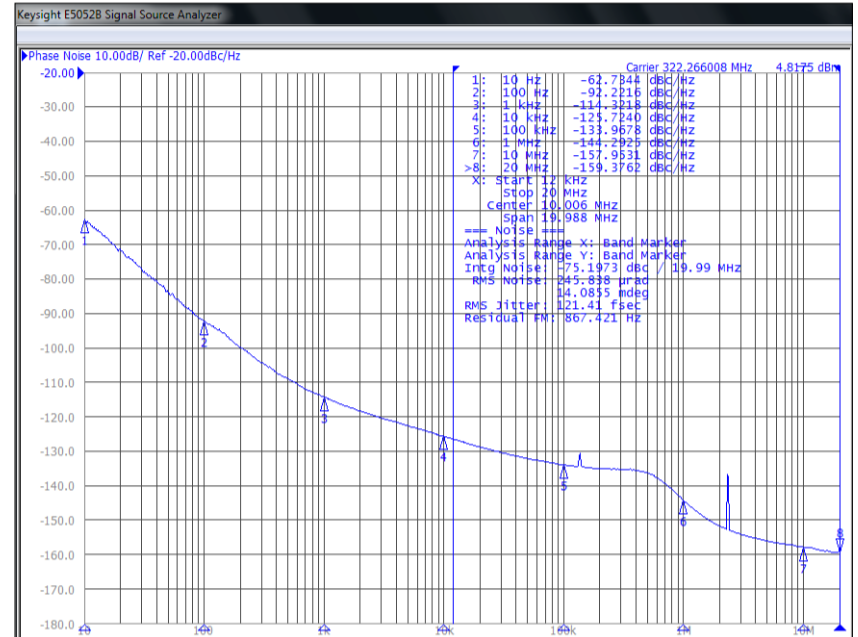
ESD SENSITIVE

SELECTED PHASE NOISE PLOTS (@25°C ± 3°C)

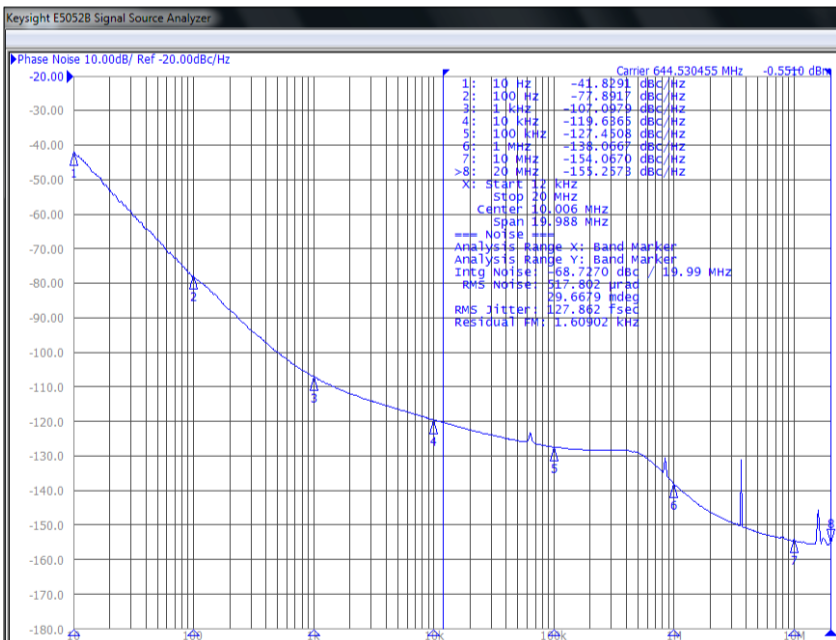
322.265625MHz | LVPECL | $V_{DD}=3.3V$



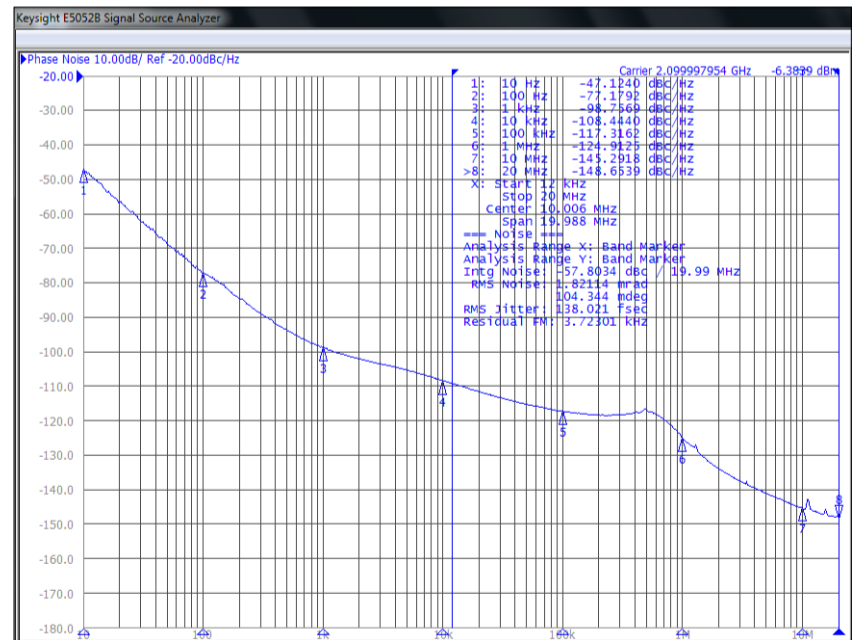
322.265625MHz | HCSL | $V_{DD}=3.3V$



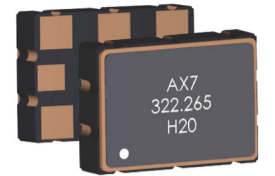
644.53125MHz | LVPECL | $V_{DD}=3.3V$



2100MHz | LVPECL | $V_{DD}=3.3V$



CLEARCLOCK™ | POWER OPTIMIZED 0.12ps 5x7mm XO



AX7

7.0 x 5.0 x 1.8 mm

RoHS/RoHS II Compliant

MSL = 1

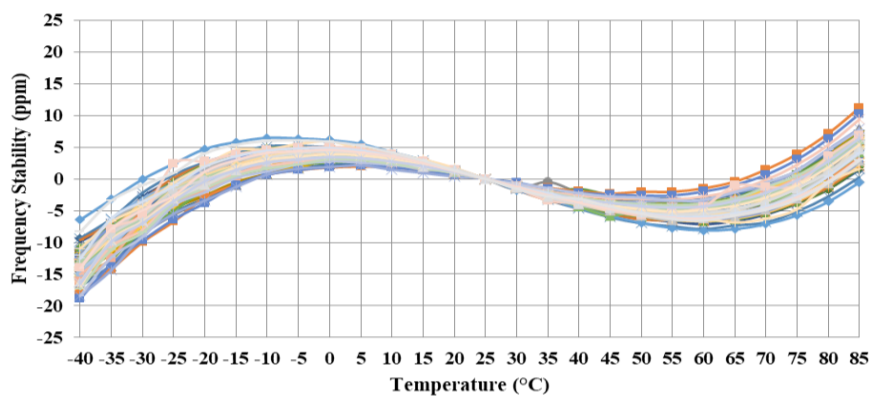


ESD SENSITIVE

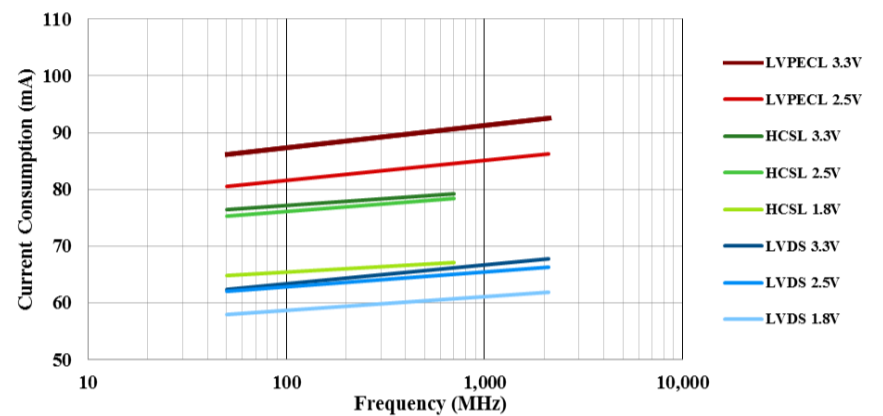
TYPICAL FREQUENCY Vs. TEMPERATURE CHARACTERISTICS

TYPICAL CURRENT CONSUMPTION (I_{DD}) Vs. FREQUENCY CHARACTERISTICS (@ 25°C ± 3°C)

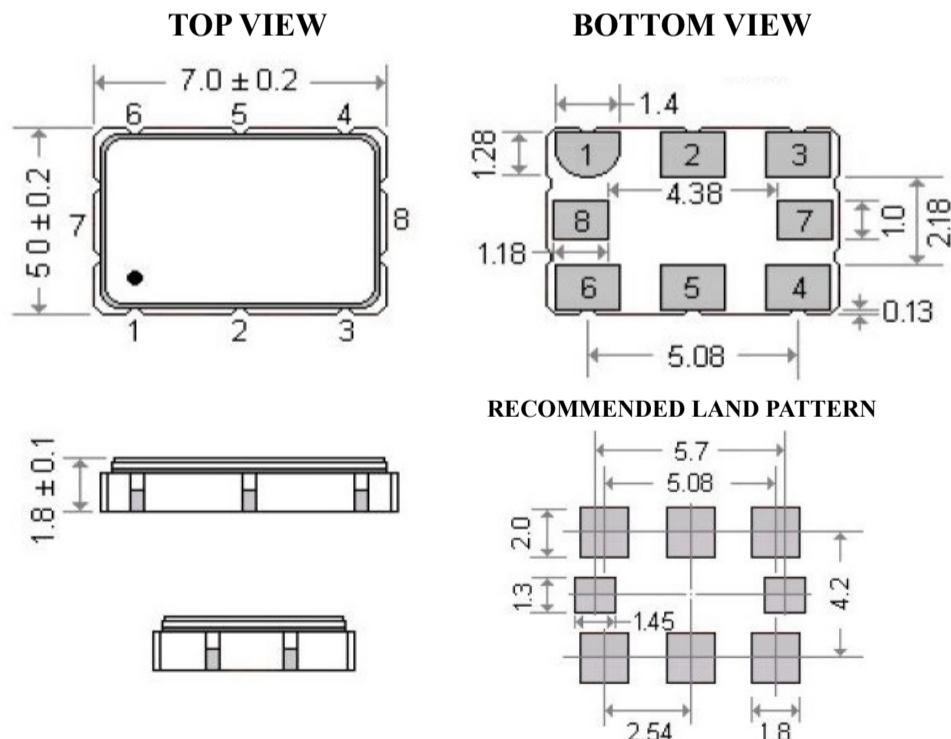
Frequency Stability vs. Temperature
AX7PAF1-122.8800 (50 units)



Current Consumption (I_{DD}) vs. Frequency
AX7



MECHANICAL DIMENSIONS

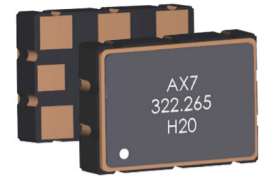


Dimensions: mm

PIN #	FUNCTION
# 1	Option 1 & 2: Output Enable/ Disable Option 3 & 4: No Connect
# 2	Option 1 & 2: No Connect Option 3 & 4: Output Enable/ Disable
# 3	GND
# 4	Output
# 5	Complementary output
# 6	Supply Voltage (V_{DD})
# 7	No connect
# 8	No connect

*Compatible with industry standard 5x7mm footprint. Pin 7 and 8 are no connect solder pads, not required.

CLEARCLOCK™ | POWER OPTIMIZED 0.12ps 5x7mm XO



AX7

7.0 x 5.0 x 1.8 mm

RoHS/RoHS II Compliant

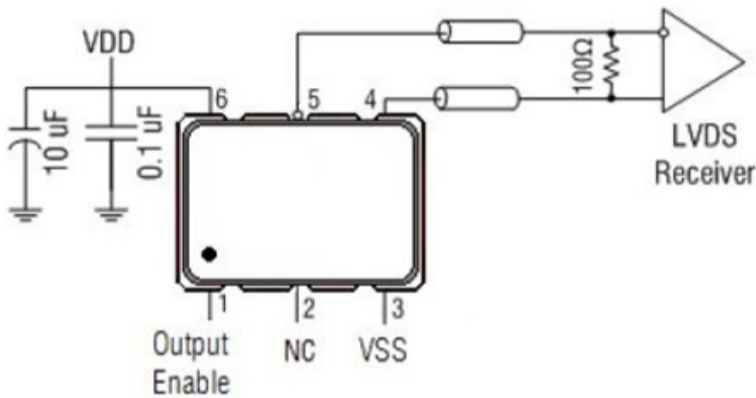
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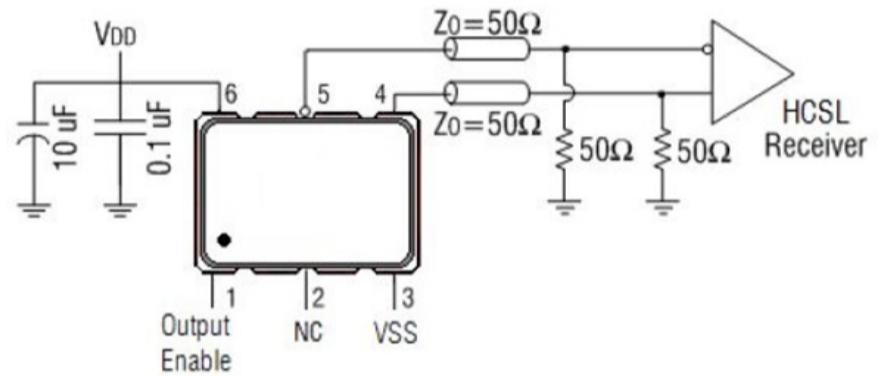
ESD SENSITIVE

RECOMMENDED TEST CIRCUIT

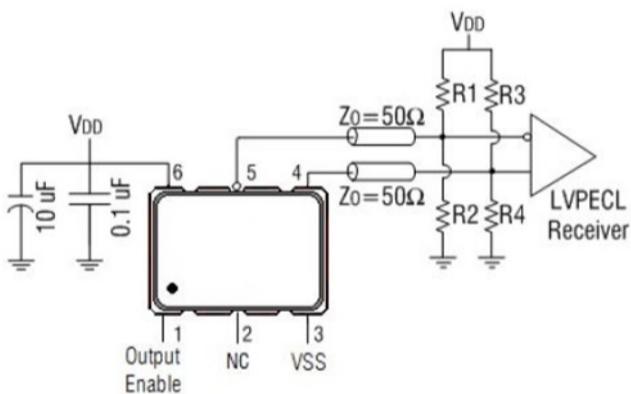
LVDS



HCSL

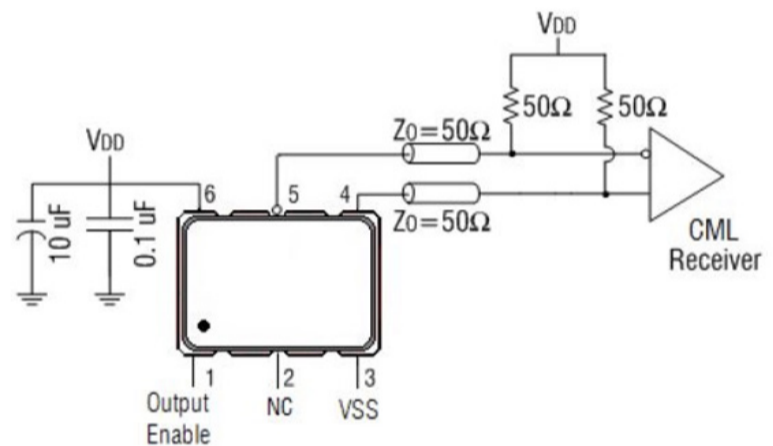


LVPECL

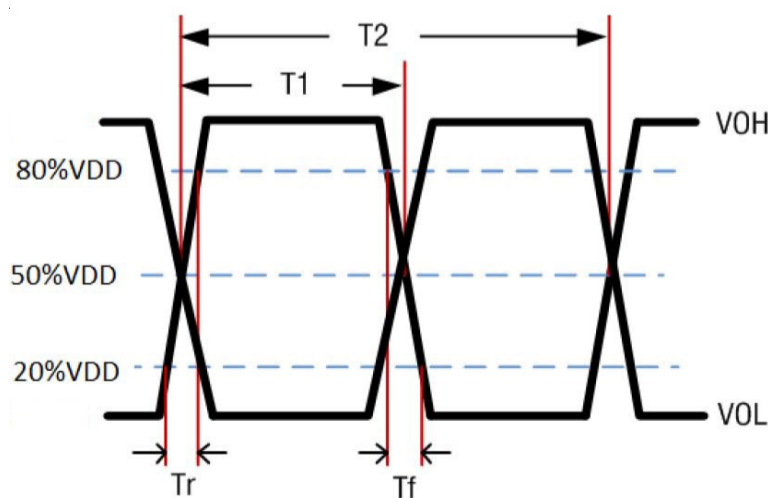


$V_{DD}=3.3V$: $R1=R3=127\Omega$; $R2=R4=82.5\Omega$
 $V_{DD}=2.5V$: $R1=R3=250\Omega$; $R2=R4=62.5\Omega$

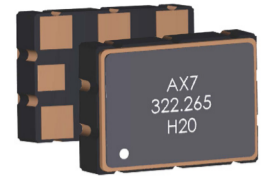
CML



DIFFERENTIAL OUTPUT WAVEFORM



CLEARCLOCK™ | POWER OPTIMIZED 0.12ps 5x7mm XO



AX7

7.0 x 5.0 x 1.8 mm

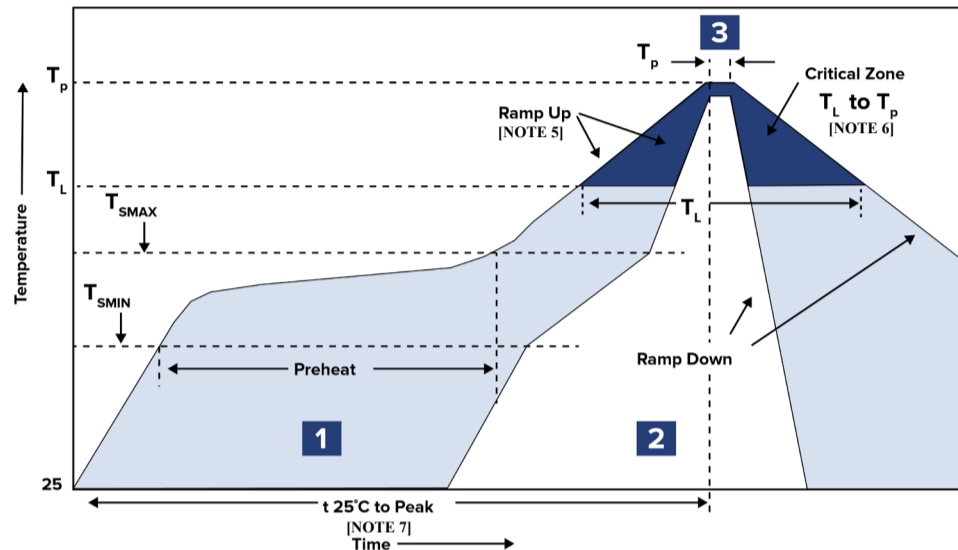
RoHS/RoHS II Compliant

MSL = 1



ESD SENSITIVE

REFLOW PROFILE



ZONE	DESCRIPTION	TEMPERATURE	TIME
1	Preheat / Soak	$T_{SMIN} \sim T_{SMAX}$ 150°C ~ 200°C	60 ~ 180 sec.
2	Reflow	T_L 217°C	60 ~ 150 sec.
3	Peak heat	T_P 260°C ± 5°C	20 ~ 40 sec.

Note 5: Ramp Up Rate ($T_L \rightarrow T_P$) = 3°C / sec. MAX

Note 6: Ramp Down Rate ($T_P \rightarrow T_L$) = 6°C / sec. MAX

Note 7: Time 25°C to Peak Temperature (25°C → T_P) = 8 minutes MAX

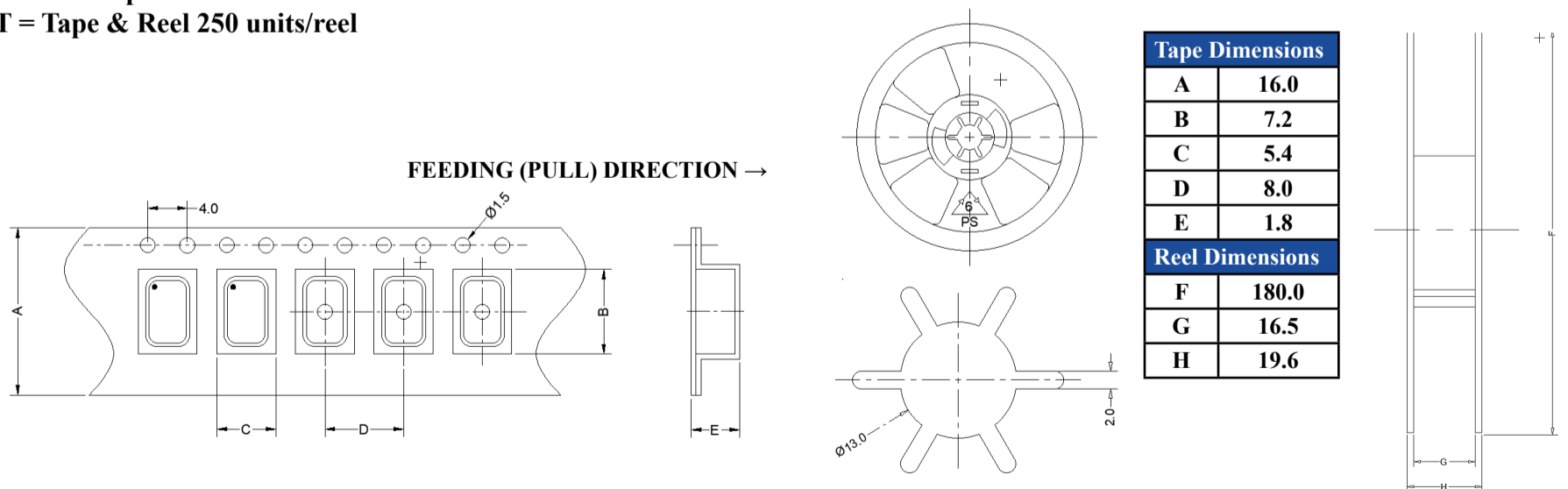
*Can withstand 2 times reflow

*All temperatures refer to topside of the package, measured on the package body surface

PACKAGING

C = Cut Tape 50 units

T = Tape & Reel 250 units/reel



Dimensions: mm