

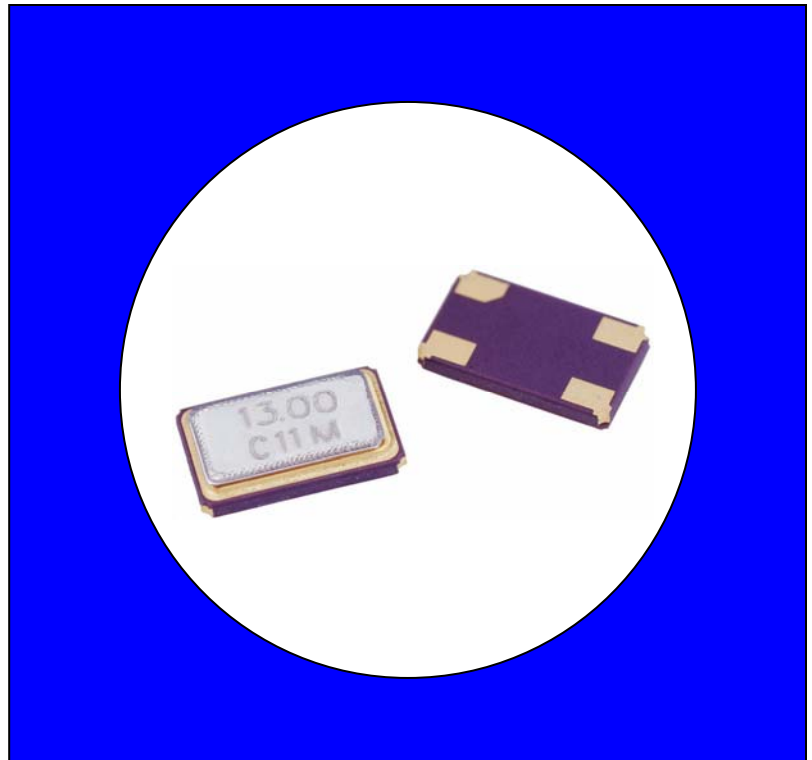


FEATURES

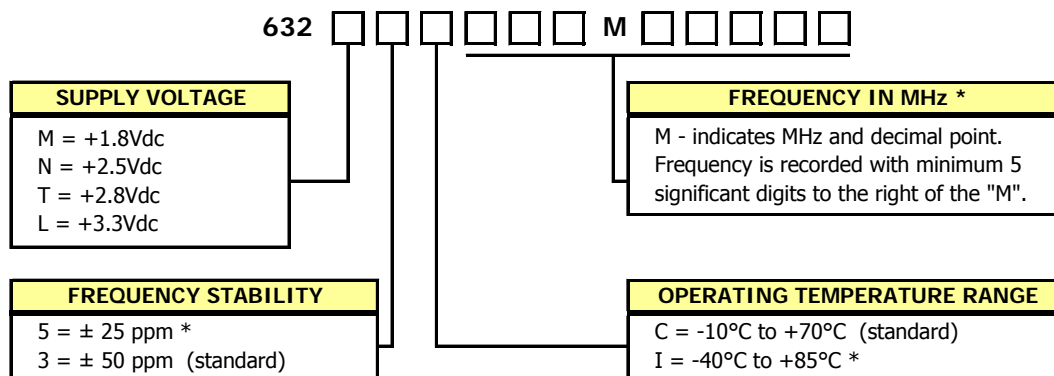
- Standard 3.2x2.5mm Surface Mount Footprint
- HCMOS/TTL Compatible
- **Fundamental and 3RD Overtone Crystals**
- Frequency Range 1.0 – 75 MHz
- Frequency Stability, ± 50 ppm
- +1.8Vdc, +2.5Vdc, +2.8Vdc, +3.3Vdc Operation
- Operating Temperature to -10°C to $+70^{\circ}\text{C}$
- Output Enable Standard
- Tape & Reel Packaging
- **RoHS/Green Compliant (6/6)**

DESCRIPTION

The Model 632 is a ceramic packaged Clock oscillator offering reduced size and enhanced stability. The small size means it is perfect for any application. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.



ORDERING INFORMATION



* Contact factory for availability.

Example Part Number: 632L3C032M76800

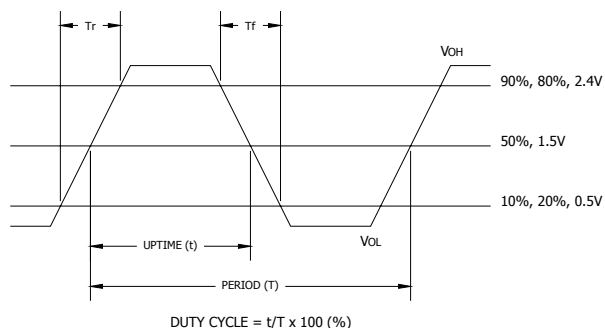
ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT		
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	4.0	V		
	Storage Temperature	T_{STG}	-	-55	-	125	°C		
	Frequency Range (See Note 1)	f_0	-	1.0	-	75	MHz		
	Frequency Stability (See Note 2 and Ordering Information)	$\Delta f/f_0$	-	-	-	50	± ppm		
	Aging	$\Delta f/f_0$	-	-	-	3	± ppm/yr		
	Operating Temperature Commercial Industrial	T_A	-	-10 -40	25	70 85	°C		
Electrical and Waveform Parameters	Supply Voltage Model 632M Model 632N Model 632T Model 632L	V_{CC}	± 10 %	1.62 2.25 2.52 2.97	1.8 2.5 2.8 3.3	1.98 2.75 3.08 3.63	V		
	Supply Current	I_{CC}	1.0 MHz to 20 MHz $C_L=15pF$	-	-	6	mA		
	Model 632M		20.1 MHz to 40 MHz $C_L=15pF$	-	-	7			
			40.1 MHz to 75 MHz $C_L=15pF$	-	-	10			
			1.0 MHz to 20 MHz $C_L=15pF$	-	-	8			
	Model 632N / Model 632T		20.1 MHz to 40 MHz $C_L=15pF$	-	-	10			
			40.1 MHz to 75 MHz $C_L=15pF$	-	-	10			
			1.0 MHz to 20 MHz $C_L=15pF$	-	-	10			
	Model 632L		20.1 MHz to 40 MHz $C_L=15pF$	-	-	15			
			40.1 MHz to 75 MHz $C_L=15pF$	-	-	15			
			Output Load	C_L					15
	Output Voltage Levels Logic '1' Level Logic '0' Level		V_{OH} V_{OL}	CMOS Load CMOS Load	$90\%V_{CC}$ -	- -		- $10\%V_{CC}$	V
	Output Current Logic '1' Level Logic '0' Level		I_{OH} I_{OL}	$V_{OH} = 90\%V_{CC}$ (1.8V, 2.5/2.8V, 3.3V) $V_{OL} = 10\%V_{CC}$ (1.8V, 2.5/2.8V, 3.3V)	- -	- -		-2, -4, -8 +2, +4, +8	mA
	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%		
	Rise and Fall Time	T_{R}, T_F	@ 10% - 90% Levels, $C_L = 15$ pF			10	ns		
	Start Up Time	T_S	Application of V_{CC}	-	-	10	ms		
	Enable Function Enable Input Voltage Disable Input Voltage	V_{IH} V_{IL}	Pin 1 Logic '1', Output Enabled Pin 1 Logic '0', Output Disabled	$0.7*V_{CC}$ -	- -	- $0.3*V_{CC}$	V		
	Enable Time	T_{PLZ}	Pin 1 Logic '1'	-	-	10	ms		
	Standby Current	I_{ST}	Pin 1 Logic '0', Output Disabled	-	-	10	uA		
	Period Jitter, Pk-Pk	-	-	-	-	100	ps		
	Period Jitter, RMS	-	-	-	-	25			
	Phase Jitter, RMS	-	Bandwidth 12 kHz - 20 MHz	-	< 2	-			

Notes:

- Contact factory for available frequencies.
- Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and aging.

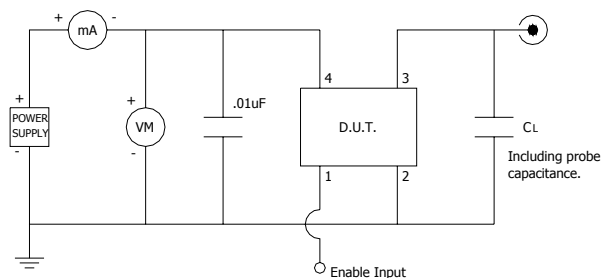
CMOS/TTL OUTPUT WAVEFORM



ENABLE TRUTH TABLE

PIN 1	PIN 3
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

TEST CIRCUIT, CMOS LOAD

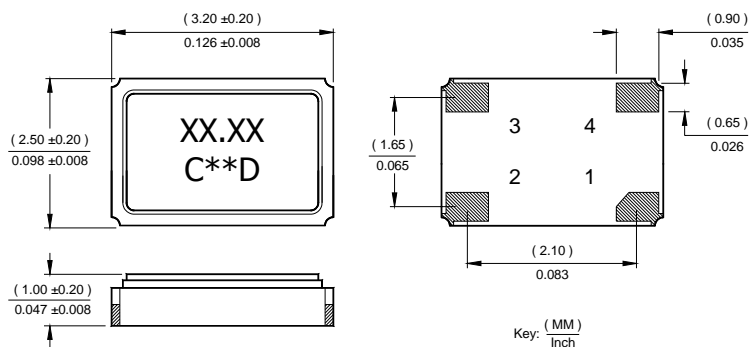


D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable Input
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V _{CC}	Supply Voltage

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

1. XX.XX – Frequency in MHz.
2. C – CTS and Pin 1 identifier.
3. ** – Manufacturing Site Code.
4. D – Manufactured Date Code. See Table I for codes.

NOTES

1. Termination pads (e4), barrier-plating is nickel (Ni) with gold (Au) flash plate.
2. Reflow conditions per JEDEC J-STD-020.

SUGGESTED SOLDER PAD GEOMETRY

